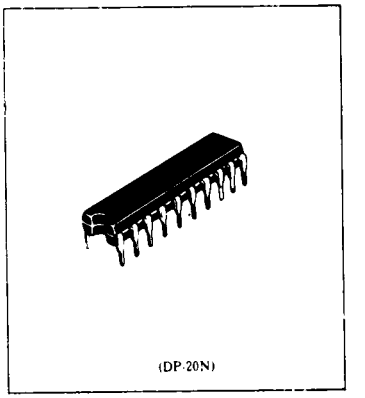
4096-word x 4-bit High Speed CMOS Static RAM



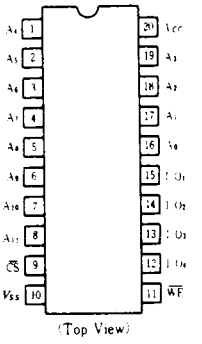
■FEATURES

- Single 5V Supply and High Density 20 Pin Package.
- High Speed: Fast Access Time 25/35/45ns (max.)
- Low Power Standby: 100μW typ, 5μW typ (L-version)
  Active: 250mW typ.
- Completely Static Memory: No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible – All Inputs and Outputs
- Capability of Battery Back Up Operation (L-version)

■ORDERING INFORMATION

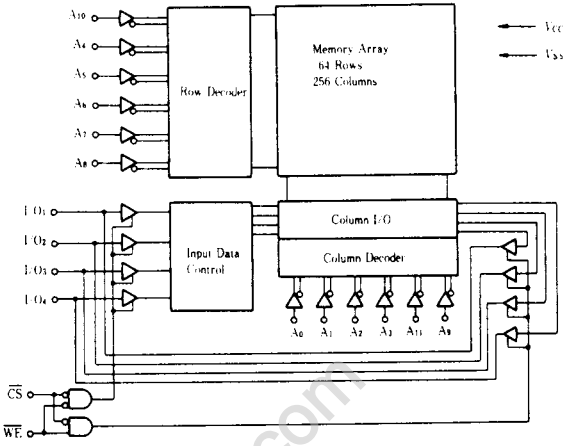
Type No.	Access Time	Package
HM6268P-25 HM6268P-35 HM6268P-45	25ns 35ns 45ns	300mil 20pin Plastic DIP
HM6268LP-25 HM6268LP-35 HM6268LP-45	25ns 35ns 45ns	

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.5V for pulse width≦10ns.

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	Din	Write Cycle

■RECOMMENDED OPERATING CONDITIONS (Ta = 0 to +70℃)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width≦10ns.

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C

Parameter	Symbol	Test Condition	Min.	Typ.*1	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA, min. cycle	–	50*3	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, min. cycle	–	15	25	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}$ ≥ V_{CC} −0.2V, 0V ≤ V_{IN} ≤ 0.2V or V_{CC} − 0.2V ≤ V_{IN}	–	0.02	2.0	mA
			–	1.2	50*2	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −0.4mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC} = 5.0V, Ta = +25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. 40mA typ. for 45ns version.

■CAPACITANCE (Ta=25°C, f=1.0MHz)

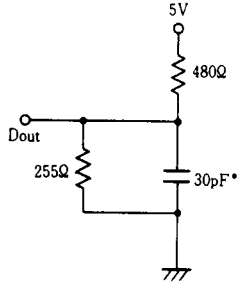
Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	9	pF

Note: This parameter is sampled and not 100% tested.

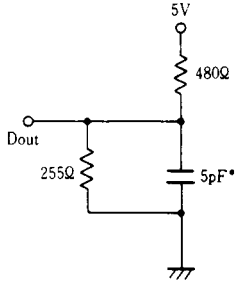
■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70℃, unless otherwise noted.)

- **AC Test Conditions**
  Input pulse levels: V_{SS} to 3.0V
  Input rise and fall times: 5ns
  Input and Output timing reference levels: 1.5V
  Output load: See Figure

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



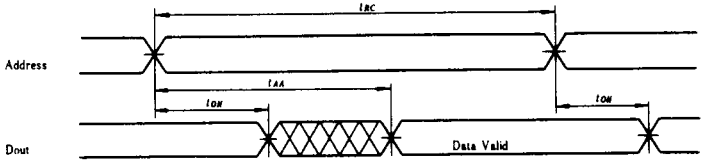
*Including scope and jig.

● READ CYCLE

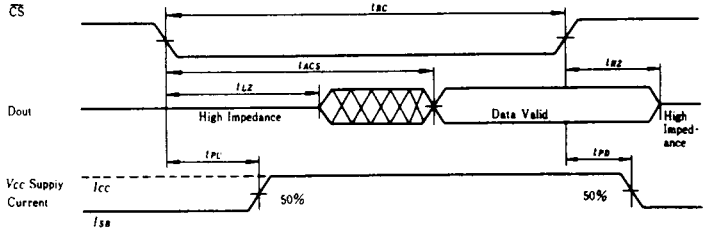
Parameter	Symbol	HM6268-25		HM6268-35		HM6268-45		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	25	–	35	–	45	–	ns
Address Access Time	t_{AA}	–	25	–	35	–	45	ns
Chip Select Access Time	t_{ACS}	–	25	–	35	–	45	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns
Chip Selection to Output in Low Z	t_{LZ}*1	10	–	10	–	10	–	ns
Chip Deselection to Output in High Z	t_{HZ}*1	0	15	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	25	–	25	–	30	ns

Note) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No. 1(1),(2)



● Timing Waveform of Read Cycle No. 2(1),(3)



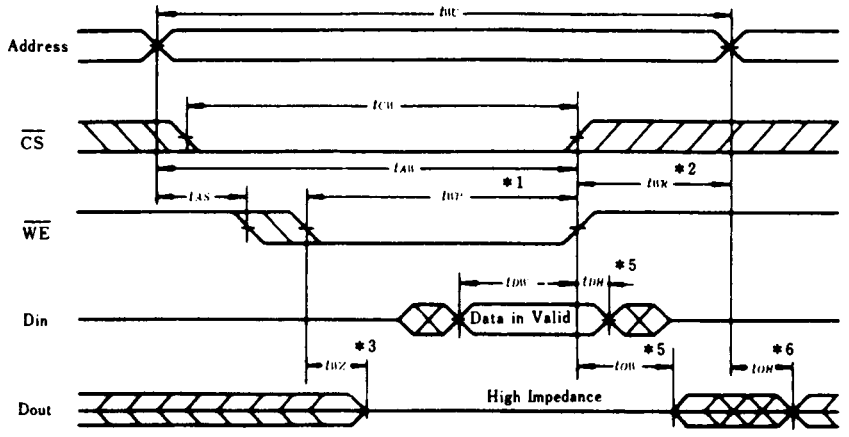
Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

● WRITE CYCLE

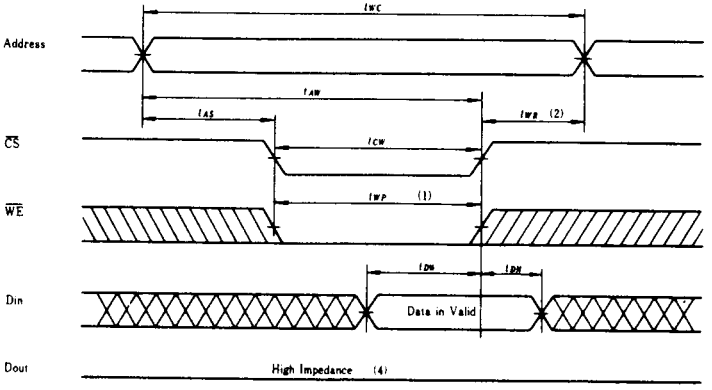
Parameter	Symbol	HM6268-25		HM6268-35		HM6268-45		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	25	—	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	35	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	12	—	20	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High Z	t_{WZ}*1	0	8	0	10	0	15	ns
Output Active from End of Write	t_{OW}*1	0	—	0	—	0	—	ns

Note) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

- Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



- Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

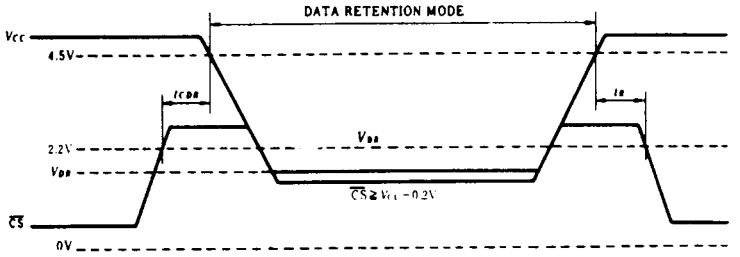
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leq Ta \leq 70°C$)

This characteristics guaranteed only for L-version.

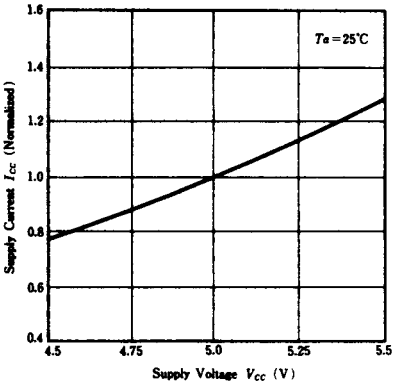
Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{in} \geq V_{CC} - 0.2V$ or $0V \leq V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30 *2 20 *3	μA
Chip Deselect to Data Retention Time	t_{CDR}	See retention waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

Notes) *1. t_{RC} = Read Cycle Time. *2. $V_{CC} = 3.0V$ *3. $V_{CC} = 2.0V$

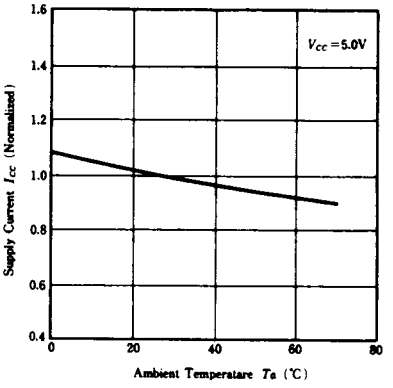
●LOW V_{CC} DATA RETENTION WAVEFORM



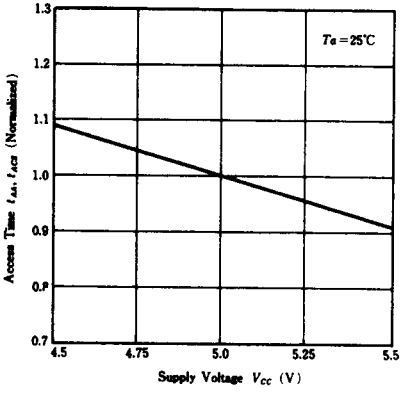
SUPPLY CURRENT VS. SUPPLY VOLTAGE



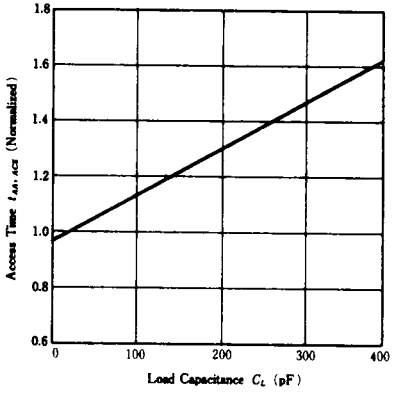
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



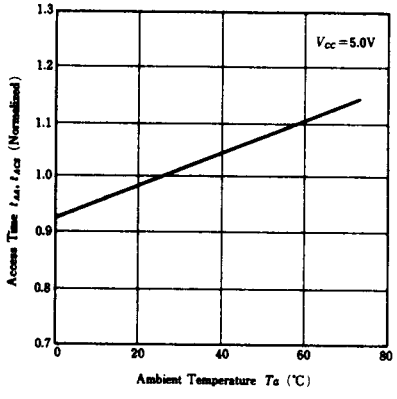
ACCESS TIME VS. SUPPLY VOLTAGE



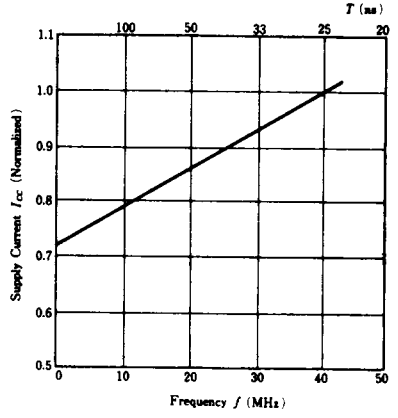
ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. AMBIENT TEMPERATURE

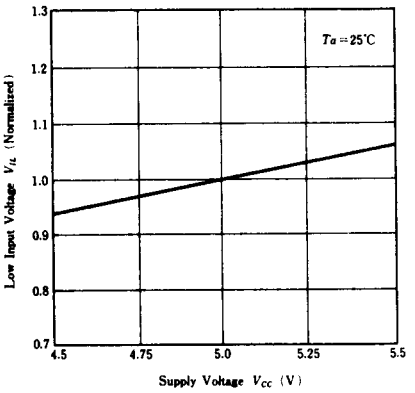


SUPPLY CURRENT VS. FREQUENCY

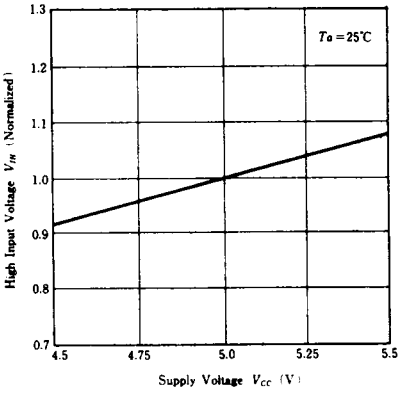


2

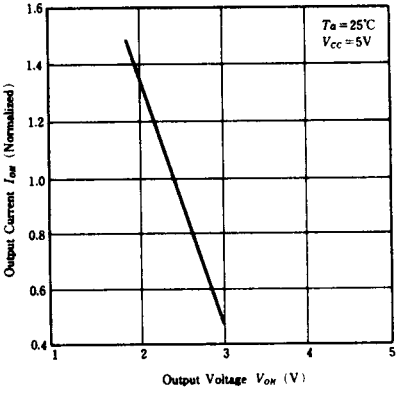
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



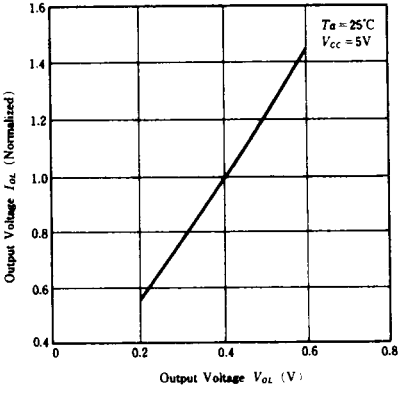
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



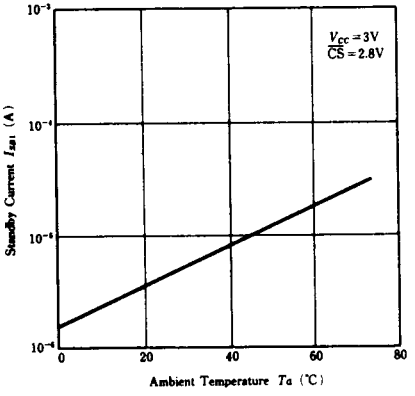
OUTPUT CURRENT VS. OUTPUT VOLTAGE



OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE