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# HM62832H Series

32768-word × 8-bit High Speed CMOS Static RAM

# HITACHI

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## Features

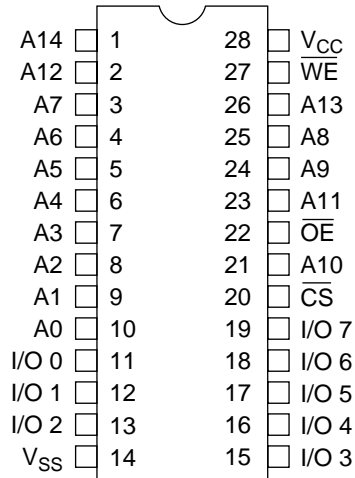
- High speed: Fast access time 25/35/45 ns (max)
- Low power  
Active: 300 mW (typ)  
Standby: 10  $\mu$ W (typ) (L-version)
- Single 5 V supply
- Completely static memory  
No clock or timing strobe required
- Equal access and cycle times
- Common data input and output – Three state output
- Directly TTL compatible – All inputs and outputs

## Ordering Information

Type No.	Access Time	Package
HM62832HP-25	25 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62832HP-35	35 ns	
HM62832HP-45	45 ns	
HM62832HLP-25	25 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM62832HLP-35	35 ns	
HM62832HLP-45	45 ns	
HM62832HJP-25	25 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM62832HJP-35	35 ns	
HM62832HJP-45	45 ns	
HM62832HLJP-25	25 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM62832HLJP-35	35 ns	
HM62832HLJP-45	45 ns	

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## Pin Arrangement

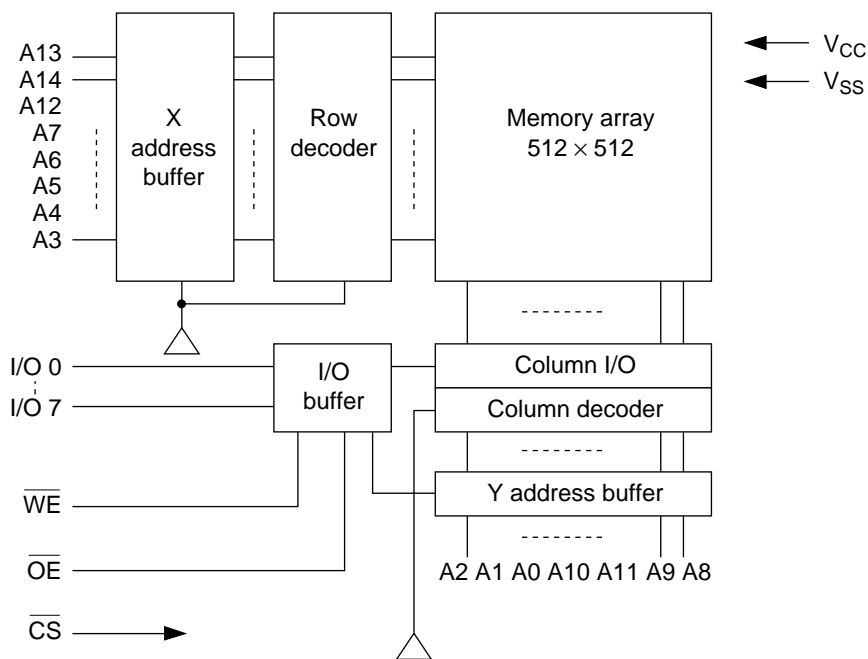


(Top view)

## Pin Description

Pin Name	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
$V_{CC}$	Power supply
$V_{SS}$	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_T$	-0.5 <sup>1)</sup> to +7.0	V
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +125	°C
Storage temperature under bias	$T_{bias}$	-10 to +85	°C

Note: 1. -2.5 V for pulse width  $\leq$  10 ns

Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	$V_{CC}$ Current	I/O Pin	Ref. Cycle
H	X	X	Not selected	$I_{SB}, I_{SB1}$	High-Z	
L	L	H	Read	$I_{CC}$	Dout	Read cycle (1) to (3)
L	H	L	Write	$I_{CC}$	Din	Write cycle (1)
L	L	L		$I_{CC}$	Din	Write cycle (2)

Note: X: H or L

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## Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
	V <sub>SS</sub>	0	0	0	V
Input voltage	V <sub>IH</sub>	2.2	—	6.0	V
	V <sub>IL</sub>	-0.5 <sup>*1</sup>	—	0.8	V

Note: 1. -2.0 V for pulse width ≤ 10 ns

## DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Min	Typ <sup>*1</sup>	Max	Unit	Test Conditions	Note
Input leakage current	I <sub>LI</sub>	—	—	2	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Output leakage current	I <sub>LO</sub>	—	—	2	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>	
Operating power supply current	I <sub>CC</sub>	—	60	120	mA	Min cycle, duty = 100%, CS = V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA	
Standby power supply current	I <sub>SB</sub>	—	15	30	mA	$\overline{CS} = V_{IH}$	
Standby power supply current	I <sub>SB1</sub>	—	0.02	2	mA	$\overline{CS} \geq V_{CC} - 0.2$ V 0 V ≤ V <sub>in</sub> ≤ 0.2 V or V <sub>in</sub> ≥ V <sub>CC</sub> - 0.2 V	
							—
Output voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 8 mA	
	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -4 mA	

Note: 1. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and not guaranteed.

## Capacitance (Ta = 25°C, f = 1.0 MHz)<sup>\*1</sup>

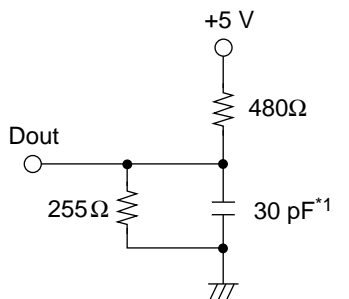
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C <sub>in</sub>	—	—	6	pF	V <sub>in</sub> = 0 V
Input/output capacitance	C <sub>I/O</sub>	—	—	10	pF	V <sub>I/O</sub> = 0 V

Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, unless otherwise noted.)

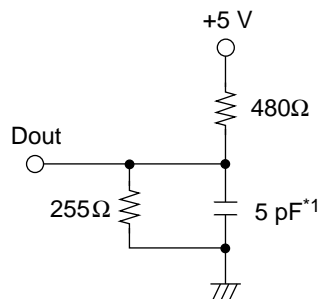
### Test Conditions

- Input pulse levels: 0.0 V to 3.0 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



Output load (A)

Note: 1. Including scope and jig



Output load (B)

(for t<sub>CLZ</sub>, t<sub>OLZ</sub>, t<sub>CHZ</sub>, t<sub>OHZ</sub>, t<sub>WHZ</sub> and t<sub>OW</sub>)

### Read Cycle

Parameter	Symbol	HM62832H-25		HM62832H-35		HM62832H-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Read cycle time	t <sub>RC</sub>	25	—	35	—	45	—	ns	
Address access time	t <sub>AA</sub>	—	25	—	35	—	45	ns	
Chip select access time	t <sub>ACS</sub>	—	25	—	35	—	45	ns	
Output enable to output valid	t <sub>OE</sub>	—	12	—	15	—	20	ns	
Output hold from address change	t <sub>OH</sub>	5	—	5	—	5	—	ns	6
Chip selection to output in low-Z	t <sub>CLZ</sub>	5	—	5	—	5	—	ns	1
Output enable to output in low-Z	t <sub>OLZ</sub>	0	—	0	—	0	—	ns	1
Chip deselection to output in high-Z	t <sub>CHZ</sub>	0	12	0	15	0	20	ns	1
Output enable to output in high-Z	t <sub>OHZ</sub>	0	12	0	15	0	20	ns	1

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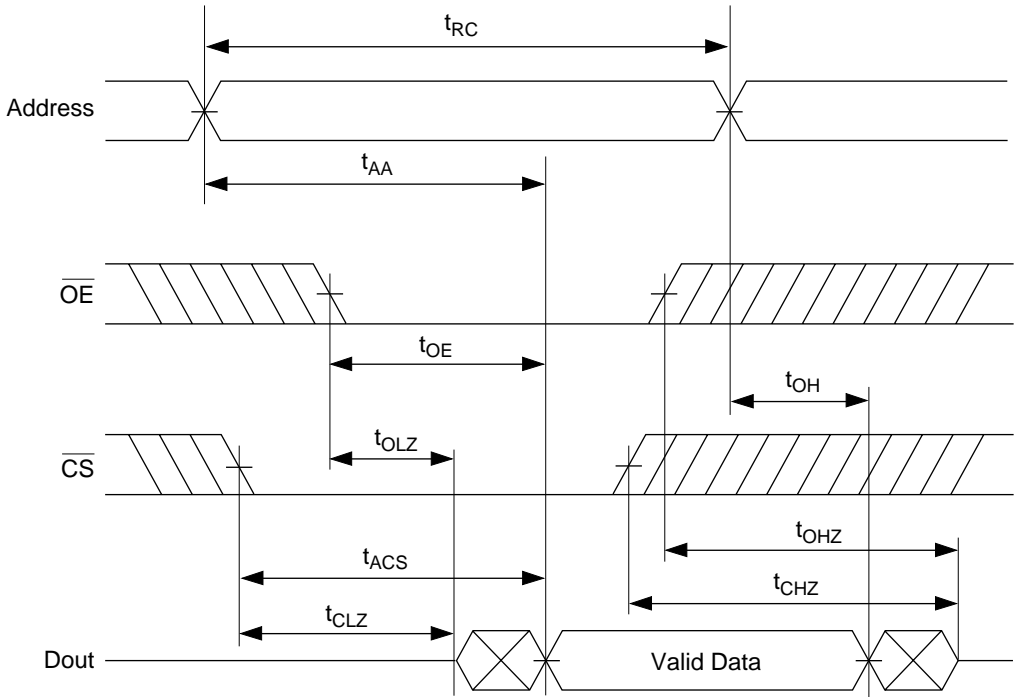
## Write Cycle

Parameter	Symbol	HM62832H-25		HM62832H-35		HM62832H-45		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write cycle time	$t_{WC}$	25	—	35	—	45	—	ns	
Chip selection to end of write	$t_{CW}$	15	—	20	—	25	—	ns	
Address valid to end of write	$t_{AW}$	20	—	30	—	40	—	ns	
Address setup time	$t_{AS}$	0	—	0	—	0	—	ns	
Write pulse width	$t_{WP}$	15	—	20	—	25	—	ns	3
Write recovery time	$t_{WR}$	0	—	0	—	0	—	ns	4
Write to output in high-Z	$t_{WHZ}$	0	12	0	15	0	20	ns	2, 5
Data to write time overlap	$t_{DW}$	12	—	15	—	20	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	0	—	ns	
Output disable to output in high-Z	$t_{OHZ}$	0	12	0	15	0	20	ns	2, 5
Output active from end of write	$t_{OW}$	5	—	5	—	5	—	ns	2, 7

- Notes:
1. Transition is measured  $\pm 200$  mV from steady state voltage with load (B). This parameter is sampled and not 100% tested.
  2. Transition is measured  $\pm 200$  mV from high impedance voltage with load (B). This parameter is sampled and not 100% tested.
  3. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}$  and a low  $\overline{WE}$ .
  4.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going high to the end of write cycle.
  5. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.
  6. Dout is in the same phase of written data of this write cycle.
  7. If  $\overline{CS}$  is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O pins.

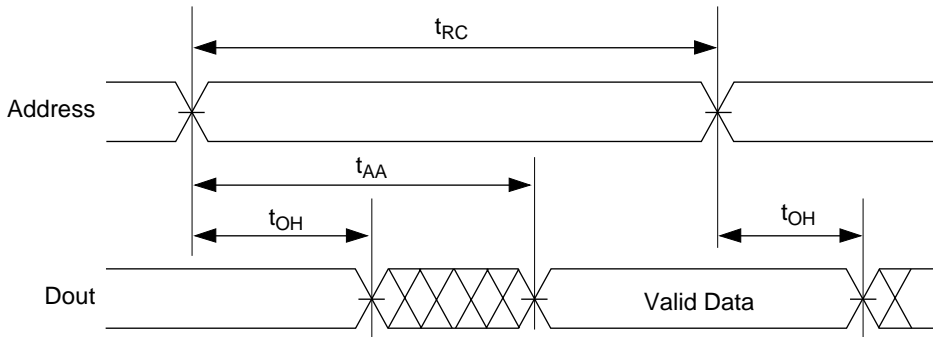
Timing Waveforms

Read Cycle Timing-1\*1 ( $\overline{WE} = V_{IH}$ )



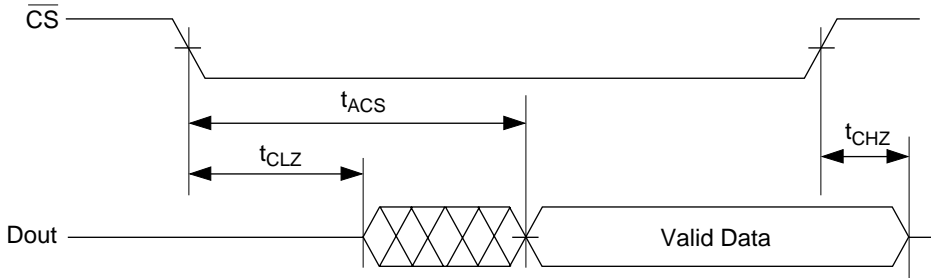
Note: 1. Transition is measured  $\pm 200$  mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Read Cycle Timing-2 ( $\overline{WE} = V_{IH}, \overline{CS} = V_{IL}, \overline{OE} = V_{IL}$ )



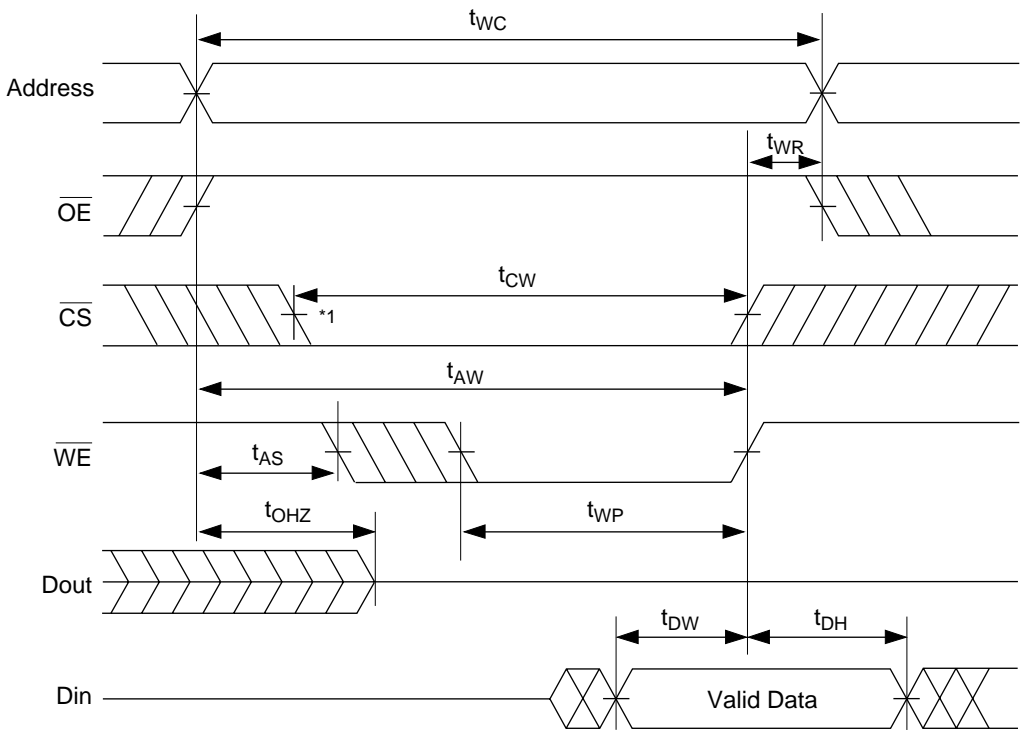
# HM62832H Series

## Read Cycle Timing-3\*1 ( $\overline{WE} = V_{IH}, \overline{OE} = V_{IL}$ )



- Notes: 1. Transition is measured  $\pm 200$  mV from steady state voltage with load (B).  
 This parameter is sampled and not 100% tested.  
 2. Address should be valid prior to or coincident with  $\overline{CS}$  transition low.

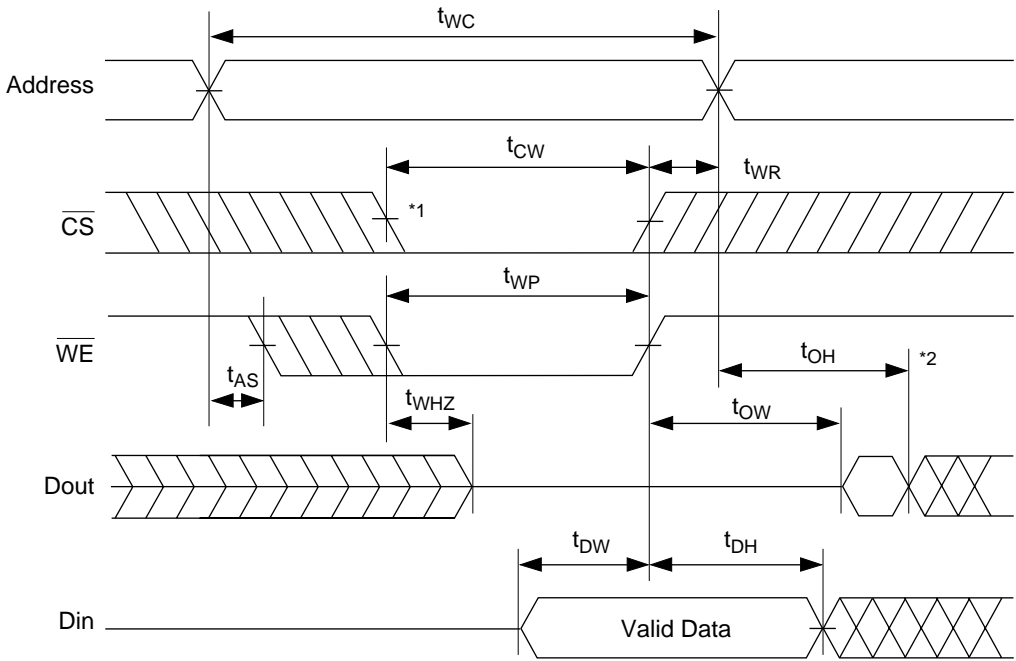
## Write Cycle Timing-1\*2



- Notes: 1. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  low transition, outputs remain in a high impedance state.  
 2.  $\overline{WE}$  must be high during all address transitions except when device is deselected with  $\overline{CS}$ .



**Write Cycle Timing-2<sup>\*3</sup> ( $\overline{OE}$  Low Fixed)**



- Notes: 1. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  low transition, outputs remain in a high impedance state.  
 2. Dout is the read data of next address.  
 3.  $\overline{WE}$  must be high during all address transitions except when device is deselected with  $\overline{CS}$ .

# HM62832H Series

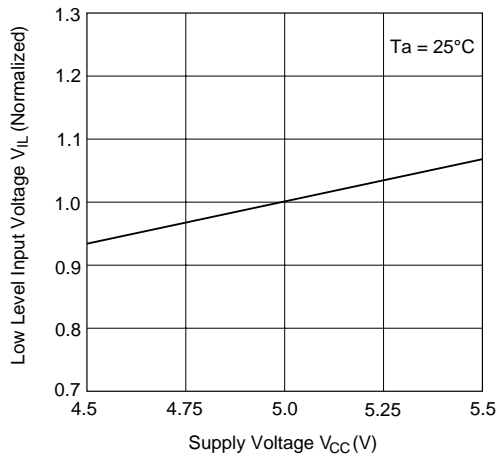
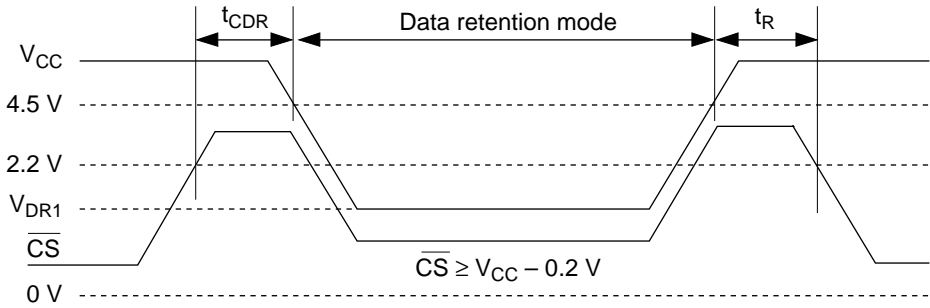
## Low $V_{CC}$ Data Retention Characteristics ( $T_a = 0$ to $+70^\circ\text{C}$ )

This characteristics is guaranteed only for L-version.

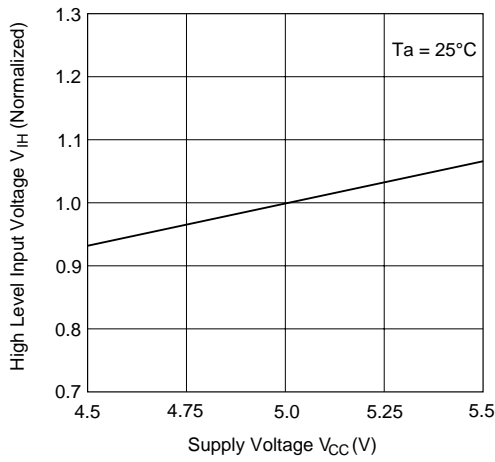
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ , $V_{in} \geq V_{CC} - 0.2 \text{ V}$ or $0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$
Data retention current	$I_{CCDR}$	—	1	$50^{-1}$	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	
Operation recovery time	$t_R$	5	—	—	ms	

Note: 1.  $V_{CC} = 3.0 \text{ V}$

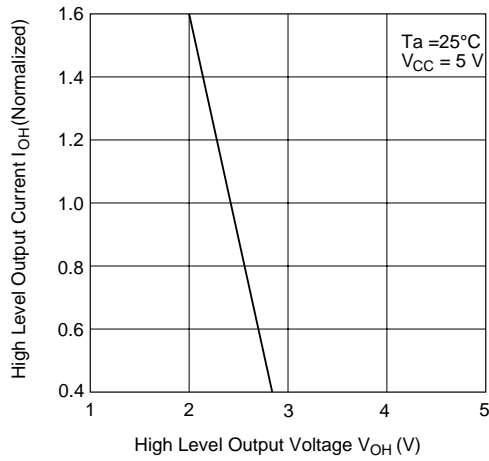
## Low $V_{CC}$ Data Retention Timing Waveform



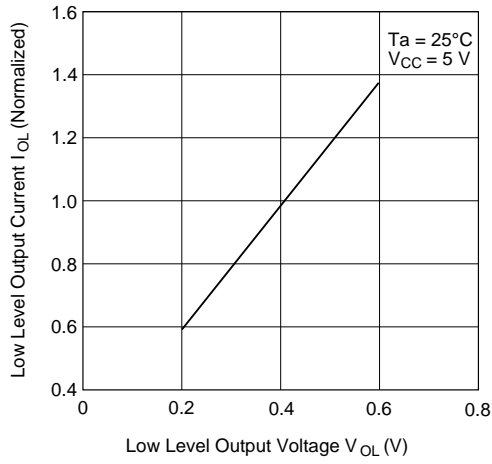
Low Level Input Voltage vs. Supply Voltage



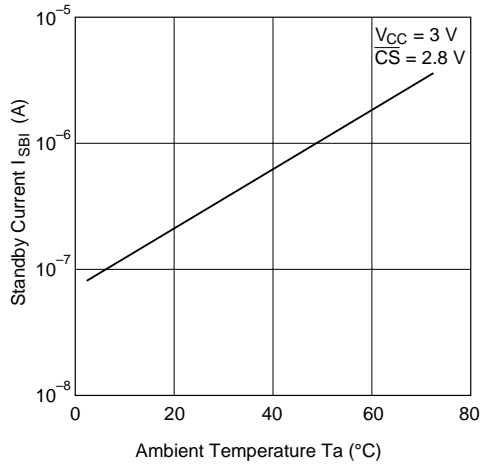
**High Level Input Voltage vs. Supply Voltage**



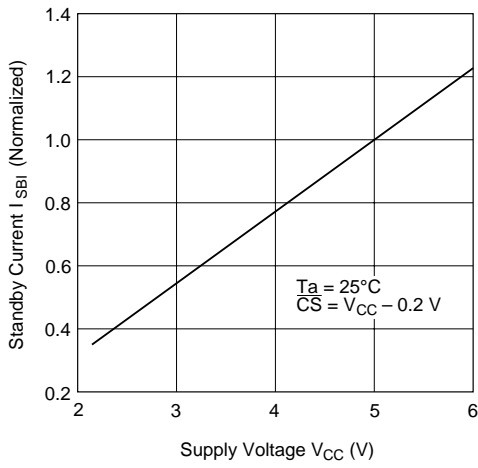
**High Level Output Current vs. High Level Output Voltage**



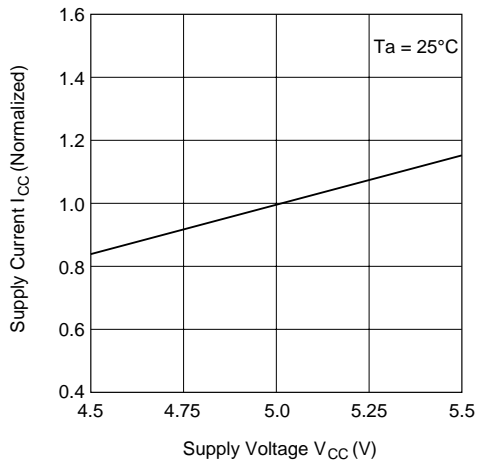
**Low Level Output Current vs. Low Level Output Voltage**



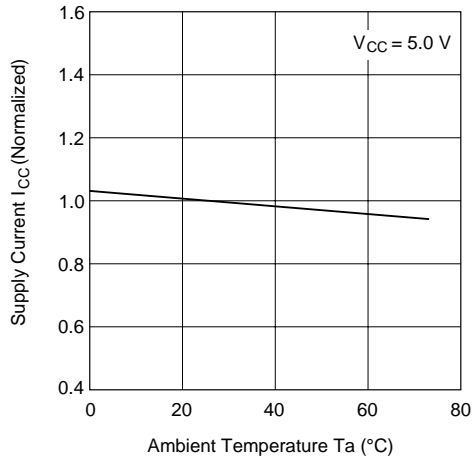
**Standby Current vs. Ambient Temperature**



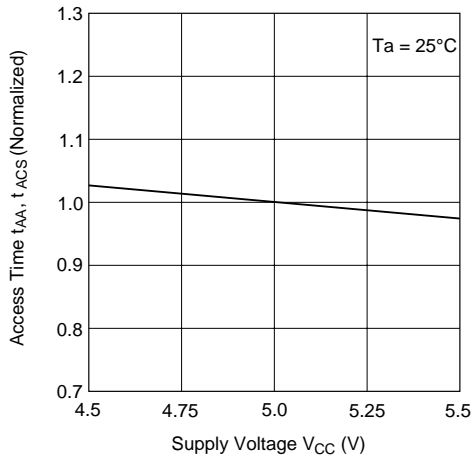
Standby Current vs. Supply Voltage



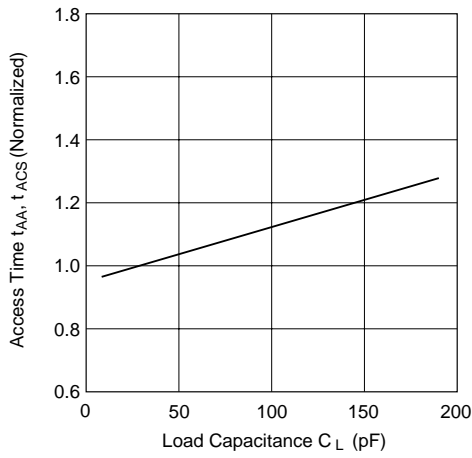
Supply Current vs. Supply Voltage



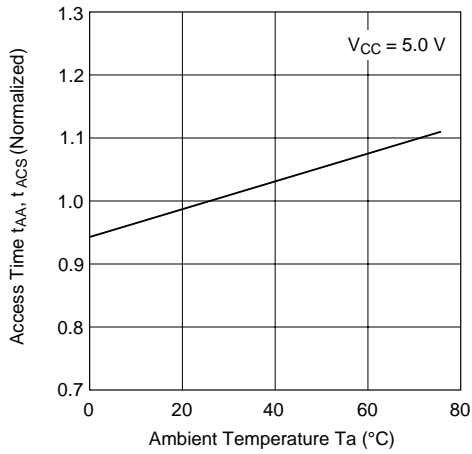
**Supply Current vs. Ambient Temperature**



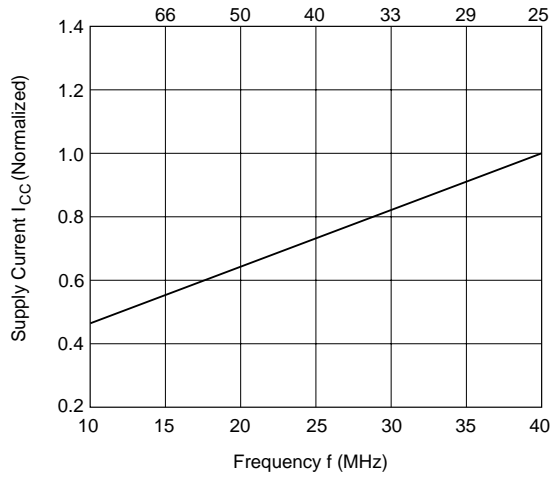
**Access Time vs. Supply Voltage**



Access Time vs. Load Capacitance



Access Time vs. Ambient Temperature



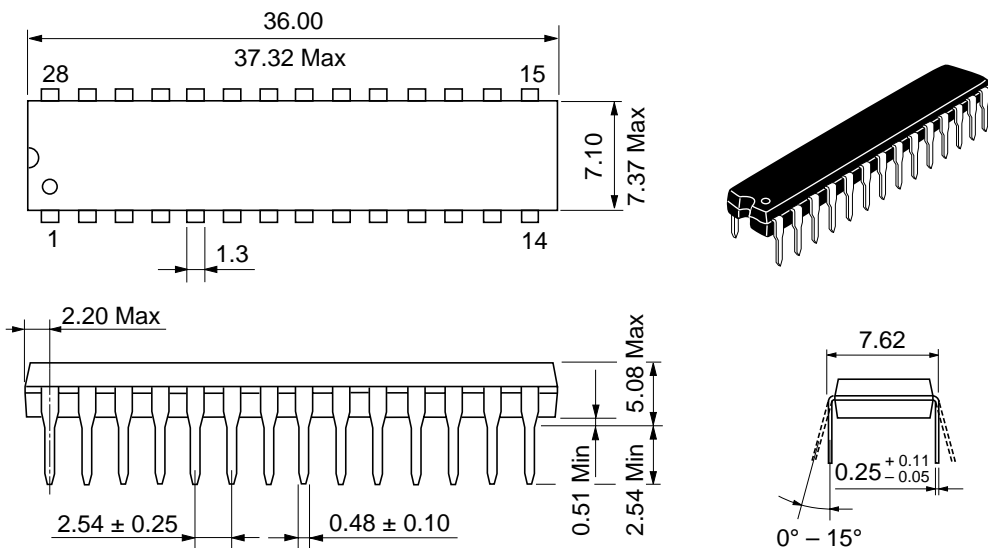
**Supply Current vs. Frequency**



Package Dimensions

HM62832HP/HLP Series (DP-28NA)

Unit: mm



HM62832HJP/HLJP Series (CP-28DN)

Unit: mm

