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# HM6288 Series

16384-word  $\times$  4-bit High Speed CMOS Static RAM

# HITACHI

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## Description

The Hitachi HM6288 is a high speed 64k static RAM organized as 16-kword  $\times$  4-bit. It realizes high speed access time (25/35 ns) and low power consumption, using CMOS process technology. It is most advantageous for the field where high speed and high density memory is required, such as cache memory for mainframes or 32-bit MPUs. The HM6288, packaged in a 300-mil plastic DIP and SOJ, is available for high density mounting. A low power version retains data with battery backup.

## Features

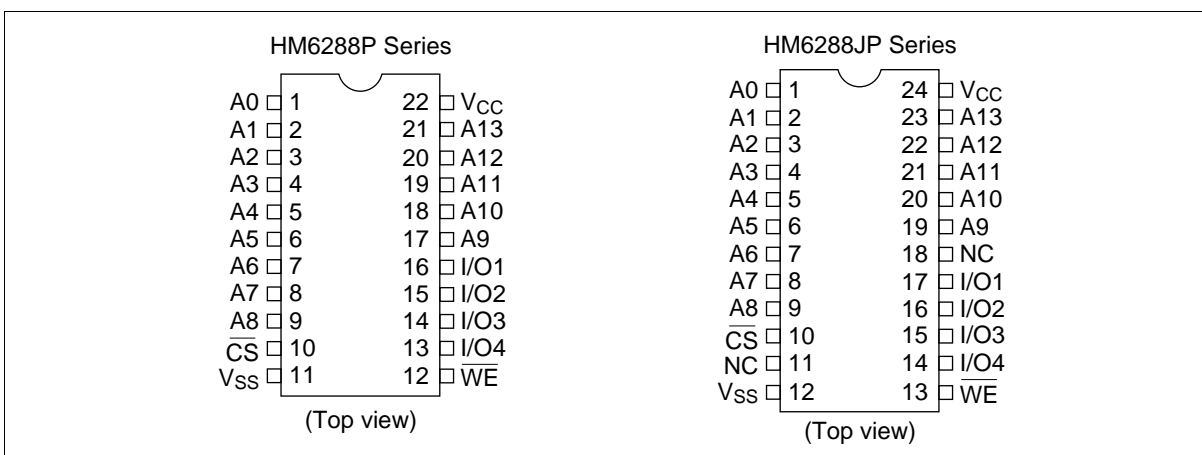
- Single 5 V supply and high density plastic package
- High speed: fast access time 25/35 ns (max)
- Low power dissipation:
  - Active mode 300 mW (typ)
  - Standby mode 100  $\mu$ W (typ)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times.
- Directly TTL compatible all inputs and outputs

## HM6288 Series

### Ordering Information

Type No.	Access Time	Package
HM6288P-25	25 ns	300-mil, 22-pin plastic DIP (DP-22NB)
HM6288P-35	35 ns	
HM6288LP-25	25 ns	300-mil, 24-pin SOJ (CP-24D)
HM6288LP-35	35 ns	
HM6288JP25	25 ns	300-mil, 24-pin SOJ (CP-24D)
HM6288JP-35	35 ns	
HM6288LJP-25	25 ns	
HM6288LJP-35	35 ns	

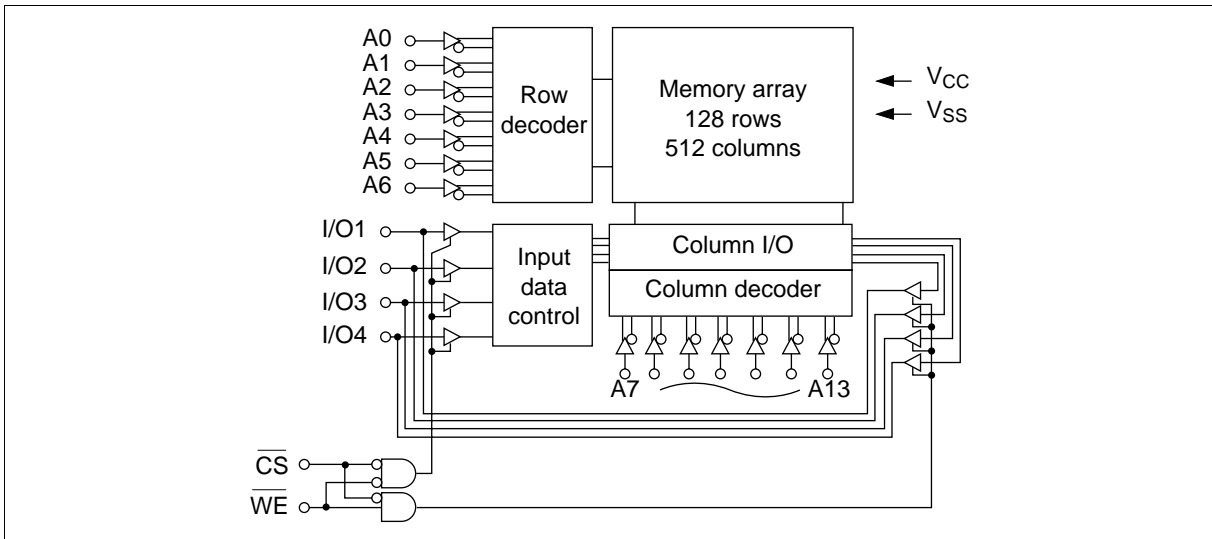
### Pin Arrangement



### Pin Description

Pin Name	Function
A0–A13	Address
I/O1–I/O4	Input/output
$\overline{\text{CS}}$	Chip select
$\overline{\text{WE}}$	Write enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground

**Block Diagram**



**Truth Table**

$\overline{\text{CS}}$	$\overline{\text{WE}}$	Mode	$V_{\text{CC}}$ Current	I/O Pin	Ref. Cycle
H	×	Standby	$I_{\text{SB}}, I_{\text{SB1}}$	High-Z	—
L	H	Read	$I_{\text{CC}}$	Dout	Read cycle 1, 2
L	L	Write	$I_{\text{CC}}$	Din	Write cycle 1, 2

Note: ×: Don't care.

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{\text{SS}}$	$V_{\text{T}}$	-0.5 to +7.0	V
Power dissipation	$P_{\text{T}}$	1.0	W
Operating temperature	$T_{\text{opr}}$	0 to +70	°C
Storage temperature	$T_{\text{stg}}$	-55 to +125	°C
Temperature under bias	$T_{\text{bias}}$	-10 to +85	°C

Note:  $V_{\text{T}}$  min.: -2.0 V for pulse width  $\leq 10$  ns

## HM6288 Series

### Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
	V <sub>SS</sub>	0	0	0	V
Input high (logic 1) voltage	V <sub>IH</sub>	2.2	—	6.0	V
Input low (logic 0) voltage	V <sub>IL</sub>	-0.5 <sup>*1</sup>	—	0.8	V

Note: 1. V<sub>IL</sub> min.: -2.0 V for pulse width ≤ 10 ns

### DC Characteristics (Ta = 0 to +70°C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Min	Typ <sup>*1</sup>	Max	Unit	Test conditions
Input leakage current	I <sub>LI</sub>	—	—	2.0	μA	V <sub>CC</sub> = Max, Vin = V <sub>SS</sub> to V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>	—	—	2.0	μA	$\overline{CS} = V_{IH}$ , V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Operating power supply current	I <sub>CC</sub>	—	60	120	mA	$\overline{CS} = V_{IL}$ , I <sub>I/O</sub> = 0 mA, min. cycle
Standby V <sub>CC</sub> current	I <sub>SB</sub>	—	15	30	mA	$\overline{CS} = V_{IH}$ , min. cycle
Standby V <sub>CC</sub> current 1	I <sub>SB1</sub>	—	0.02	2.0	mA	$\overline{CS} \geq V_{CC} - 0.2V$ , 0 V ≤ Vin ≤ 0.2V or V <sub>CC</sub> - 0.2V ≤ Vin
	I <sub>SB1</sub> <sup>*2</sup>	—	0.02	0.1	mA	
Output low voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 8 mA
Output high voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -4.0 mA

Notes: 1. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and not guaranteed.

2. L-version

### Capacitance (Ta = 25°C, f = 1.0 MHz)<sup>\*1</sup>

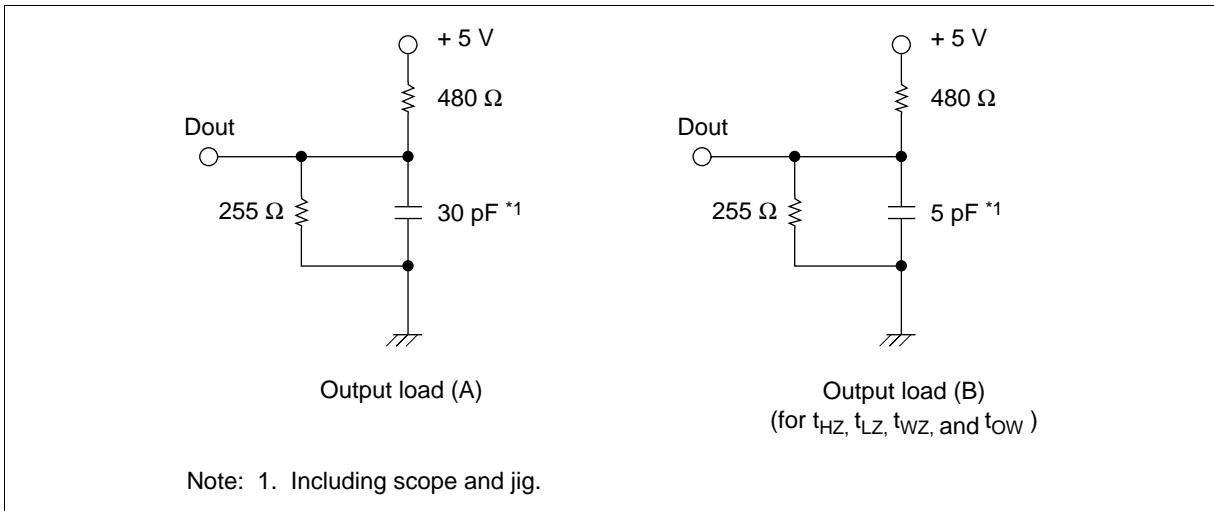
Parameter	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	C <sub>in</sub>	—	6	pF	V <sub>in</sub> = 0 V
Input/output capacitance	C <sub>I/O</sub>	—	8	pF	V <sub>I/O</sub> = 0 V

Note: 1. This parameter is sampled and not 100% tested.

**AC Characteristics**

**Test Conditions**

- Input pulse levels: 0 V to 3.0 V
- Input and output timing reference levels: 1.5 V
- Input rise and fall time: 5 ns
- Output load: See figure



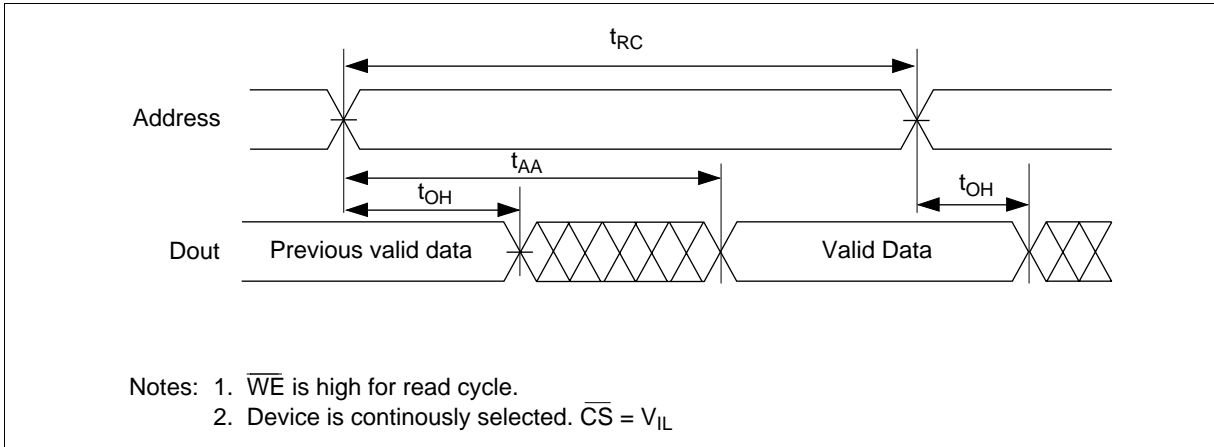
**Read Cycle**

Parameter	Symbol	HM6288-25		HM6288-35		Unit
		Min	Max	Min	Max	
Read cycle time	$t_{RC}$	25	—	35	—	ns
Address access time	$t_{AA}$	—	25	—	35	ns
Chip select access time	$t_{ACS}$	—	25	—	35	ns
Output hold from address change	$t_{OH}$	3	—	5	—	ns
Chip selection to output in low-Z	$t_{LZ}^{-1}$	5	—	5	—	ns
Chip deselection to output in high-Z	$t_{HZ}^{-1}$	0	12	0	20	ns
Chip selection to power up time	$t_{PU}$	0	—	0	—	ns
Chip deselection to power down time	$t_{PD}$	—	25	—	30	ns

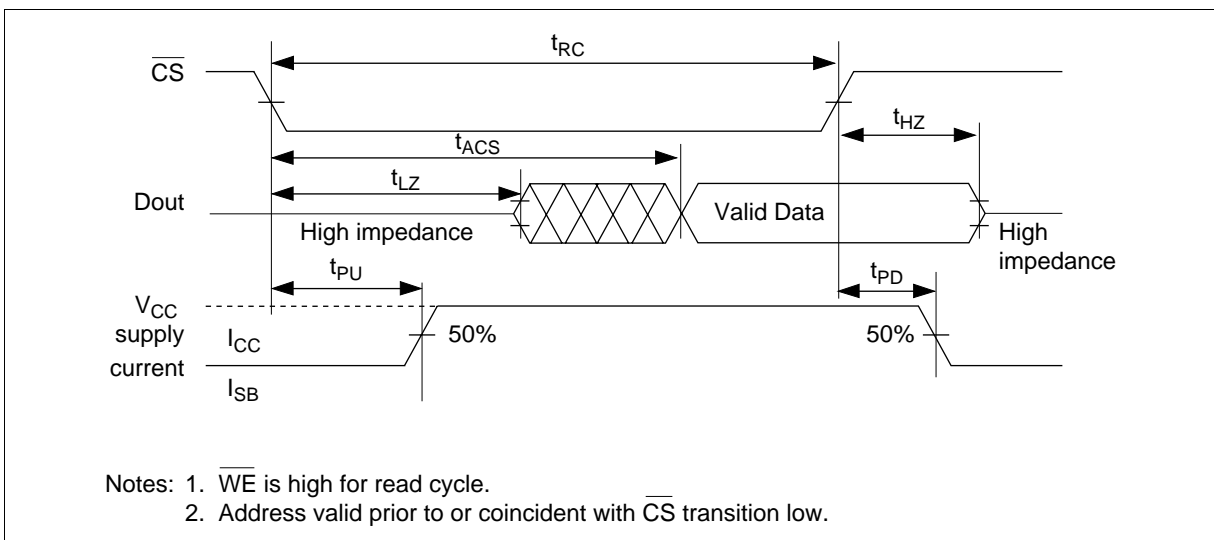
Note: 1. Transition is measured  $\pm 200$  mV from steady state voltage with load (B).  
 These parameters are sampled and not 100% tested.

## HM6288 Series

### Read Timing Waveform (1)



### Read Timing Waveform (2)



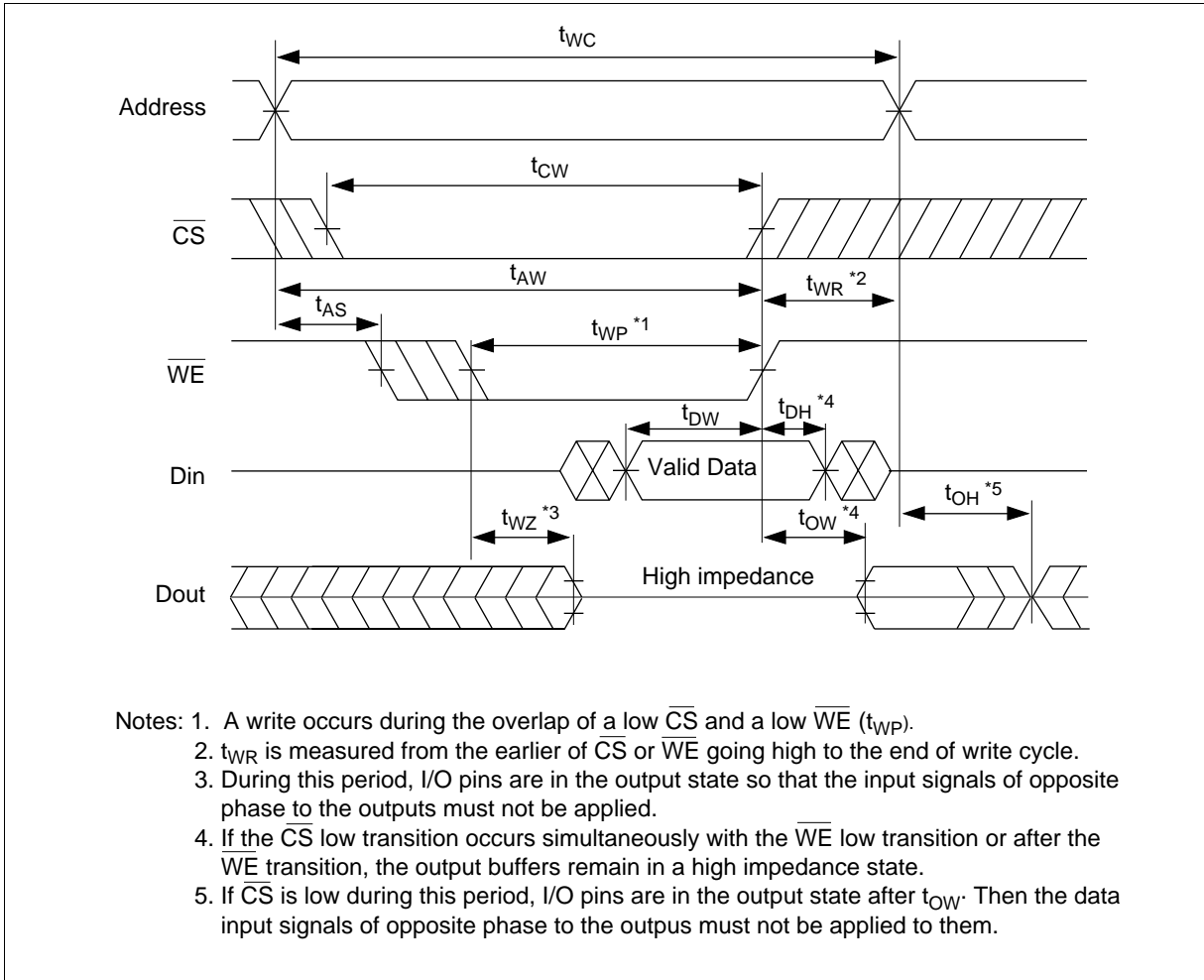
**Write Cycle**

Parameter	Symbol	HM6288-25		HM6288-35		Unit
		Min	Max	Min	Max	
Write cycle time	$t_{WC}$	25	—	35	—	ns
Chip selection to end of write	$t_{CW}$	20	—	30	—	ns
Address valid to end of write	$t_{AW}$	20	—	30	—	ns
Address setup time	$t_{AS}$	0	—	0	—	ns
Write pulse width	$t_{WP}$	20	—	30	—	ns
Write recovery time	$t_{WR}$	0	—	0	—	ns
Date valid to end of write	$t_{DW}$	12	—	20	—	ns
Data hold time	$t_{DH}$	0	—	0	—	ns
Write enabled to output in high-Z	$t_{WZ}^{*1}$	0	8	0	10	ns
Output active from end of write	$t_{OW}^{*1}$	5	—	5	—	ns

Note: 1. Transition is measured  $\pm 200$  mV from steady state voltage with load (B).  
 These parameters are sampled and not 100% tested.

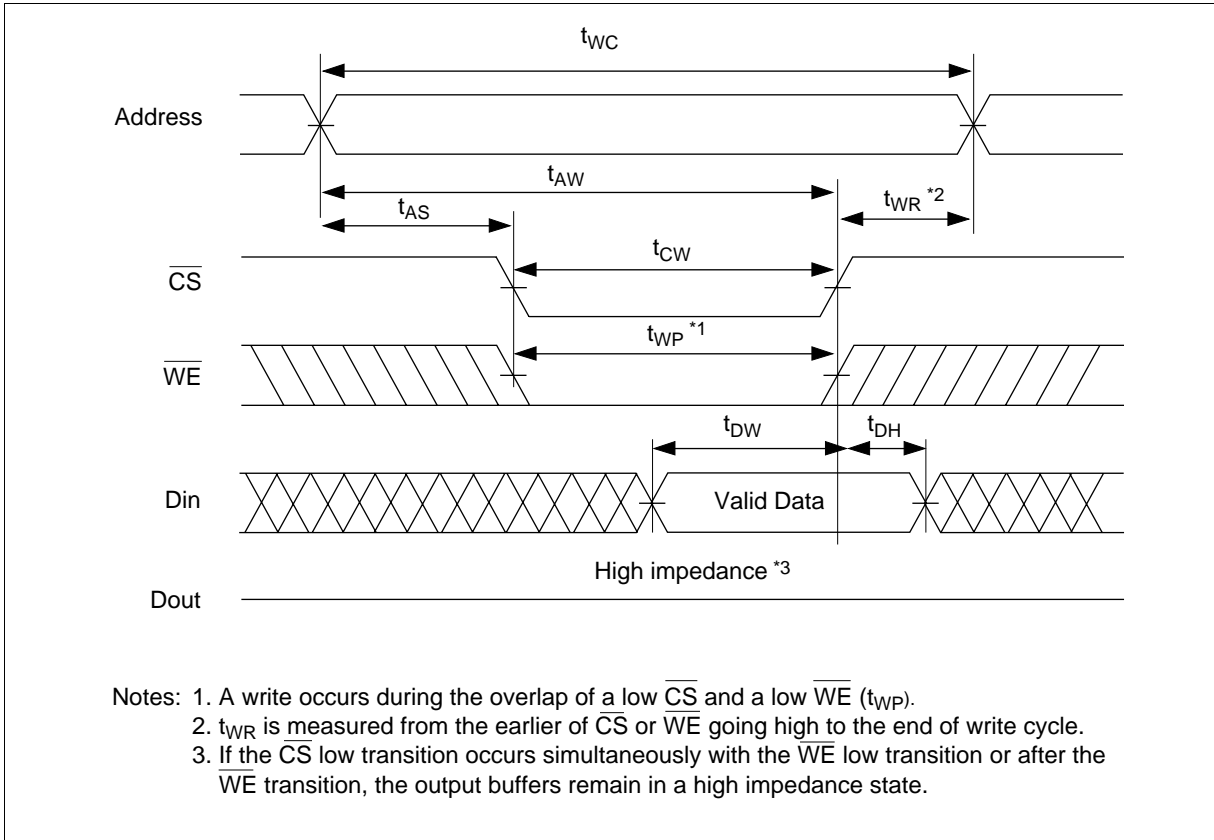
## HM6288 Series

### Write Timing Waveform (1) ( $\overline{WE}$ Controlled)





Write Timing Waveform (2) ( $\overline{CS}$  Controlled)



## HM6288 Series

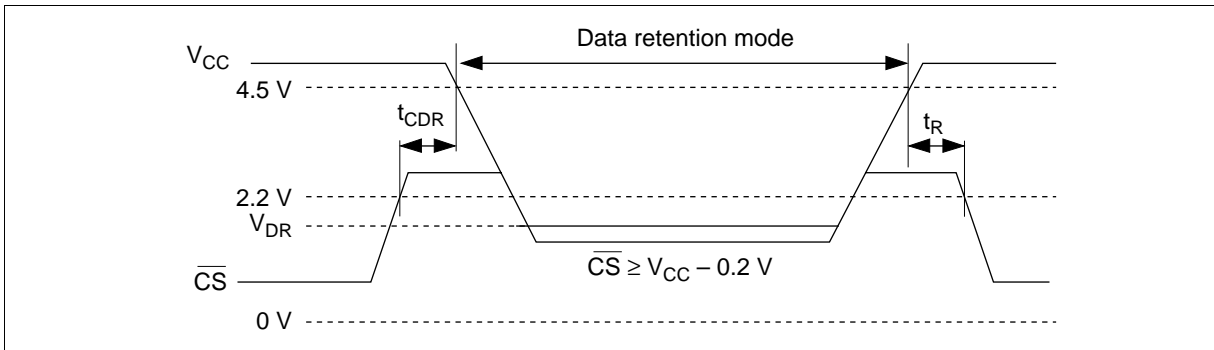
### Low $V_{CC}$ Data Retention Characteristics ( $T_a = 0$ to $+70^\circ\text{C}$ )

Data retention characteristics are guaranteed only for L version.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, $V_{in} \geq V_{CC} - 0.2$ V or $0$ V $\leq V_{in} \leq 0.2$ V
Data retention current	$I_{CCDR}$	—	—	$50^{+2}$	$\mu\text{A}$	
		—	—	$35^{-3}$	$\mu\text{A}$	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	$t_{RC}^{*1}$	—	—	ns	

- Notes: 1.  $t_{RC}$  = read cycle time  
 2.  $V_{CC} = 3.0$  V  
 3.  $V_{CC} = 2.0$  V

### Low $V_{CC}$ Data Retention Waveform

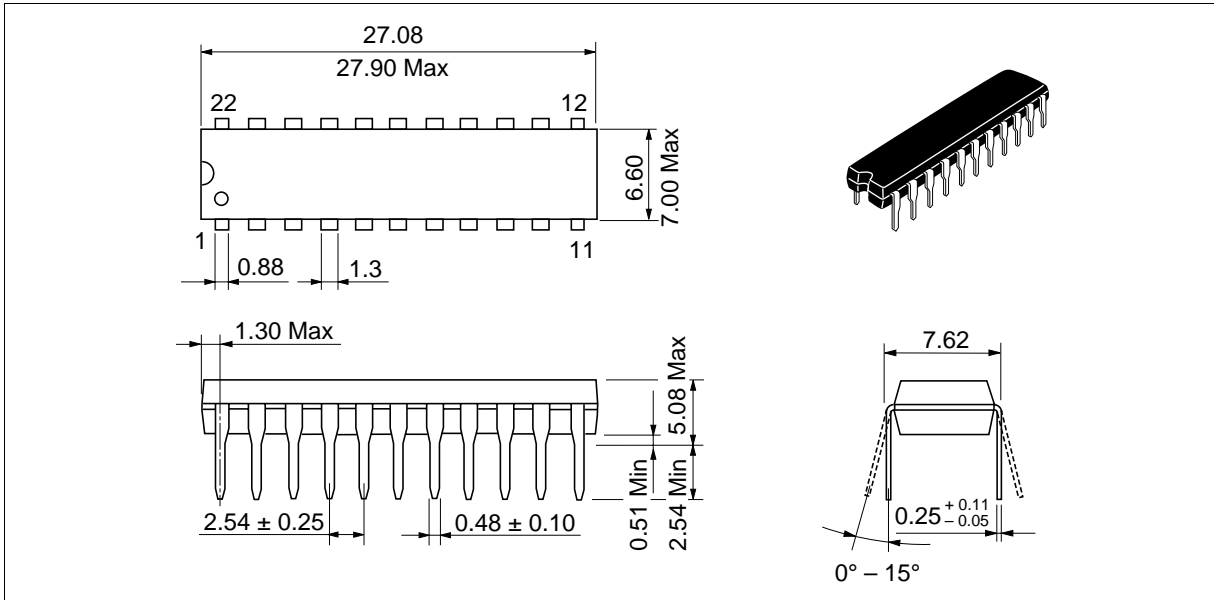


## HM6288 Series

### Package Dimensions

HM6288P/LP Series (DP-22NB)

Unit: mm



HM6288JP/LJP Series (CP-24D)

Unit: mm

