

65536-Word × 4-Bit High Speed Static RAM (with  $\overline{OE}$ )

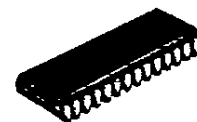
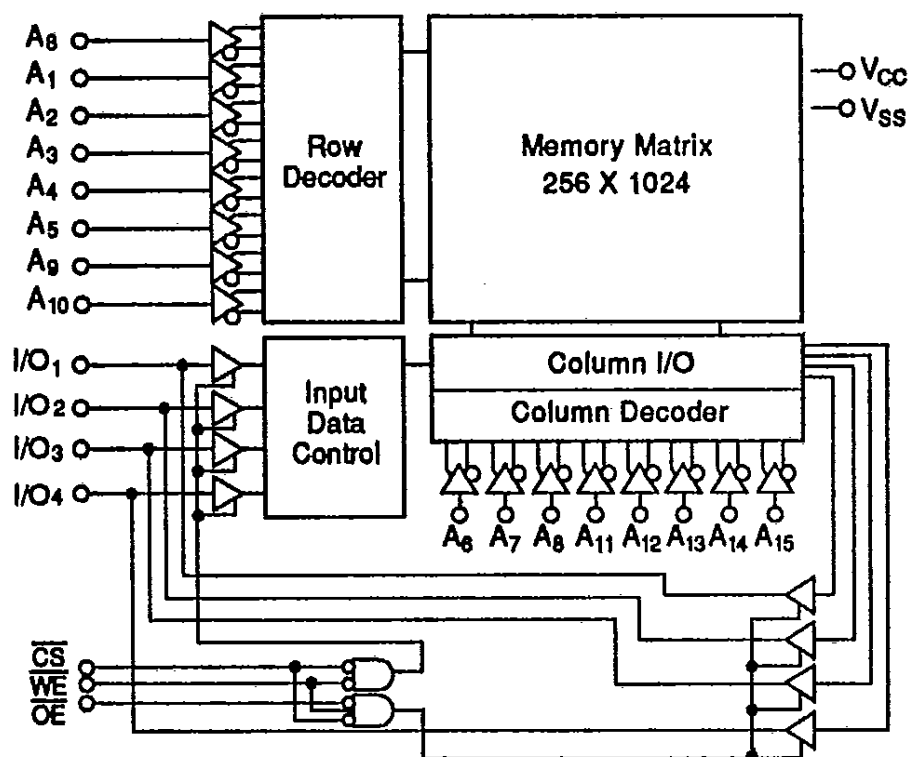
## ■ FEATURES

- Super Fast  
Access Time ..... 20/25ns (max.)
- Fast  $\overline{OE}$   
Access Time ..... 10ns (max.)
- Low Power Dissipation ..... 350mW (typ.)
- +5V Single Supply
- Completely Static Memory  
No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output
- 300 mil 28 pin SOJ

## ■ ORDERING INFORMATION

| Type No.    | Access Time | Package                                    |
|-------------|-------------|--------------------------------------------|
| HM6709JP-20 | 20ns        | 300 mil 28 pin<br>Plastic SOJ<br>(CP-28DN) |
| HM6709JP-25 | 25ns        |                                            |

## ■ BLOCK DIAGRAM



(CP-28DN)

## ■ PIN ARRANGEMENT

|                 |    |    |                 |
|-----------------|----|----|-----------------|
| NC              | 1  | 28 | VCC             |
| A0              | 2  | 27 | A15             |
| A1              | 3  | 26 | A14             |
| A2              | 4  | 25 | A13             |
| A3              | 5  | 24 | A12             |
| A4              | 6  | 23 | A11             |
| A5              | 7  | 22 | A10             |
| A6              | 8  | 21 | NC              |
| A7              | 9  | 20 | NC              |
| A8              | 10 | 19 | I/O1            |
| A9              | 11 | 18 | I/O2            |
| $\overline{CS}$ | 12 | 17 | I/O3            |
| $\overline{OE}$ | 13 | 16 | I/O4            |
| VSS             | 14 | 15 | $\overline{WE}$ |

(Top View)

## ■ ABSOLUTE MAXIMUM RATINGS

| Item                                    | Symbol                 | Rating       | Unit |
|-----------------------------------------|------------------------|--------------|------|
| Terminal Voltage to V <sub>SS</sub> Pin | V <sub>T</sub>         | -0.5 to +7.0 | V    |
| Power Dissipation                       | P <sub>T</sub>         | 1.0          | W    |
| Operating Temperature Range             | T <sub>opr</sub>       | 0 to +70     | °C   |
| Storage Temperature Range (with bias)   | T <sub>stg(bias)</sub> | -10 to +85   | °C   |
| Storage Temperature Range               | T <sub>stg</sub>       | -55 to +125  | °C   |

■ RECOMMENDED DC OPERATING CONDITIONS (0°C ≤ T<sub>a</sub> ≤ 70°C)

| Item               | Symbol            | Min. | Typ. | Max. | Unit |
|--------------------|-------------------|------|------|------|------|
| Supply Voltage     | V <sub>CC</sub>   | 4.5  | 5.0  | 5.5  | V    |
|                    | V <sub>SS</sub>   | 0.0  | 0.0  | 0.0  | V    |
| Input High Voltage | V <sub>IH</sub>   | 2.2  | —    | 6.0  | V    |
| Input Low Voltage  | V <sub>IL</sub> * | -3.0 | —    | 0.8  | V    |

\*Pulse width: 20ns, DC: -0.5V

## ■ TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Mode            | V <sub>CC</sub> Current            | I/O Pin  | Ref. Cycle                  |
|-----------------|-----------------|-----------------|-----------------|------------------------------------|----------|-----------------------------|
| H               | H or L          | H or L          | Not Selected    | I <sub>SB</sub> , I <sub>SB1</sub> | High Z   | —                           |
| L               | H               | H               | Output Disabled | I <sub>CC</sub> , I <sub>CC1</sub> | High Z   | —                           |
| L               | L               | H               | Read            | I <sub>CC</sub> , I <sub>CC1</sub> | Data Out | Read Cycle (1) (2) (3)      |
| L               | H               | L               | Write           | I <sub>CC</sub> , I <sub>CC1</sub> | Data In  | Write Cycle (1) (2) (3) (4) |
| L               | L               | L               |                 | I <sub>CC</sub> , I <sub>CC1</sub> | Data In  | Write Cycle (5) (6)         |

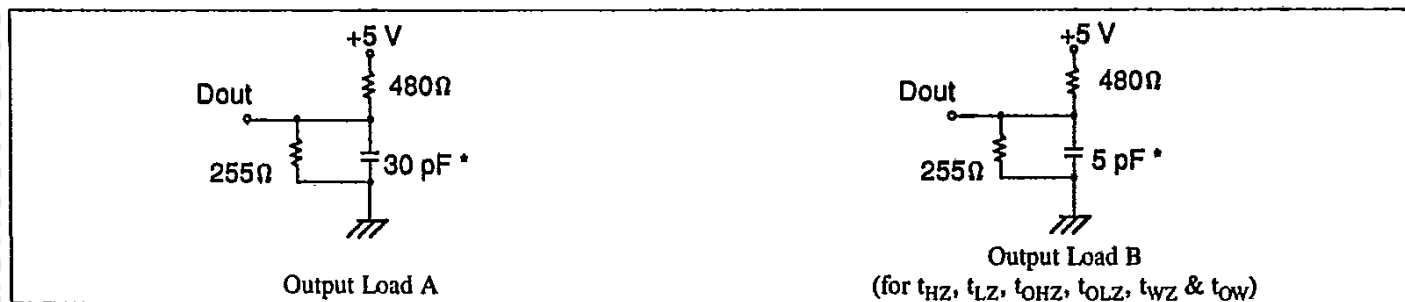
■ DC AND OPERATING CHARACTERISTICS (V<sub>CC</sub> = 5V ± 10%, T<sub>a</sub> = 0°C to 70°C)

| Item                           | Symbol           | Test Condition                                                                                                                           | Min. | Typ. | Max. | Unit |
|--------------------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| Input Leakage Current          | I <sub>LI</sub>  | V <sub>CC</sub> = 5.5V, V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>                                                             | —    | —    | 2    | μA   |
| Output Leakage Current         | I <sub>LO</sub>  | $\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ , $\overline{WE} = V_{IL}$<br>V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub> | —    | —    | 10   | μA   |
| Operating Power Supply Current | I <sub>CC</sub>  | $\overline{CS} = V_{IL}$ , I <sub>I/O</sub> = 0mA                                                                                        | —    | —    | 100  | mA   |
| Average Operating Current      | I <sub>CC1</sub> | Min. Cycle, Duty: 100%, I <sub>I/O</sub> = 0mA                                                                                           | —    | —    | 120  | mA   |
| Standby Power Supply Current   | I <sub>SB</sub>  | $\overline{CS} = V_{IH}$ , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                                          | —    | —    | 30   | mA   |
|                                | I <sub>SB1</sub> | $\overline{CS} \geq V_{CC} - 0.2V$<br>V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V                                 | —    | —    | 10   | mA   |
| Output Low Voltage             | V <sub>OL</sub>  | I <sub>OL</sub> = 8mA                                                                                                                    | —    | —    | 0.4  | V    |
| Output High Voltage            | V <sub>OH</sub>  | I <sub>OH</sub> = -4mA                                                                                                                   | 2.4  | —    | —    | V    |

## ■ AC TEST CONDITIONS

- Input Pulse Levels: V<sub>SS</sub> to 3.0V
- Input and Output Reference Levels: 1.5V

- Input Rise and Fall Time: 4ns
- Output Load: See Figure



\*Including scope and jig capacitance.

# ■ CAPACITANCE ( $T_a = 25^\circ\text{C}$ , $f = 1.0\text{MHz}$ )

| Item                     | Symbol    | Test Conditions       | Min. | Typ. | Max. | Unit |
|--------------------------|-----------|-----------------------|------|------|------|------|
| Input Capacitance        | $C_{IN}$  | $V_{IN} = 0\text{V}$  | —    | —    | 6    | pF   |
| Input/Output Capacitance | $C_{I/O}$ | $V_{I/O} = 0\text{V}$ | —    | —    | 10   | pF   |

**NOTE:** This parameter is sampled and not 100% tested.

# ■ AC CHARACTERISTICS ( $V_{CC} = 5\text{V} \pm 10\%$ , $T_a = 0^\circ\text{C}$ to $70^\circ\text{C}$ , unless otherwise noted.)

## • Read Cycle

| Item                                 | Symbol    | HM6709JP-20 |      | HM6709JP-25 |      | Unit | Notes |
|--------------------------------------|-----------|-------------|------|-------------|------|------|-------|
|                                      |           | Min.        | Max. | Min.        | Max. |      |       |
| Read Cycle Time                      | $t_{RC}$  | 20          | —    | 25          | —    | ns   | —     |
| Address Access Time                  | $t_{AA}$  | —           | 20   | —           | 25   | ns   | —     |
| Chip Select Access Time              | $t_{ACS}$ | —           | 20   | —           | 25   | ns   | —     |
| Chip Selection to Output in Low Z    | $t_{LZ}$  | 0           | —    | 0           | —    | ns   | 1, 2  |
| Output Enable to Output Valid        | $t_{OE}$  | 0           | 10   | 0           | 10   | ns   | —     |
| Output Enable to Output in Low Z     | $t_{OLZ}$ | 0           | —    | 0           | —    | ns   | 1, 2  |
| Chip Deselection to Output in High Z | $t_{HZ}$  | 0           | 8    | 0           | 10   | ns   | 1, 2  |
| Output Hold from Address Change      | $t_{OH}$  | 5           | —    | 5           | —    | ns   | —     |

**NOTES:** 1. This parameter is sampled and not 100% tested.

2. Transition is measured  $\pm 200\text{mV}$  from steady state voltage with specified loading is Load B.

## • Write Cycle

| Item                               | Symbol    | HM6709JP-20 |      | HM6709JP-25 |      | Unit | Notes |
|------------------------------------|-----------|-------------|------|-------------|------|------|-------|
|                                    |           | Min.        | Max. | Min.        | Max. |      |       |
| Write Cycle Time                   | $t_{WC}$  | 20          | —    | 25          | —    | ns   | 1     |
| Chip Selection to End of Write     | $t_{CW}$  | 15          | —    | 20          | —    | ns   | —     |
| Address Setup Time                 | $t_{AS}$  | 0           | —    | 0           | —    | ns   | —     |
| Address Valid to End of Write      | $t_{AW}$  | 15          | —    | 20          | —    | ns   | —     |
| Write Pulse Width                  | $t_{WP}$  | 15          | —    | 20          | —    | ns   | —     |
| Write Recovery Time                | $t_{WR}$  | 3           | —    | 3           | —    | ns   | —     |
| Write to Output in High Z          | $t_{WZ}$  | 0           | 8    | 0           | 10   | ns   | 2, 3  |
| Data Valid to End of Write         | $t_{DW}$  | 12          | —    | 15          | —    | ns   | —     |
| Data Hold Time                     | $t_{DH}$  | 0           | —    | 0           | —    | ns   | —     |
| Output Disable to Output in High Z | $t_{OHZ}$ | 0           | 8    | 0           | 10   | ns   | 2, 3  |
| Output Active from End of Write    | $t_{OW}$  | 0           | —    | 0           | —    | ns   | 2, 3  |

**NOTES:** 1. All write cycle timings are referenced from the last valid address to the first transitioning address.

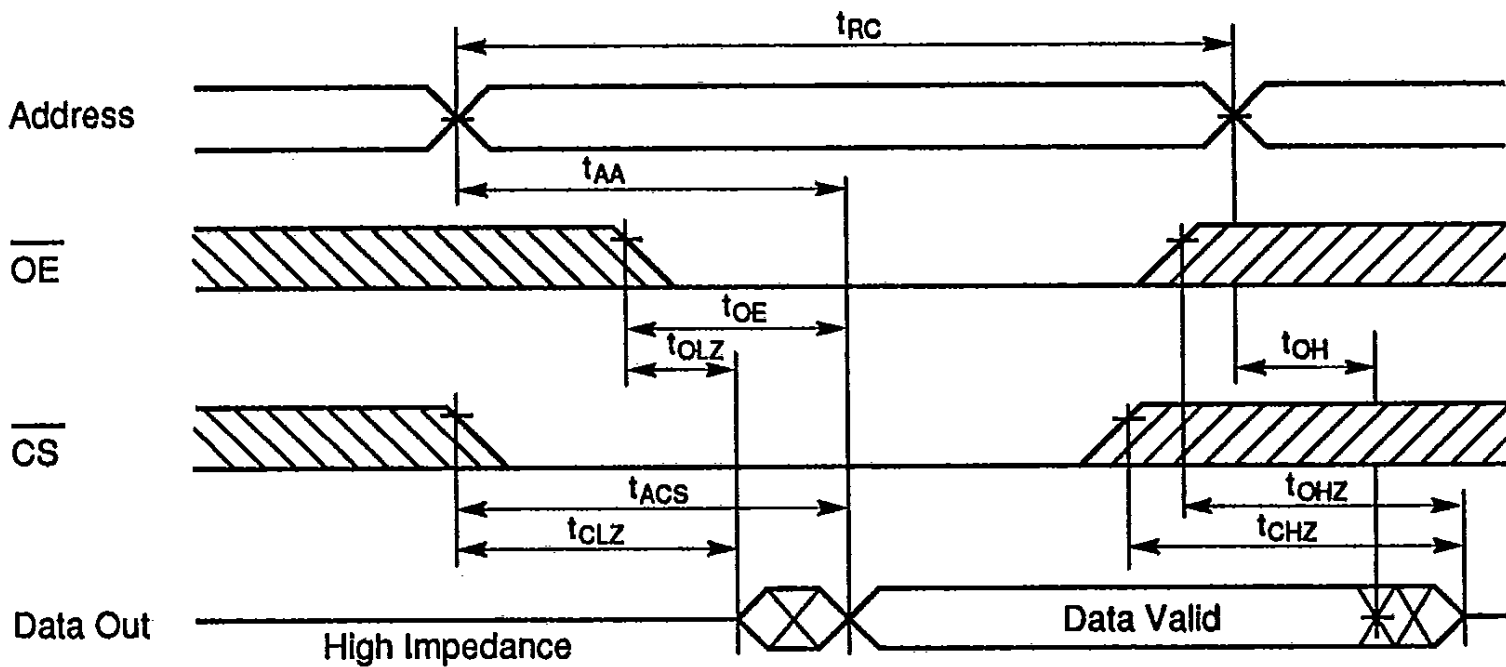
2. This parameter is sampled and not 100% tested.

3. Transition is measured  $\pm 200\text{mV}$  from steady state voltage with specified loading in Load B.

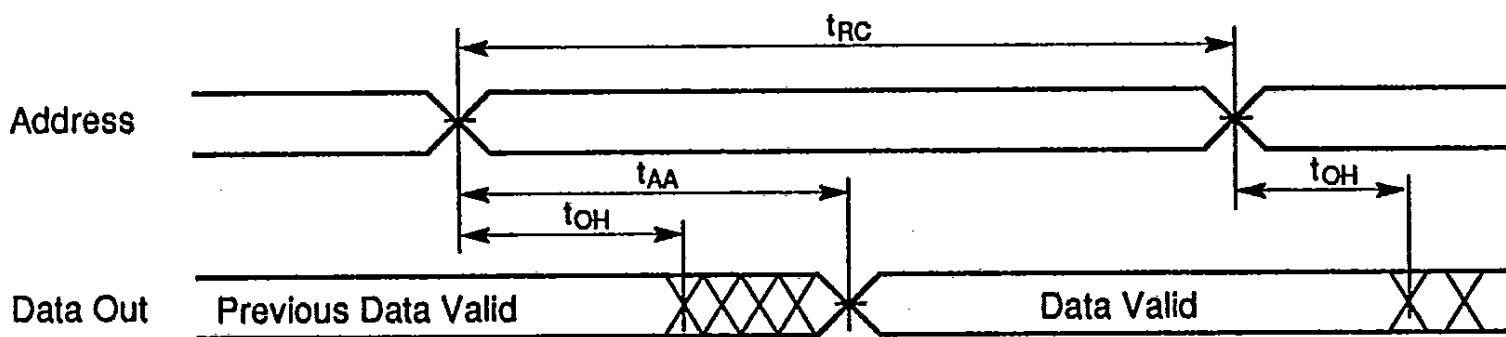
## ■ TIMING WAVEFORM

T-46-23-10

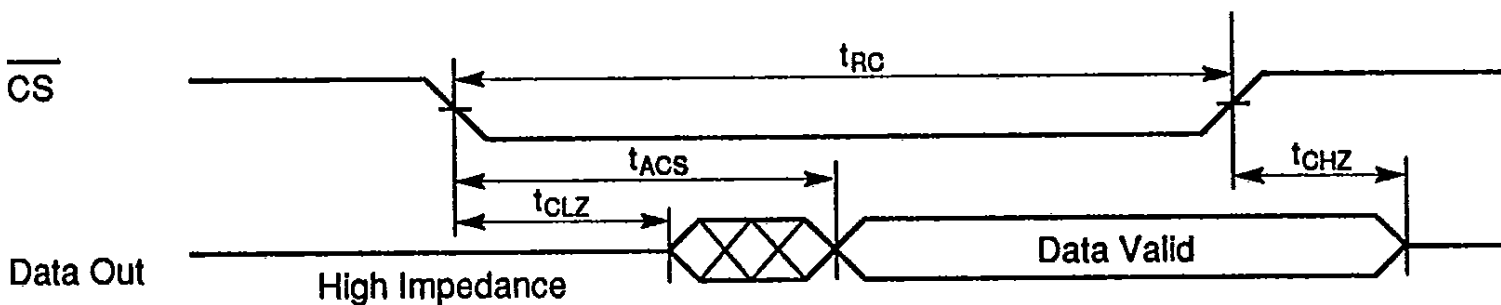
## • Read Cycle (1) (1)



## • Read Cycle (2) (1) (2) (3)

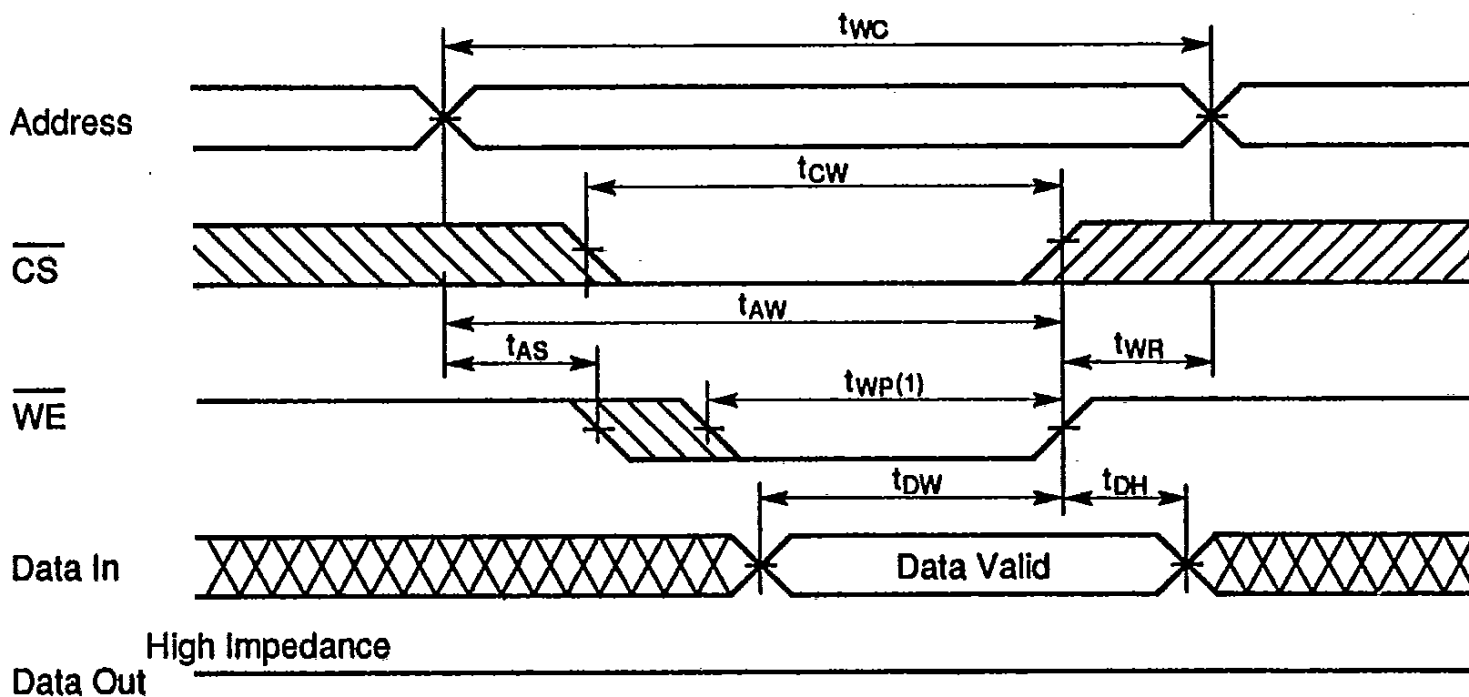
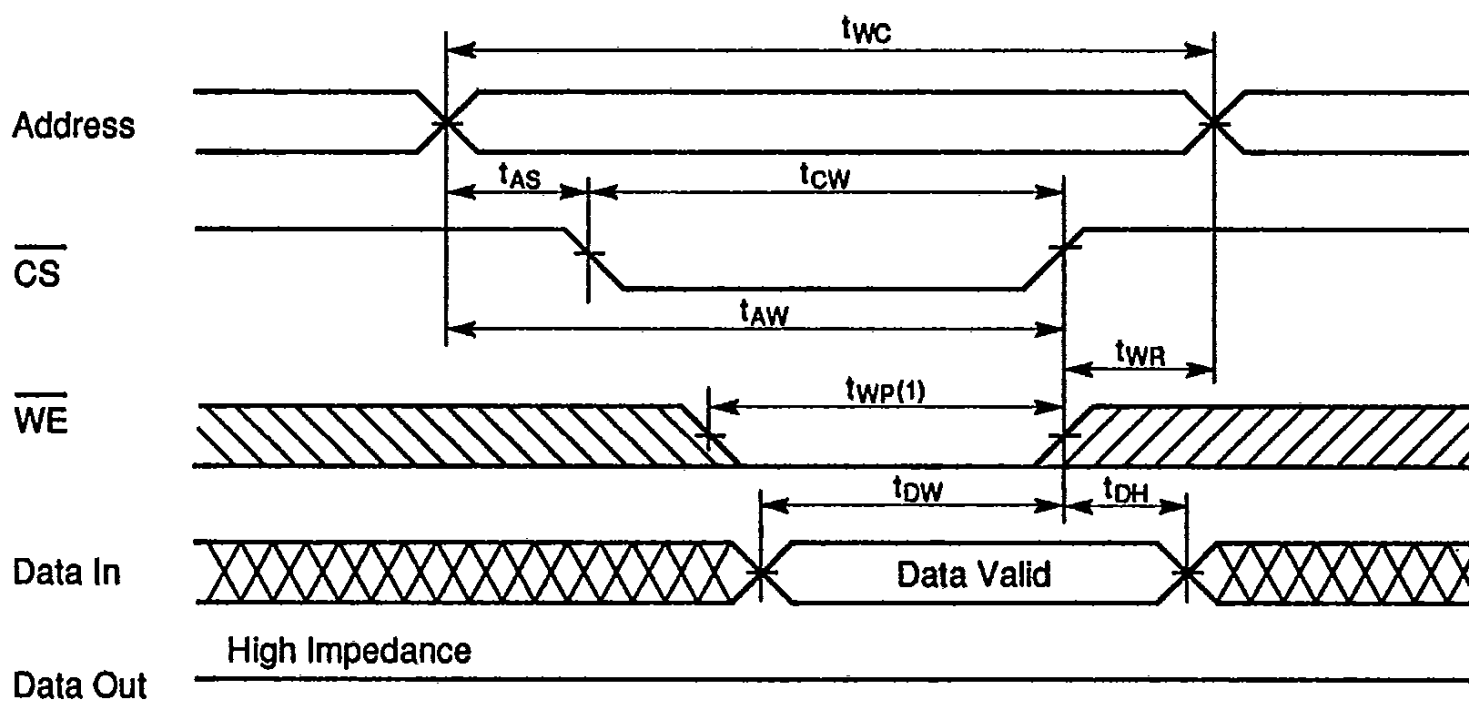


## • Read Cycle (3) (1) (3) (4)



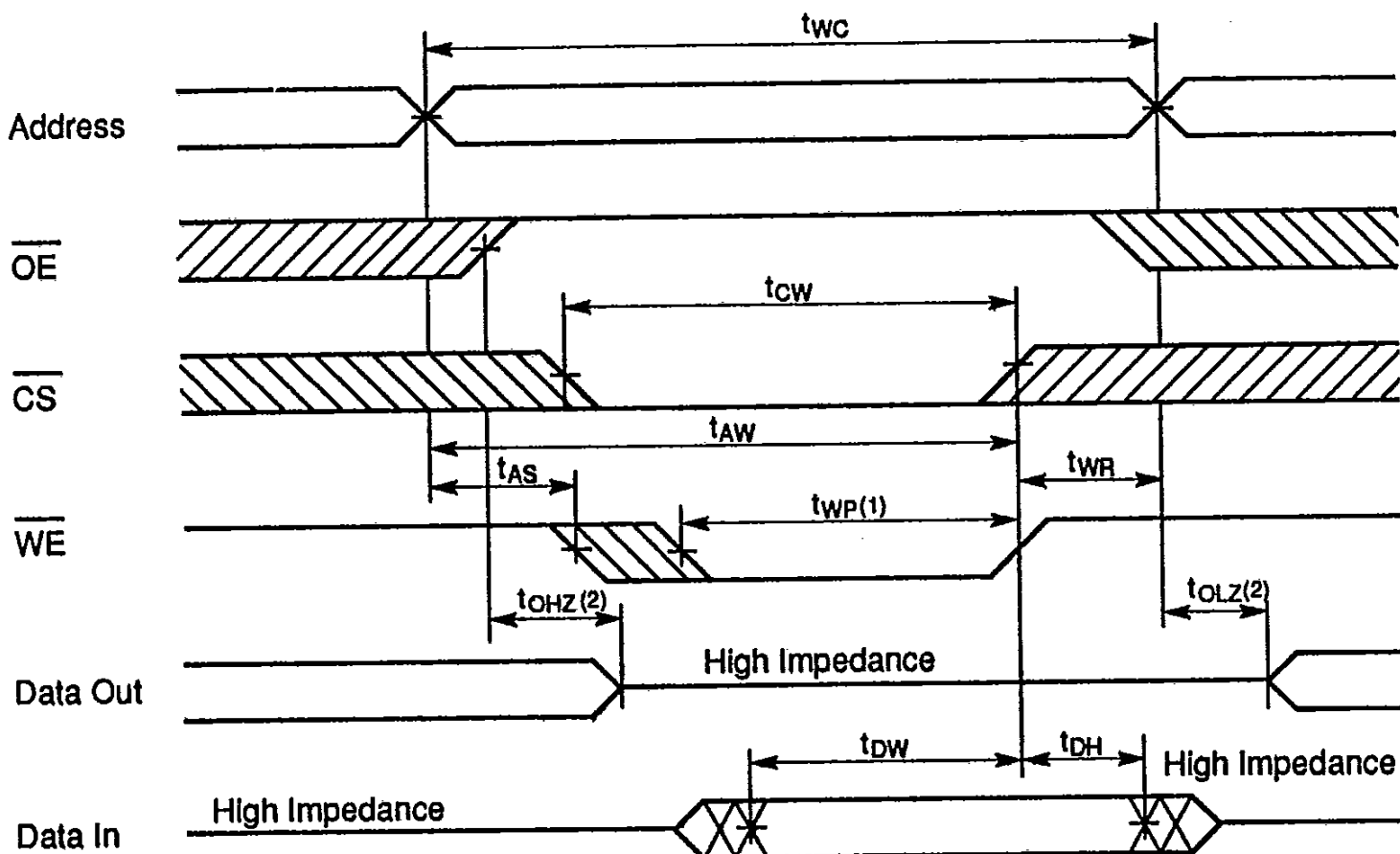
## NOTES:

1.  $\overline{WE} = V_{IH}$
2.  $\overline{CS} = V_{IL}$
3.  $\overline{OE} = V_{IL}$
4. Address valid prior to or coincident with  $\overline{CS}$  transition low.

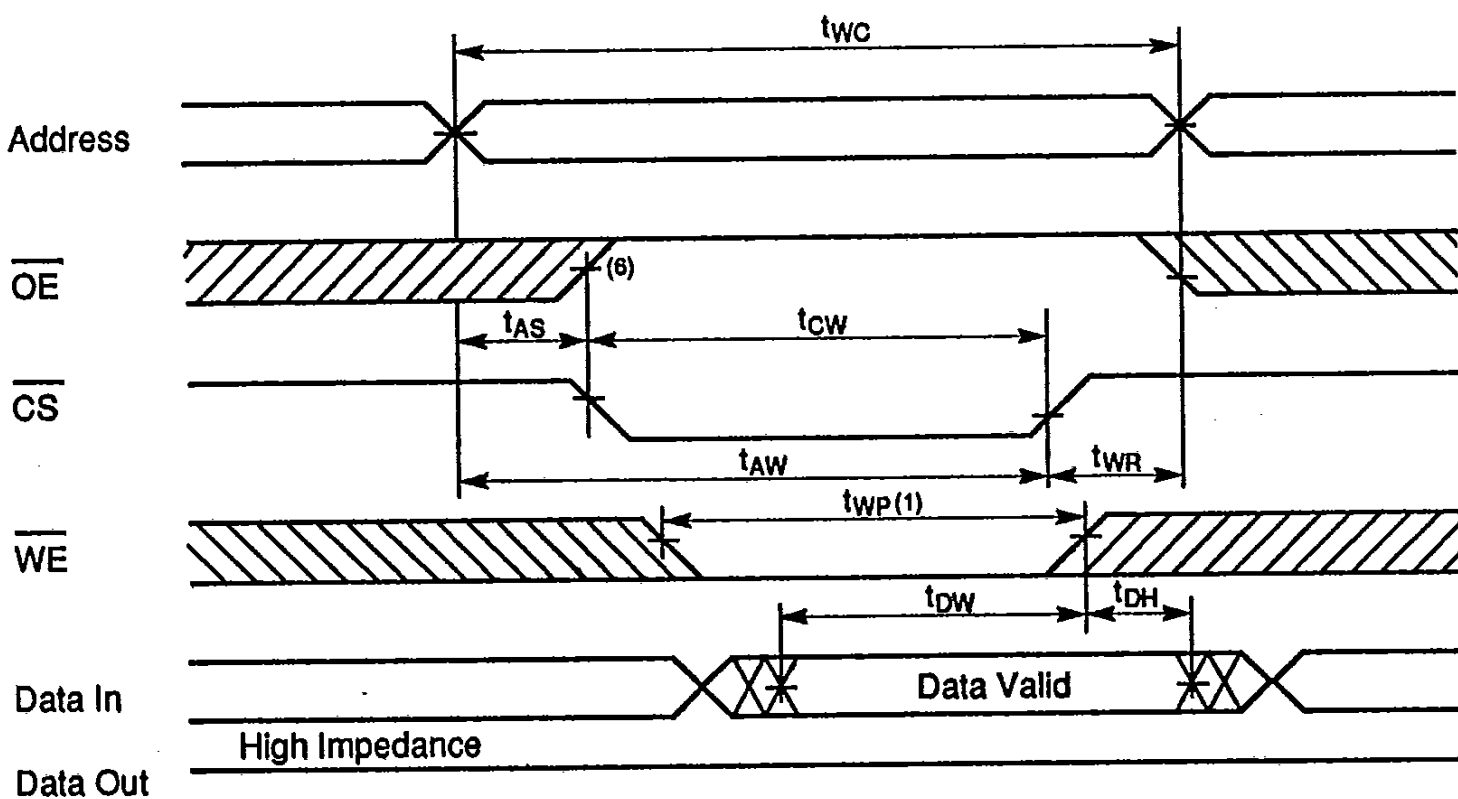
**• Write Cycle (1) ( $\overline{OE} = H$ ,  $\overline{WE}$  Controlled)****• Write Cycle (2) ( $\overline{OE} = H$ ,  $\overline{CS}$  Controlled)**

• **Write Cycle (3)** ( $\overline{OE}$  = Clocked,  $\overline{WE}$  Controlled)

T-46-23-10

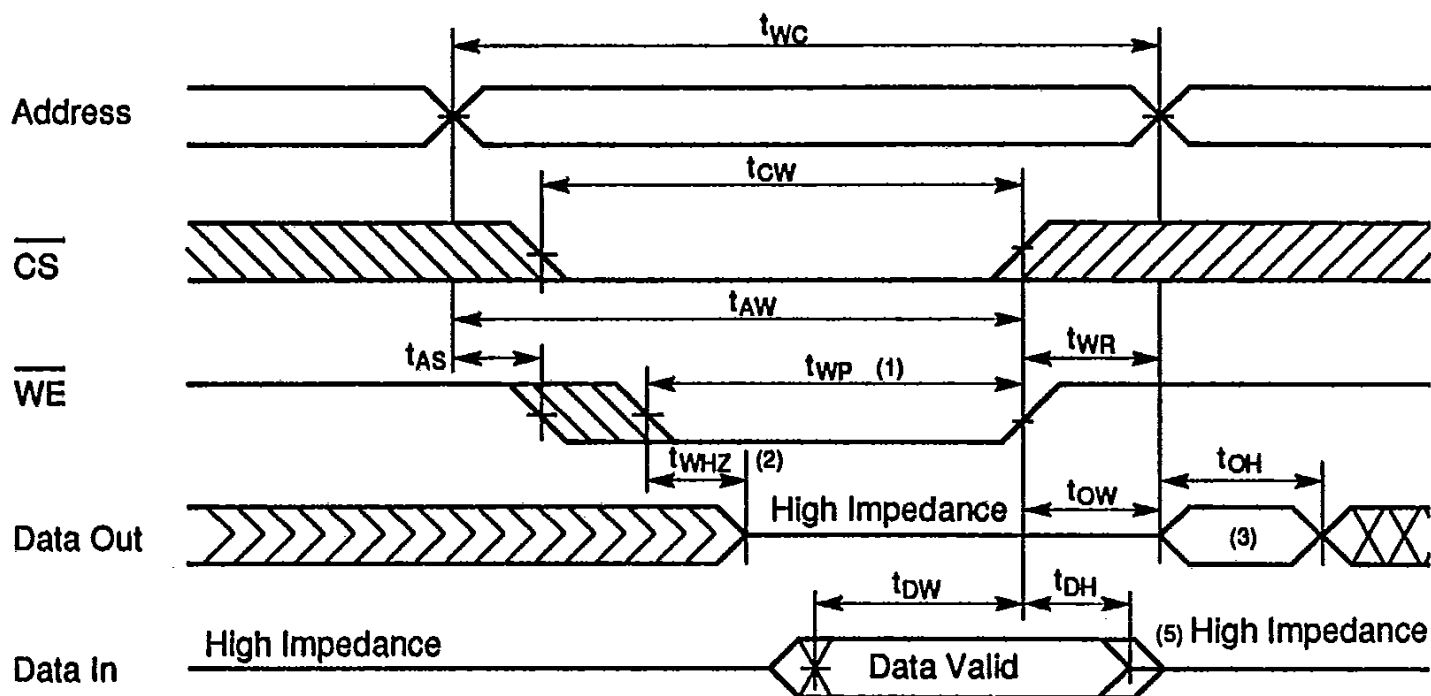
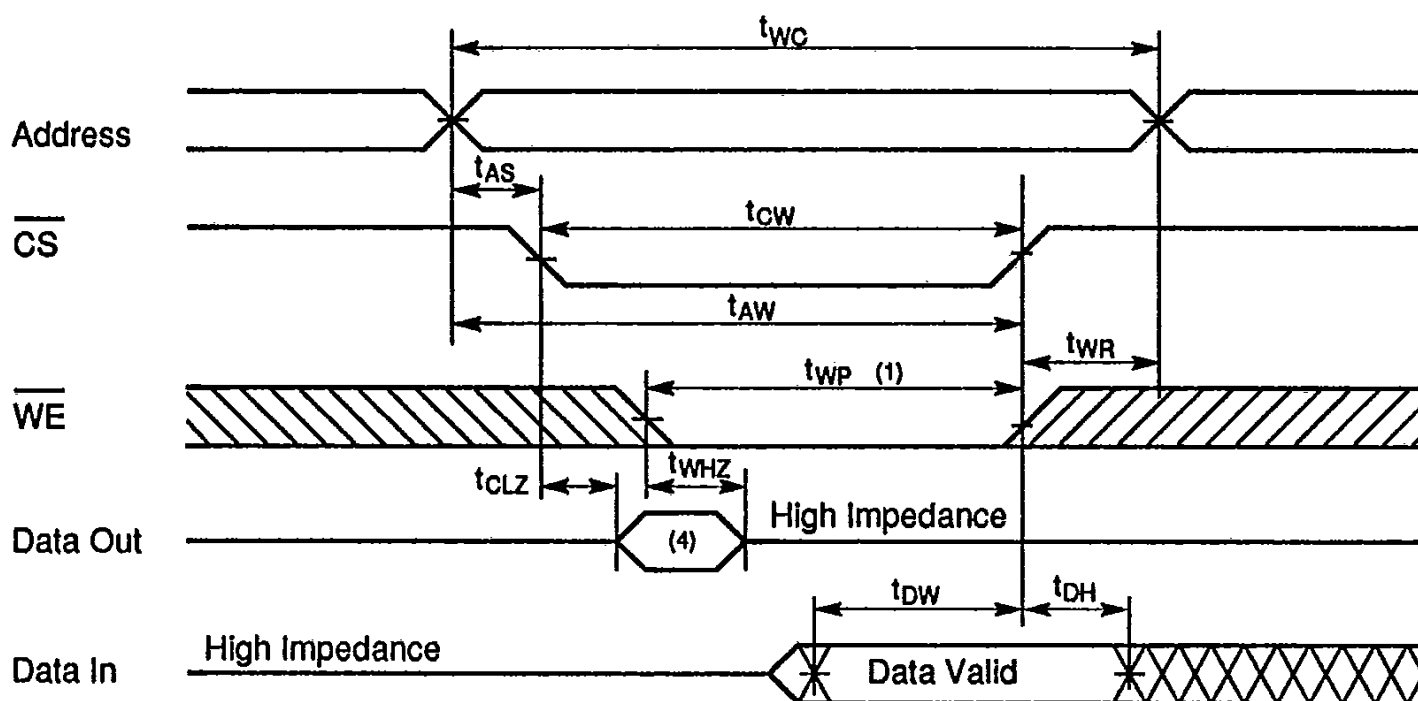


• **Write Cycle (4)** ( $\overline{OE}$  = Clocked,  $\overline{CS}$  Controlled)



• Write Cycle (5) ( $\overline{OE} = L$ ,  $\overline{WE}$  Controlled)

T-46-23-10

• Write Cycle (6) ( $\overline{OE} = L$ ,  $\overline{CS}$  Controlled)

## NOTES:

1. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}$  and a low  $\overline{WE}$ .
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If the  $\overline{CS}$  is low transition occurs after the  $\overline{WE}$  low transition, output remain in a high impedance state.
5. If  $\overline{CS}$  is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{OE}$  high transition or after the  $\overline{OE}$  transition, output remain in high impedance state.

www.DataSheet4U.com