

50 Gbps, 1:2 FANOUT BUFFER MODULE

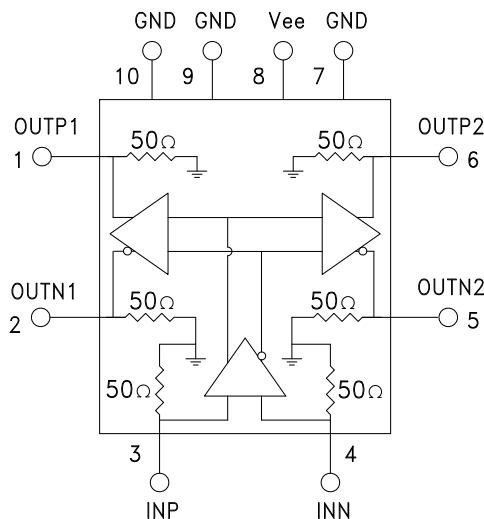


Typical Applications

The HMC-C062 is ideal for:

- OC-768 and SDH STM-256 Equipment
- Serial Data Transmission up to 50 Gbps
- Short, intermediate, and long haul fiber optic applications
- Broadband Test and Measurement

Functional Diagram



Features

- Supports Data Rates up to 50 Gbps
- Supports Clock Frequencies up to 30 GHz
- Inputs Terminated Internally in 50 ohms
- Supports Single-Ended or Differential Operation
- Very Low Power Consumption: 455 mW
- Less than 200 fs Additive RMS Jitter
- Fast Rise and Fall Times: <11ps
- Single -3.3V Power Supply
- Hermetically Sealed Module: 1.85mm connectors
- 40°C to +70°C Operating Temperature

General Description

The HMC-C062 is a fanout buffer designed to support data transmission rates of up to 50 Gbps. The device can also operate with clock signals up to 30 GHz. The input is broadband from DC to 30 GHz. During normal operation, input data (or clock) is transferred to both output channels. Differential input signals to the HMC-C062 are terminated with 50 Ohms to ground on-chip, and may be either AC or DC coupled. The differential outputs of the HMC-C062 may be either AC or DC coupled. Outputs can be connected directly to a 50 Ohm to ground terminated system, while DC blocking capacitors may be used if the terminating system is 50 Ohms to a non-ground DC voltage. The HMC-C062 operates from a single -3.3V DC supply, and is housed in a hermetically sealed module with 1.85mm connectors.

Electrical Specifications, $T_A = +25^\circ\text{C}$, $V_{ee} = -3.3\text{V}$

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage	±5% Tolerance	-3.46	-3.3	-3.13	V
Power Supply Current			138	170	mA
Maximum Data Rate	NRZ Format	50			Gbps
Maximum Clock Frequency		30			GHz
Deterministic Jitter [2]			2		ps
Additive Random Jitter [3]			< 0.2		ps
Rise Time, tr	20% - 80%		9.5		ps
Fall Time, tf	20% - 80%		11		ps

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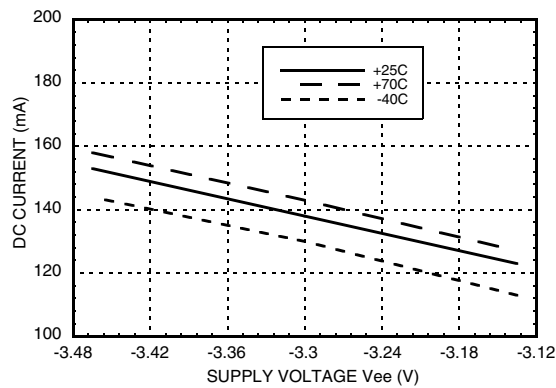
Electrical Specifications, (continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
Output Amplitude	Differential @ 40 Gbps		500		mV
Input Amplitude	Single-Ended	100		800	mV
	Differential	100		2000	mV
Input Return Loss	< 25 GHz		9		dB
Output Return Loss	< 25 GHz		9		dB
Propagation Delay, td			270		ps
Input High Voltage		-0.5		0.5	V
Input Low Voltage		-1		0	V
Output High Voltage			-25		mV
Output Low Voltage			-300		mV

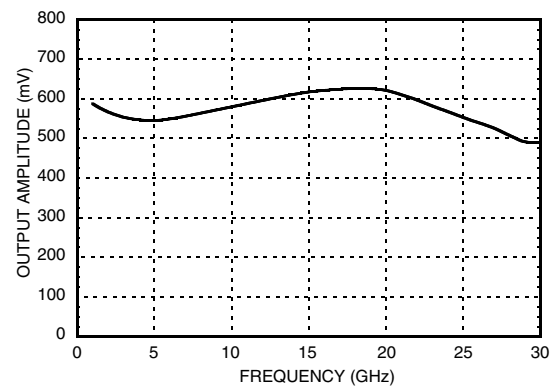
[1] Deterministic jitter measured at 40 Gbps with PRBS 2¹³-1 pattern. It is the peak to peak deviation from the ideal time crossing

[2] Random jitter is measured with 40 Gbps 10101... pattern

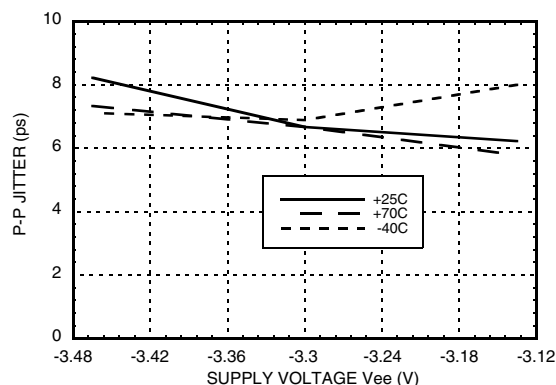
DC Current vs. Supply Voltage



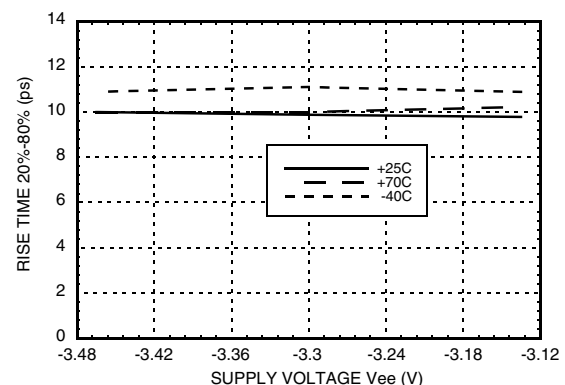
Differential Output vs. Frequency [3]



Peak-to-Peak Jitter vs. Supply Voltage [1] [2]



Rise Time vs. Supply Voltage [1]



[1] Data input = 40 Gbps PRBS 2²³-1

[2] Source jitter was not deembedded.

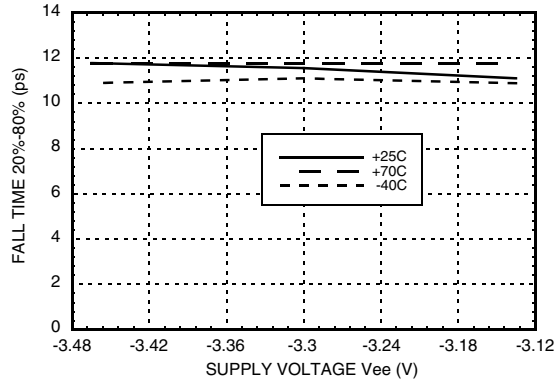
[3] Measured with 101010... pattern

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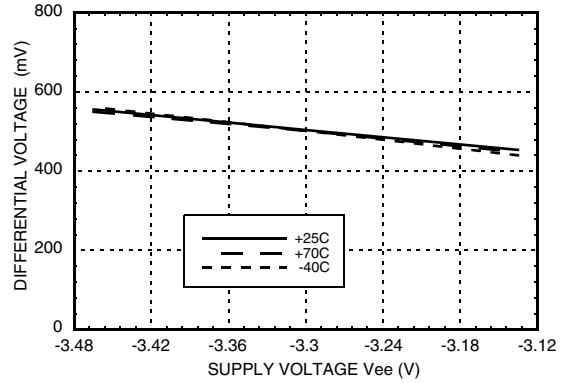
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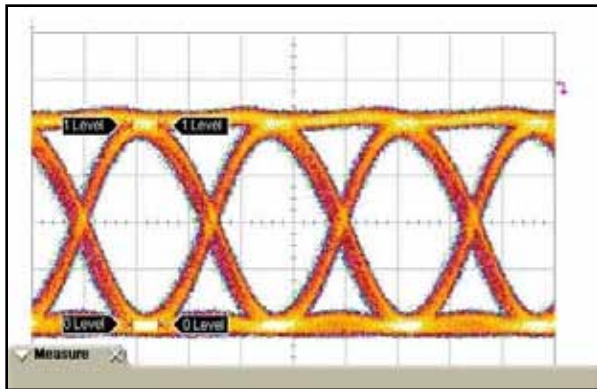
Fall Time vs. Supply Voltage [1]



Differential Output vs. Supply Voltage

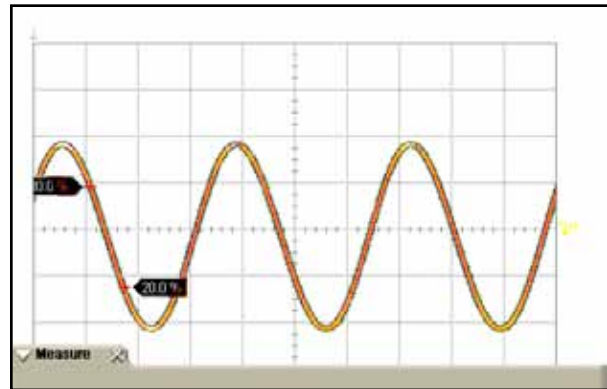


Eye Diagrams



	Current	Minimum	Maximum	Total Meas
Jitter p-p (3)	5.33 ps	4.000 ps	5.333 ps	30
Rise Time (3)	9.56 ps	9.11 ps	9.56 ps	30
Fall Time (3)	10.67 ps	10.44 ps	11.11 ps	30
Eye Amplitude (3)	249 mV	249 mV	249 mV	30
Vertical Scale	58.1 mV / div			
Horizontal Scale	10.0 ps / div			

Test Conditions:
 Eye diagram data presented on an Infinium DCA 86100C
 Rate = 40 GB/s
 Psuedo Random Code = 2²³-1
 Vin = 200 mVpp Differential
 Vout = Single-ended



	Current	Minimum	Maximum	Total Meas
Rise Time (f1)	6.00 ps	5.56 ps	6.00 ps	30
Fall Time (f1)	6.44 ps	6.22 ps	6.44 ps	30
Jitter p-p (f1)	1.333 ps	667 fs	1.556 ps	30
Jitter RMS (f1)	252 fs ps	193 fs	252 fs	30
Vertical Scale	124.2 mV / div			
Horizontal Scale	10.0 ps / div			

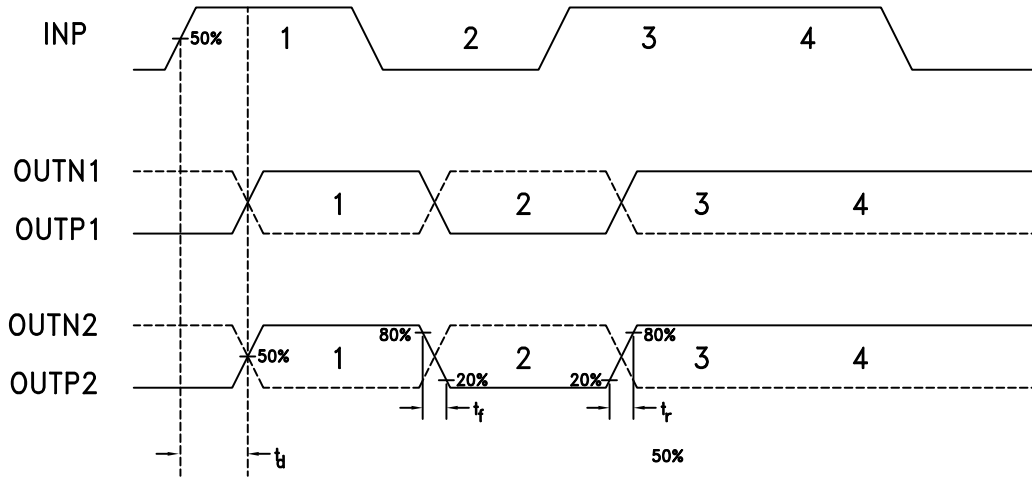
Test Conditions:
 Eye diagram data presented on an Infinium DCA 86100C
 Rate = 30 GHz clock
 Vin = 300 mVpp single ended
 Vout = Differential
 Source Jitter is not deembedded from RMS Jitter measurements

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Timing Diagram



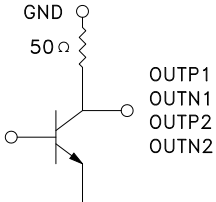
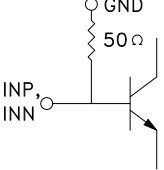

Truth Table

Input	Outputs	
IN	OUT1	OUT2
L	L	L
H	H	H

Notes:
 IN = INP - INN
 OUT1 = OUTP1 - OUTN1
 OUT2 = OUTP2 - OUTN2

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Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 2 5, 6	OUTP1, OUTN1 OUTP2, OUTN2	Differential outputs (Channel 1) Differential outputs (Channel 2)	
3, 4	INP, INN	Differential inputs.	
7, 9, 10	GND	Signal and supply ground.	
8	Vee	Negative Supply	