0.1 MHz to 500 MHz Clock Generator with Integer N PLL

Data Sheet **HMC1031**

FEATURES

- Low current consumption: 1.95 mA typical
- High phase frequency detector rate: 140 MHz
- Hardware pin-programmable clock multiplication ratios: 1×/5×/10×
- Lock detect indicator
- Power-down mode (0.8 µA typical)
- 8-lead MSOP package: 4.9 mm × 3.0 mm

APPLICATIONS

- Low jitter clock generation
- Low bandwidth (BW) jitter attenuation
- Low frequency phase-locked loops (PLLs)
- Frequency translation
- Oven controlled crystal oscillator (OCXO) frequency multipliers
- Phase lock clean high frequency references to 10 MHz equipment

FUNCTIONAL BLOCK DIAGRAM

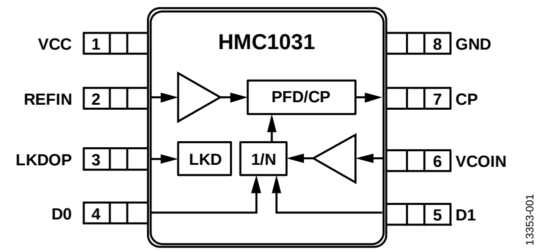

Figure 1.

GENERAL DESCRIPTION

Together with an external loop filter and a voltage controlled crystal oscillator (VCXO), the HMC1031 forms a complete clock generator solution targeted at low frequency jitter attenuation and reference clock generation applications.

The HMC1031 features a low power integer N divider, supporting divide ratios of 1, 5, and 10, which is controlled via external hardware pins and requires no serial port.

The integrated phase detector and charge pump are capable of operating at up to 140 MHz, and a maximum VCXO input of 500 MHz ensures frequency compliance with a wide variety of system clocks and VCXOs.

Additional features include an integrated lock detect indicator available on a dedicated hardware pin, and a built in power-down mode.

The HMC1031 is housed in an 8-lead MSOP package.

Rev. C Document Feedback

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REVISION HISTORY

10/15—v02.0215 to Rev. C

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

Changed MS8E to MSOP and VCO Input to VCOIN ... Throughout
Changes to Features Section ... 1
Changes to Figure 3, Figure 4, and Figure 6 ... 6
Deleted GND Interface Schematic; Renumbered Sequentially .. 7
Change to Figure 17 ... 8
Changes to Lock Detector Section ... 10
Changes to Figure 25 ... 12
Updated Outline Dimensions ... 13
Changes to Ordering Guide ... 13

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, VCC = 3.3 V, unless otherwise specified.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY VOLTAGE		2.7	3.3	3.5	V
OPERATING TEMPERATURE		−40	+27	+85	°C
FREQUENCY[1]					
Reference Input[2]				140	MHz
VCO Input				500	MHz
CHARGE PUMP					
Current			50		µA
Output Range[3]			0.2 to VCC − 0.4		V
INPUT					
Voltage Swing (Reference and VCOIN Inputs)[1]	Externally ac-coupled to the chip[2]	0.1		3.5	V p-p
REFIN, VCOIN DC Bias	0.5 × VCC approximately		1.65		V
Duty Cycle		40		60	%
Impedance at 50 MHz	Applicable to REFIN and VCOIN pins		3600||4		Ω||pF
DIVIDE RATIOS	VCO/VCXO feedback divider		1/5/10		
FIGURE OF MERIT (FOM)[4]					
Floor	Divide by 10	−212	−208	−204	dBc/Hz
Flicker		−254	−252	−248	dBc/Hz
PHASE AND FLICKER NOISE					
Flicker Noise (PN_{FLICK})	PN_{FLICK} = *Flicker FOM* + 20log(f_{VCXO}) − 10log(f_{OFFSET}), where f_{VCXO} is the VCXO frequency and f_{OFFSET} is the offset frequency		Determined by formula		
Phase Noise Floor (PN_{FLOOR})	PN_{FLOOR} = *Floor FOM* + 10log(f_{PD}) + 20log(f_{VCXO}/f_{PD}), where f_{PD} is the phase detector frequency		Determined by formula		
CURRENT					
Supply[5]	100 MHz reference = VCXO, VCC = 3.3 V		1.95		mA
Power-Down[6]	VCC = 3.0 V, 25°C, D0 = 0, D1 = 0		0.05		µA
	VCC = 3.3 V, 85°C		0.8		µA
	VCC = 3.6 V, 85°C		1		µA
LOCK DETECT OUTPUT CURRENT	CMOS output level			3	mA

[1] The REFIN and VCOIN inputs must be ac-coupled to the HMC1031. The peak input level must not exceed VCC + 0.4 V with respect to GND.
[2] The lower limit of operation, 0.1 MHz, is limited by off chip ac coupling. Select the size of the ac coupling capacitor such that the impedance, relative to the 3.6 kΩ input impedance of the device and any termination impedances on the evaluation board (50 Ω by default), is insignificant.
[3] The PLL may lock in the voltage range of 0.2 V to VCC − 0.4 V. However, the charge pump gain may be reduced. See Figure 14 for charge pump compliance.
[4] See Figure 20 and Figure 21 for additional flicker FOM and floor FOM data, respectively.
[5] See Figure 17 for additional supply current data. Base frequency: 100 MHz; base VCC: 3.3 V, 0.8 mA/V to 1 mA/V; base phase frequency detector (PFD) current: 1.8 mA, 8 µA/MHz; base divider current: 1.15 mA, 15 µA/MHz. For example, the device current for a 10 MHz reference and 50 MHz VCO at 3.0 V VCC can be calculated as: ΔPFD current = $(10 − 100) \times (8 \times 10^{-6}) = −0.72$ mA, ΔDIV current = $(50 − 100) \times (15 \times 10^{-6}) = −0.75$ mA, device current = (1.8 − 0.72) + (1.15 − 0.75) = 1.48 mA at 3.3 V VCC. At 3 V, the VCC device current is approximately: $1.48 − (0.85 \times 10^{-3}) \times (3.3 − 3.0) = 1.225$ mA.
[6] In power-down mode, the REFIN/VCOIN inputs and charge pump outputs are tristated. The power-down leakage current is measured without any signal applied to the HMC1031.

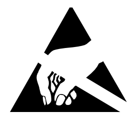
ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC to GND	−0.3 V to +3.6 V
D0, D1 Pins to GND	−0.3 V to +3.6 V
Maximum REFIN Input Voltage	VCC + 0.4 V
Maximum VCOIN Input Voltage	VCC + 0.4 V
Maximum Junction Temperature	125°C
Maximum Peak Reflow Temperature (MSL1)	260°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Thermal Resistance	0.2°C/mW
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
ESD Sensitivity (Human Body Model (HBM))	Class 2

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

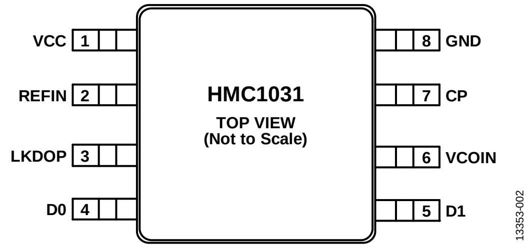


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCC	Supply Voltage (3.3 V Typical).
2	REFIN	Reference Input. REFIN is an externally ac-coupled reference frequency input.
3	LKDOP	Lock Detect Output, CMOS Drive.
4, 5	D0, D1	Integer N Division Ratio Selection. D0 and D1 are the CMOS inputs used to specify the integer N division ratio. See Table 4.
6	VCOIN	Voltage Controlled Oscillator Input. VCOIN is an ac-coupled VCO/VCXO input.
7	CP	Charge Pump Output.
8	GND	Ground.

Table 4. Frequency Multiplication Truth Table

D0	D1	PLL Feedback Division Ratio (N)[1]
0	0	Power-down mode
1	0	Divide by 1
0	1	Divide by 5
1	1	Divide by 10

[1] Set by SW1 in the evaluation PCB schematic (see Figure 24).

INTERFACE SCHEMATICS

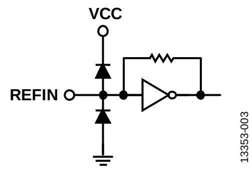


Figure 3. REFIN Interface Schematic

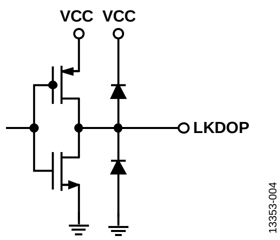


Figure 4. LKDOP Interface Schematic

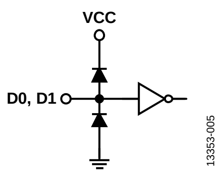


Figure 5. D0, D1 Interface Schematic

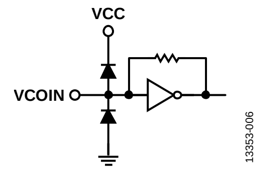


Figure 6. VCOIN Interface Schematic

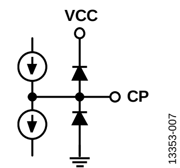


Figure 7. CP Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, VCC = 3.3 V, unless otherwise specified.

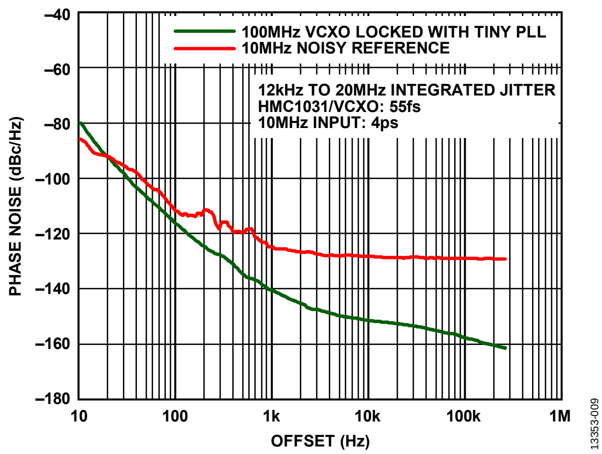


Figure 8. 10 MHz to 100 MHz with Noisy Reference Phase Noise; Loop Filter Value: C8 = 4.7 nF, R7 = 1.2 kΩ, C9 = 62 µF, Loop Filter BW = 8 Hz, VCXO = 100 MHz Crystek CVHD-950

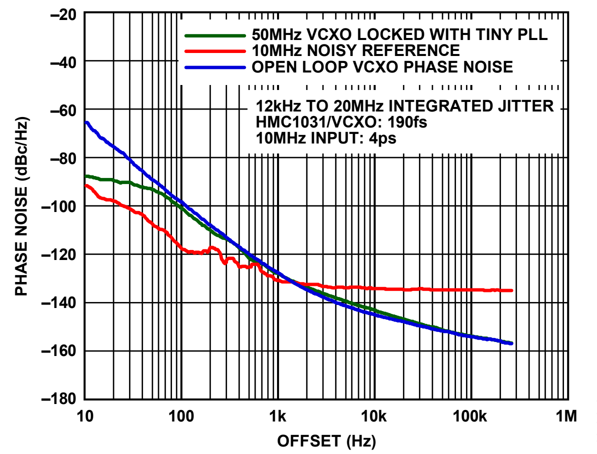


Figure 11. 10 MHz to 50 MHz with Noisy Reference Phase Noise; Loop Filter Value: C8 = 220 nF, R7 = 3.3 kΩ, C9 = 2.2 µF, Loop Filter BW = 50 Hz, VCXO = Bliley V105ACACB, 50 MHz

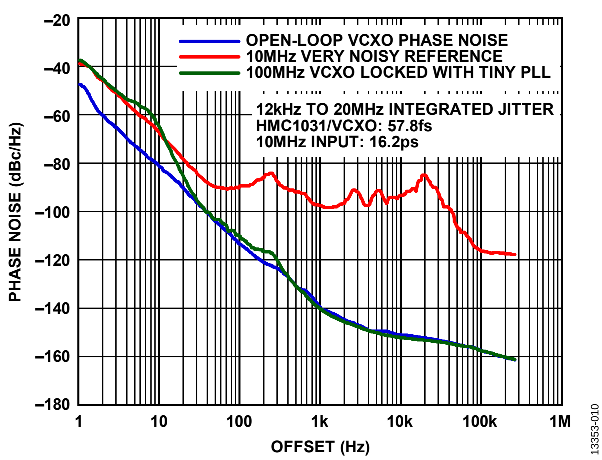


Figure 9. 10 MHz to 100 MHz with Very Noisy Reference Phase Noise; Loop Filter Value: C8 = 4.7 nF, R7 = 1.2 kΩ, C9 = 62 µF; Loop Filter BW = 8 Hz; VCXO = 100 MHz Crystek CVHD-950

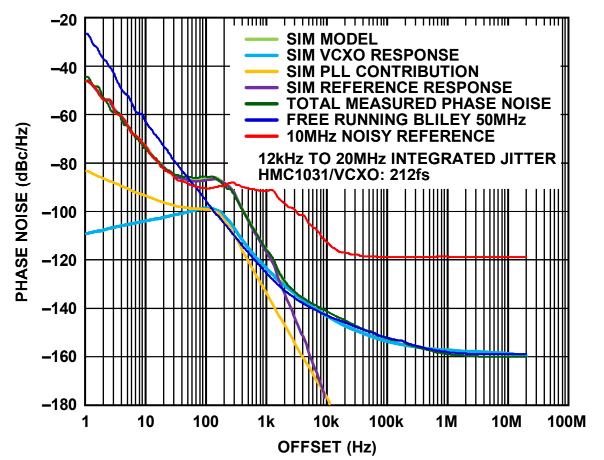


Figure 12. Typical Closed-Loop Phase Noise, HMC1031 as Jitter Attenuator, Loop BW = 100 Hz; Refer to Loop Filter Configuration 2 in Table 5

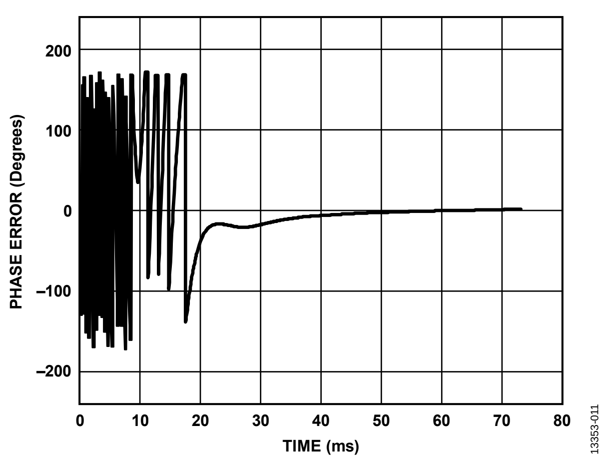


Figure 10. Phase Error During Lock Time for Divide by 5; 10 MHz Input; 50 MHz Output; Loop BW = 100 Hz; Refer to Loop Filter Configuration 2 in Table 5

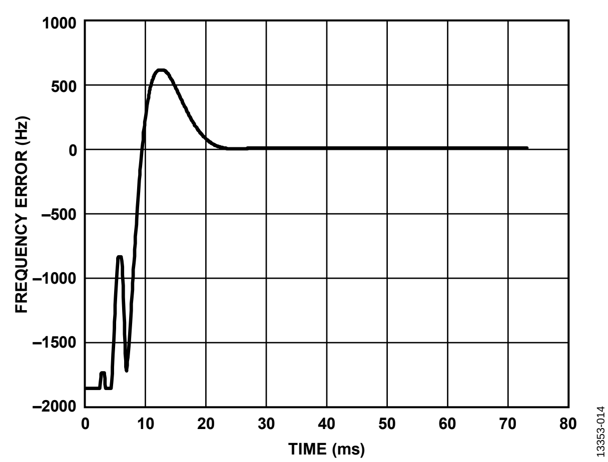


Figure 13. Frequency Error During Lock Time for Divide by 5; 10 MHz Input; 50 MHz Output; Loop Bandwidth = 100 Hz; Refer to Loop Filter Configuration 2 in Table 5

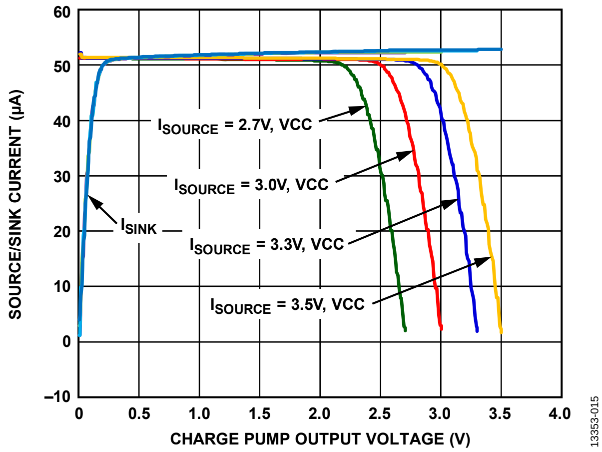


Figure 14. Typical Source and Sink Current vs. Charge Pump Output Voltage

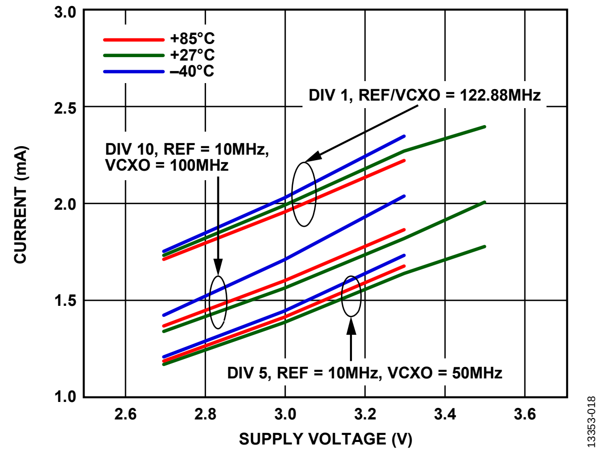


Figure 17. Current vs. Supply Voltage, Different Configurations

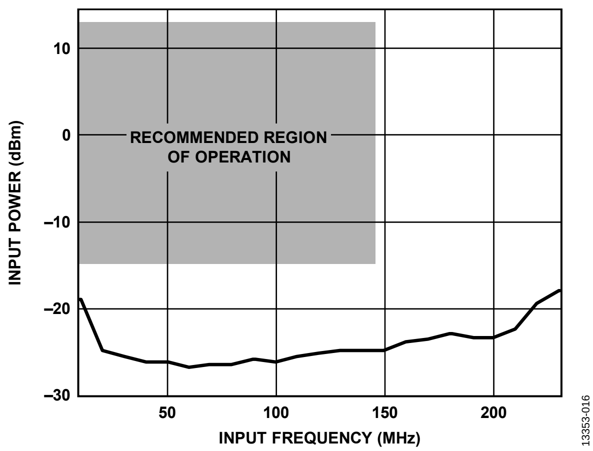


Figure 15. REFIN Input Power vs. Input Frequency

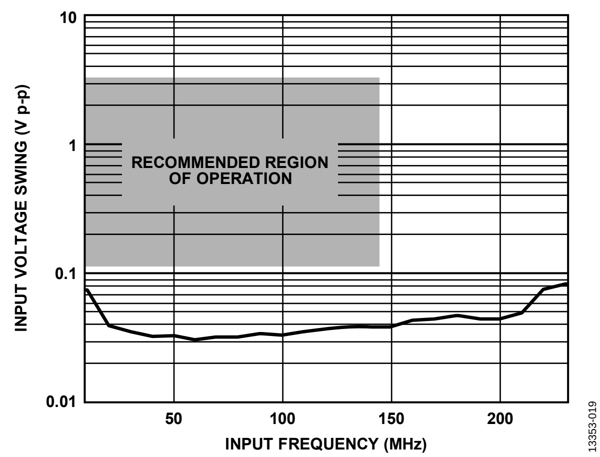


Figure 18. REFIN Input Voltage Swing vs. Input Frequency

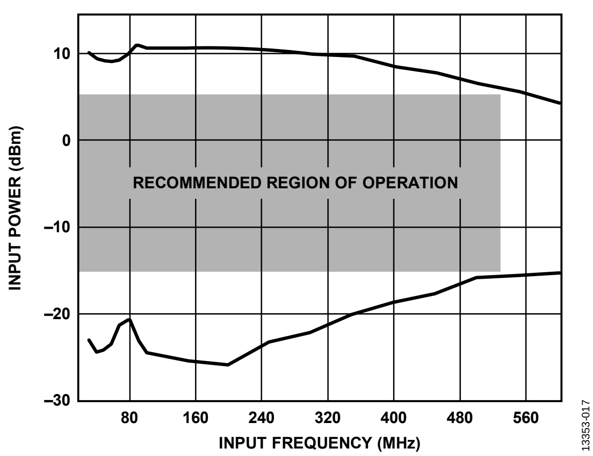


Figure 16. VCOIN Input Power vs. Input Frequency, Maximum Frequency Is Guaranteed in the Recommended Region of Operation Across Temperature and Process Variation

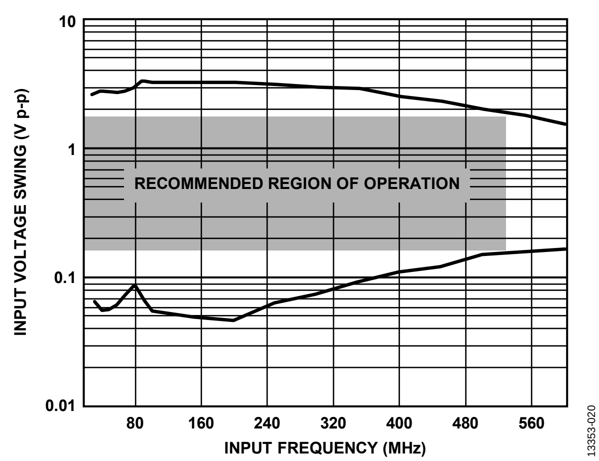


Figure 19. VCOIN Input Voltage Swing vs. Input Frequency; Maximum Frequency Is Guaranteed in the Recommended Region of Operation Across Temperature and Process Variation

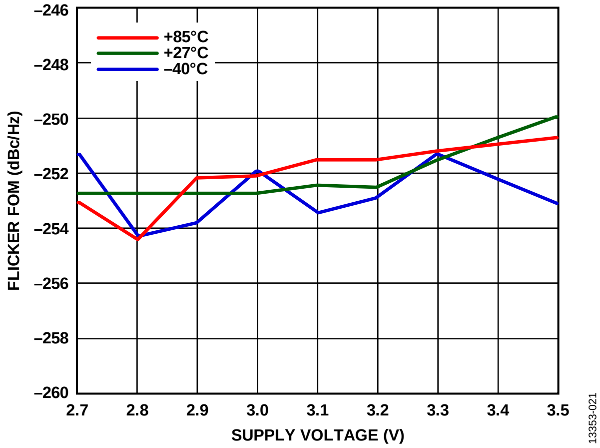


Figure 20. Flicker FOM

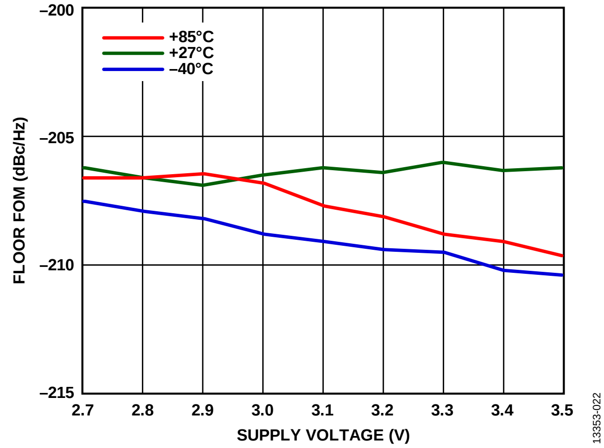


Figure 21. Floor FOM

APPLICATIONS INFORMATION

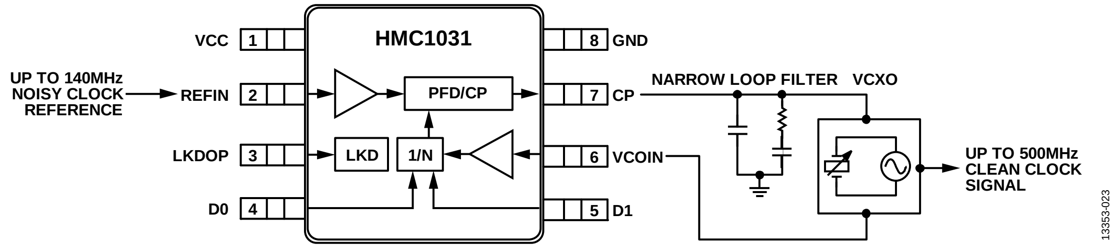


Figure 22. Typical Application Diagram

JITTER ATTENUATION

In some cases, reference clocks to the system may come from external noisy sources with high jitter. The HMC1031 can be used to attenuate this incoming jitter and distribute a clean clock in the system. In such a scheme, a narrow loop filter is selected for the HMC1031. The device frequency locks to the external VCXO, but the reference jitter is attenuated as defined by the set loop filter bandwidth. The final output frequency and phase noise characteristics outside the loop bandwidth is defined by the phase noise characteristics of the VCXO used. A low jitter clock reference yields better clocking performance and better LO performance of the RF PLL VCOs, and improves the SNR performance of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs).

FREQUENCY TRANSLATION

The reference clock in a test and measurement system or a communications system is often a high accuracy OCXO with excellent long-term stability. In some applications, the OCXO frequency must be multiplied up to a higher rate to drive the primary clock inputs in a system. The HMC1031 offers a very low power, small package and high performance method to multiply its incoming frequency in 1×, 5×, and 10× rates. Such multiplication is required because the higher reference clocks improve phase noise, ADC/DAC signal-to-noise ratio (SNR), clock generator jitter, and PHY bit error rates (BERs). In this scheme, the HMC1031 can be connected to an external low cost VCXO (for example, at 50 MHz or 100 MHz), and lock this external VCXO to the excellent long-term stability of the OCXO.

LOOP BANDWIDTHS WITH HMC1031

In typical jitter attenuation applications, an incoming reference clock is frequency locked with a narrow PLL loop bandwidth such that its incoming noise is filtered out by the PLL and VCXO combination. The out of band phase noise of the PLL follows the VCXO that it is locked to. A narrow PLL loop bandwidth ensures that the output jitter is determined by the VCXO (or any other type of high quality factor VCO) and not affected by the spectral noise of the incoming clock beyond the set loop bandwidth.

To facilitate narrow bandwidth loop filter configurations, the HMC1031 is designed to have a low charge pump current of 50 µA. This architecture offers advantages in low power consumption and loop filter design. Typically, narrow loop filter bandwidths require large filter capacitors. Due to the low charge pump current design of the HMC1031, smaller loop filter capacitor sizes can be used to implement narrow loop filters. Note that the HMC1031 is designed to operate in loop bandwidths of only a few kilohertz in its widest loop bandwidth configuration.

USING VCOs/VCXOs WITH NEGATIVE TUNING SLOPE

In its typical configuration, the HMC1031 works with any VCO/VCXO that has a positive tuning slope. For any VCO/VCXO with negative tuning slope, that is, when the frequency decreases with increasing tuning voltage, connect the loop filter ac ground to VCC instead of GND.

LOCK DETECTOR

The lock detector measures the arrival times between the divided VCO edge and reference edge appearing at the phase detector. When this offset becomes greater than approximately 6 ns, the lock detector indicates an out of lock condition. Any leakage current on the CP output causes a phase offset between the two edges. Due to the relatively small 50 µA charge pump current, the HMC1031 is sensitive to leakage currents and may indicate a false out of lock condition if the leakage current from the charge pump (Pin 7) to ground is too high.

Leakage currents include dc current through the loop filter capacitors and/or dc current into the VCO tuning voltage pin, V_{TUNE}. It is recommended to use low leakage, loop filter multilayer ceramic capacitors (MLCCs) and careful VCO selection to maximize V_{TUNE} resistance. The maximum acceptable leakage is dependent on the phase detector operating frequency and can be calculated as follows:

$$\frac{I_{LEAKAGE}}{I_{CP}} = \frac{3\text{ ns}}{t_{PD}}$$

where:

$I_{LEAKAGE}$ is the total leakage current in µA.
I_{CP} is the charge pump current in µA (set to 50 µA).
t_{PD} is the reference frequency period in ns.

Internal delays reduce the available lock detector range from 6 ns to 3 ns.

For example, to guarantee correct lock detector operation with a 10 MHz reference (t_{PD} = 100 ns) and no leakage into the VCO V_{TUNE} pin, the total capacitor leakage must be less than 1.5 µA. A typical MLCC 33 nF, 25 V loop filter capacitor has approximately 0.5 nA of leakage (Murata GRM155R71E333KA88).

PRINTED CIRCUIT BOARD (PCB)

Use a sufficient number of via holes to connect the top and bottom ground planes (see Figure 23). The evaluation circuit board design is available from Analog Devices upon request.

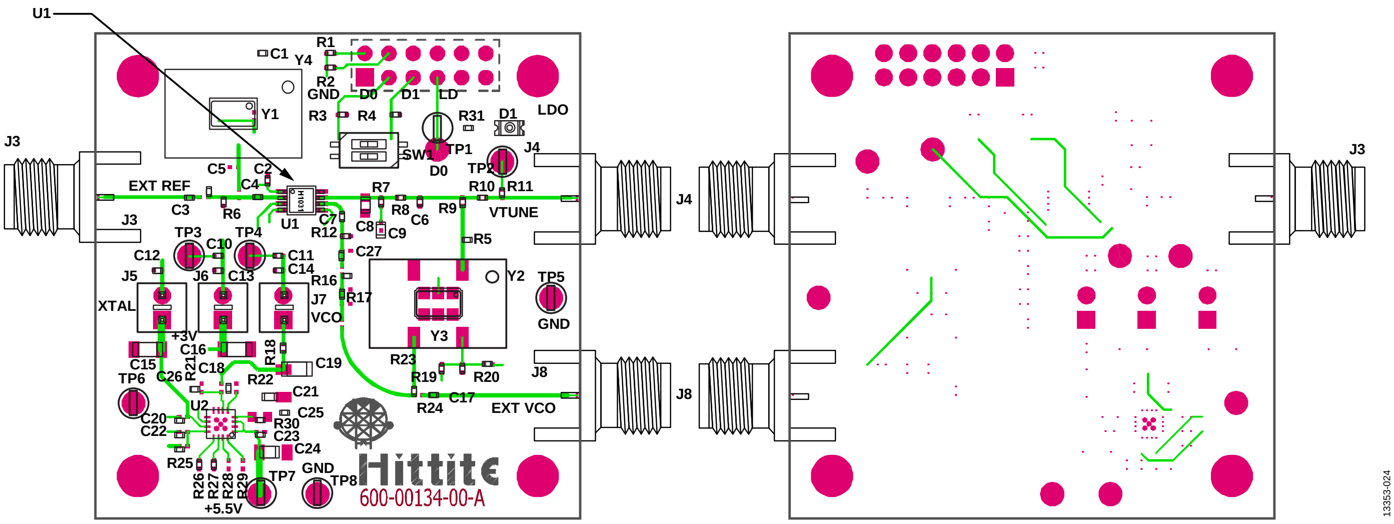
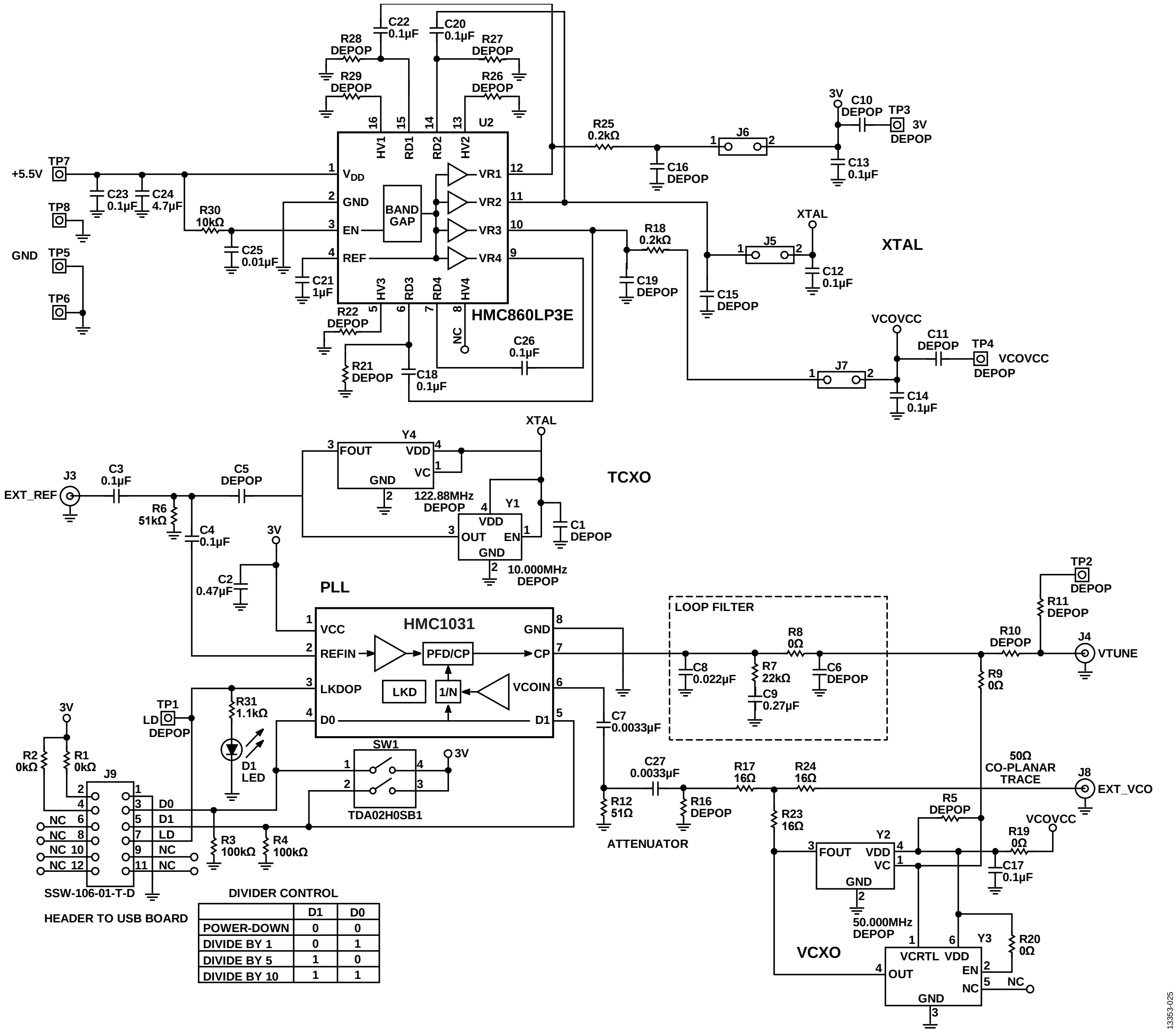


Figure 23. Evaluation PCB



	D1	D0
POWER-DOWN	0	0
DIVIDE BY 1	0	1
DIVIDE BY 5	1	0
DIVIDE BY 10	1	1

Figure 24. Evaluation PCB Schematic

Table 5. Loop Filter Configuration

Configuration	f_{REF} (MHz)	f_{VCO} (MHz)	Divider	Bandwidth (Hz)	C8	R7	C9
1	10	100	10	10	220 nF	7.5 kΩ	4.7 µF
2	10	50	5	100	100 nF	5.6 kΩ	1 µF
3	10	50	5	2000	300 pF	100 kΩ	3.9 nF

OUTLINE DIMENSIONS

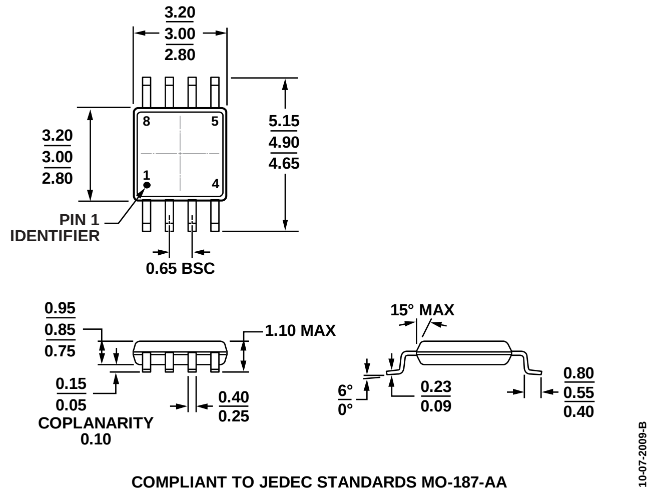


Figure 25. 8-Lead Mini Small Outline Package [MSOP]
(HRM-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding[2]
HMC1031MS8E	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	HRM-8-1	H1031 XXXX
HMC1031MS8ETR	−40°C to +85°C	8-Lead Mini Small Outline Package [MSOP]	HRM-8-1	H1031 XXXX
EVAL01-HMC1031MS8E		HMC1031MS8E Evaluation PCB		

[1] E = RoHS Compliant Part.
[2] XXXX is the four-digit lot number.

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