HMC1031MS8E

v00.0312

## CLOCK GENERATOR WITH INTEGER-N PLL
0.1 - 500 MHz

Typical Applications

• Low Jitter Clock Generation

• Low Bandwidth Jitter Attenuation

• Low Frequency PLL

• Frequency Translation

• OCXO Frequency Multiplier

• Phase Lock clean high frequency references to 10MHz equipment

Features

Low Current Consumption: <2 mA Typical

High Phase Frequency Detector Rate: 140 MHz

Hardware Pin Programmable Clock Multiplication Ratios: x1/ x5/ x10

Lock Detect Indicator

Power Down Mode (0.7 µA typical)

8 Lead MS8E Package: 4.8 mm x 3.0 mm

Functional Diagram
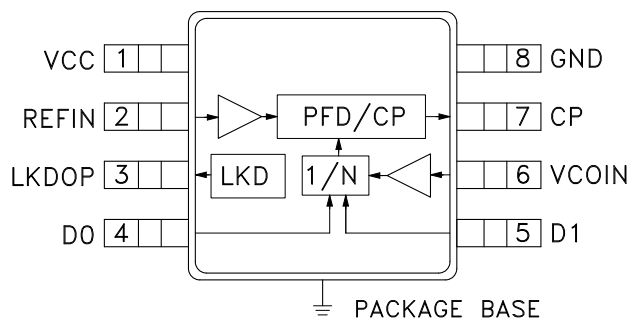
General Description

Together with an external loop filter and a VCXO, the HMC1031MS8E forms a complete clock generator solution targeted at low frequency jitter-cleaner and reference clock generation applications.

The HMC1031MS8E features a low power integer-N divider supporting divide ratios of 1/5/10, that is controlled via external hardware pins and requires no serial port.

The Integrated Phase Detector and Charge Pump are capable of operating up to 140 MHz, and a maximum VCXO input of 500 MHz ensure frequency compliance with a wide variety of system clocks and VCXOs.

Additional features include Integrated Lock Detect Indicator available on a dedicated hardware pin, and a built-in Power Down Mode.

The HMC1031MS8E is housed in a 8 lead MS8E SMT package.

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1

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CLOCK GENERATOR WITH INTEGER-N PLL
0.1 - 500 MHz

CLOCK GENERATORS - SMT

Electrical Specifications

T_A = +25 °C, VCC = 3.3 V, Unless Otherwise Specified.

Parameter	Conditions	Min	Typ	Max	Units
Power Supply Voltage		2.7	3.3	3.5	V
Operating Temperature		-40	27	85	°C
Reference Frequency	Externally AC coupled [1]			140	MHz
VCO Frequency				500	MHz
Charge Pump Current			50		µA
Input Voltage Swing (Reference & VCO Inputs) [2]	Exernally AC Coupled to the Chip.	0.1		3.5	Vpp
REF, VCO Input DC Bias	0.5*VCC approximately		1.65		V
Input Duty Cycle		40		60	%
Charge Pump Output Range			0.2 to VCC - 0.4 V Typically[3]		
Input Impedance at 50 MHz	Applicable to REF an VCO Input Pins.		3600‖4		Ω‖pF
Divide Ratios	VCO/VCXO Feedback Divider		1/5/10		

Phase Noise [4]
    Floor Figure of Merit
    Flicker Figure of Merit
	Divide-by 10	-212
		-254
			-208
			-252
				-204
				-248
					dBc/Hz
					dBc/Hz

Flicker Noise at f_{offset}	PN_{flick} = Flicker FOM +20log(f_{vcxo}) -10log(f_{offset})				dBc/Hz
Phase Noise Floor at f_{vcxo} with f_{pd}	PN_{floor} = Floor FOM + 10log(f_{pd}) +20log(f_{vcxo}/f_{pd})				dBc/Hz
Supply Current [5]	100 MHz REF=VCXO, 3.3 V VCC		1.95		mA
Power Down Current [6] [D0,D1 = 00]	3.0 V VCC, 25 °C 3.3 V VCC, 85 °C 3.6 V VCC, 85°C		0.05 0.8 1		uA uA uA
Lock Detect Output Current	CMOS Output Level			3	mA

[1] The lower limit of operation is limited by off-chip AC coupling. The size of the AC coupling should be chosen to have insignificant impedance relative to the 3.6kOhm input impedance of the part, and any termination impedances on the evaluation board (50Ohm by default).

[2]REF and VCO inputs should be AC coupled to HMC1031MS8E. Peak Input level should not exceed VCC+0.4 V with respect to GND.

[3] PLL may lock in the voltage range of 0.2 to VCC - 0.4 V. However, the charge pump gain may be reduced. See Figure 9 CP Compliance

[4] See Figure 15, 16 for addional Flicker FOM and Floor FOM data.

[5] See Figure 10 for additional supply current data. Base Frequency 100MHz, Base VCC: 3.3V, 0.8 to 1mA/V, Base PFD current: 1.8 mA, 8 µA/MHz Base DIV current: 1.15mA, 15 µA/MHz. For example, the device current for a 10 MHz ref and 50 MHz VCO at 3.0 V VCC can be calculated as PFD Current delta = (10-100)*8e-6 = -0.72, DIV current delta = (50-100)*15e-6=-0.75 mA, Device current = (1.8-0.72)+(1.15-0.75)=1.48 mA at 3.3V VCC   At 3 V VCC device current would be approx: 1.48 - 0.85e-3*(3.3-3.0) = 1.225 mA

[6] In Power down mode, the REF/VCO inputs and charge pump outputs are tri-stated. The power down leakage current is measured without any signal applied to HMC1031MS8E.

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2

CLOCK GENERATOR WITH INTEGER-N PLL
0.1 - 500 MHz

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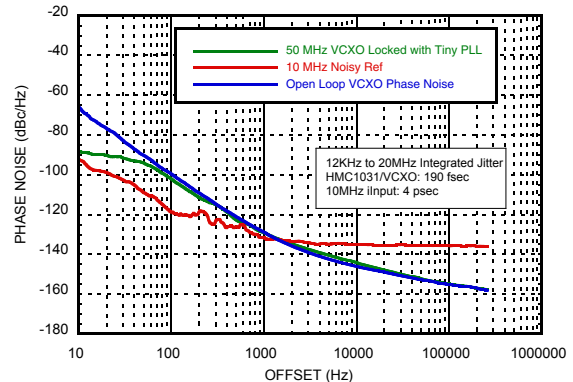
Typical Performance Characteristics

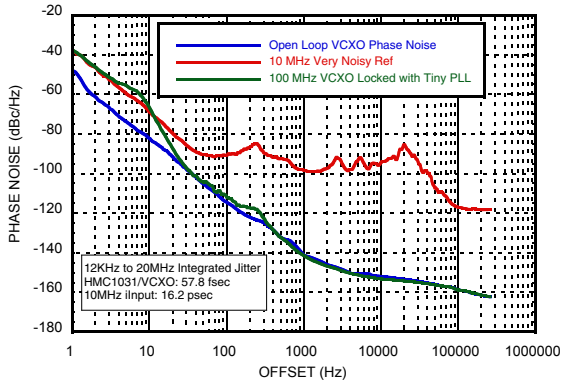T_A = +25 °C, VCC = 3.3 V, Unless Otherwise Specified.

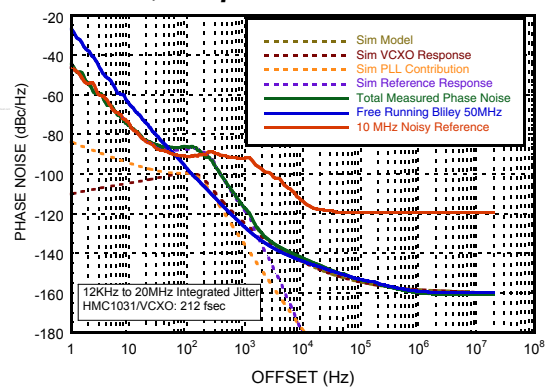**Figure 1. 10 MHz to 100 MHz with Noisy Reference Phase Noise** [1]
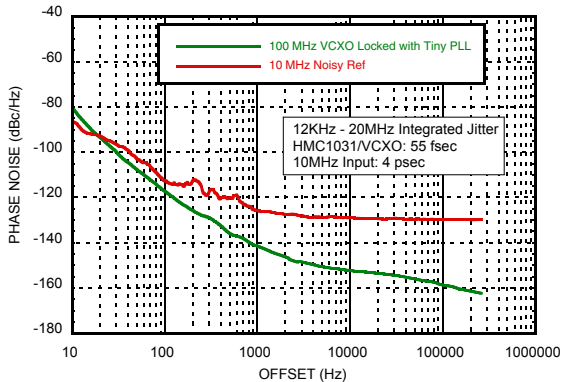
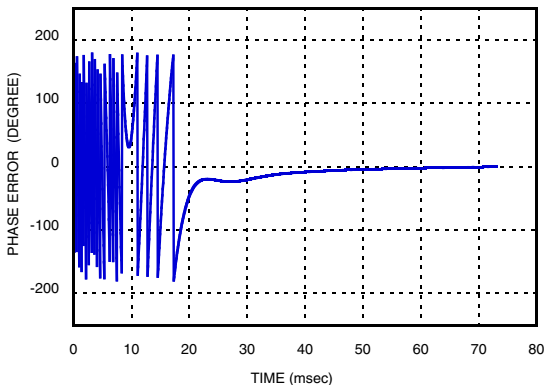**Figure 2. 10MHz to 50MHz with Noisy Reference Phase Noise** [1]

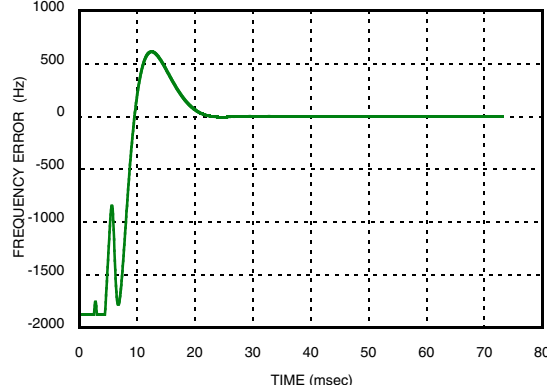**Figure 3. 10MHz to 100MHz with Very Noisy Reference Phase Noise** [1]

Figure 4. Typical Close Loop Phase Noise, HMC1031MS8E as Jitter Attenuator, Loop Bandwidth 100 Hz [1]

Figure 5. Phase Error during Lock Time for DIV 5, 10 MHz IN,50 MHz OUT, Loop Bandwidth 100 Hz [1]

Figure 6. Frequency Error during Lock Time for DIV 5, 10 MHz IN,50 MHz OUT, Loop Bandwidth 100 Hz [1]

[1] Loop Filter Value: C1 4.7 µF, R2 1.2 KΩ, C2 62 µF for Loop Filter bandwidth 8 Hz, VCXO: Crystek CVHD-950 100 MHz
[2] Loop Filter Value: C1 220 nF, R2 3.3 KΩ, C2 2.2 µF for Loop Filter bandwidth 50 Hz, VCXO: Bliley V105ACACB 50 MHz
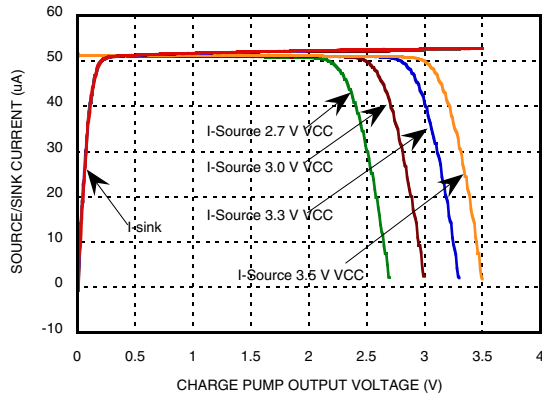[3] Loop Filter Value Refer to Loop Filter Configuration Table No 1. VCXO: Crystek CVHD-950 100MHz
[4] Loop Filter Value Refer to Loop Filter Configuration Table No 2. Simulated data is generated from Hittite PLL Design Software.
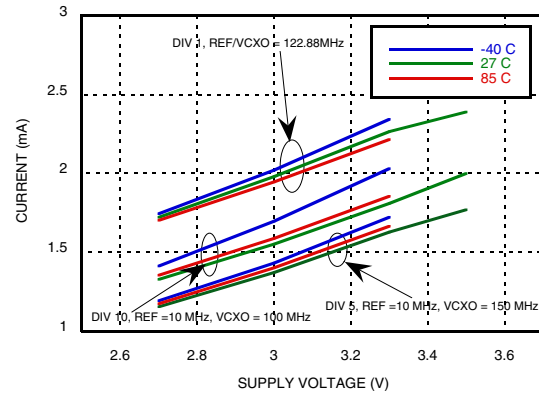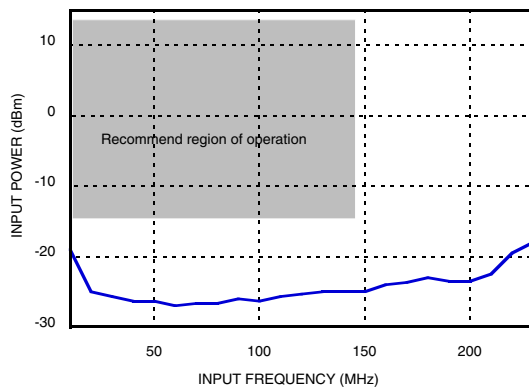
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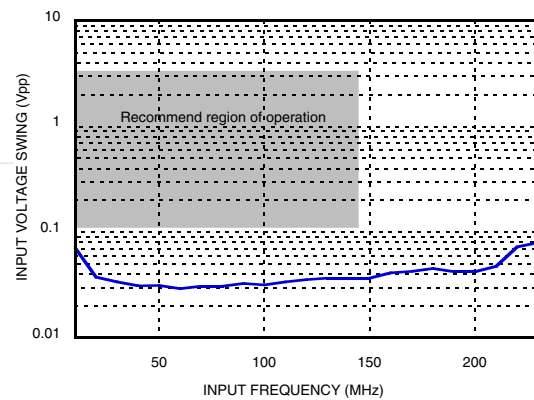### Figure 7. Typical Charge Pump Output Source and Sink Current vs. Output Voltage

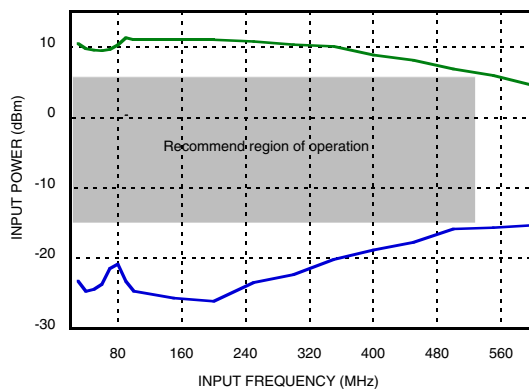### Figure 8. HMC1031MS8E Current vs. Different Config

Figure 9. HMC1031MS8E REF Input Sensitivity vs. Frequency [1]

Figure 10. HMC1031MS8E REF Input Sensitivity vs. Frequency [4]

Figure 11. HMC1031MS8E VCO Input Sensitivity vs. Frequency [5]

Figure 12. HMC1031MS8E VCO Input Sensitivity vs. Frequency [5]
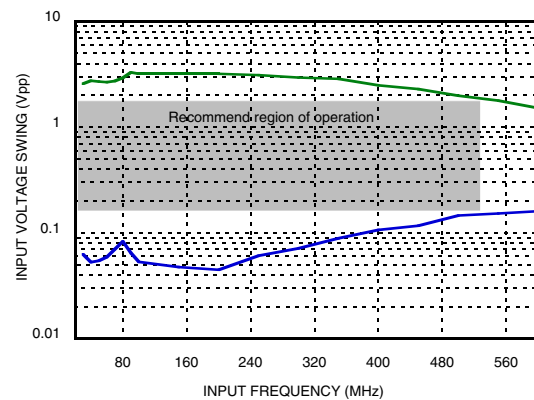
[5] Maximum frequency is guaranteed in the recommended region of operation across temperature and process variation.

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4

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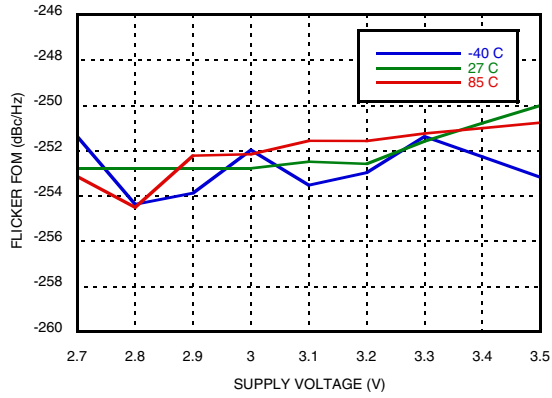CLOCK GENERATORS - SMT

Figure 13. HMC1031MS8E Flicker FOM

Figure 14. HMC1031MS8E Floor FOM

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RoHS ✓
EARTH FRIENDLY
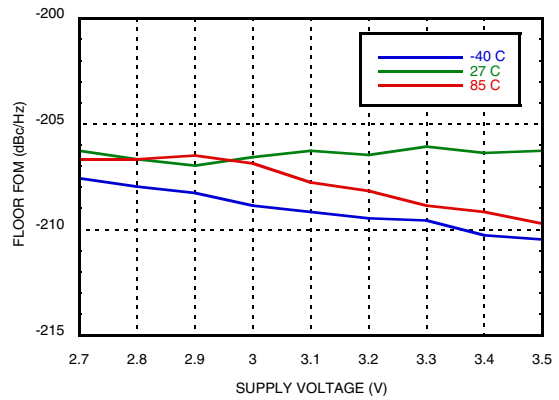
Absolute Maximum Ratings

VCC to GND	- 0.3 V to 3.6 V
D0, D1 pins to GND	-0.3 V to 3.6 V
Maximum REF input voltage	VCC + 0.4 V
Maximum VCO input voltage	VCC + 0.4 V
Maximum Junction Temperature	+125 °C
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
Thermal Resistance	0.2 °C/mW

Reflow Soldering
   Peak Temperature
   Time at Peak Temperature
	+260 °C
	40 seconds

ESD Sensitivity (HBM)	Class 2

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The absolute maximum ratings apply individually only and not in combination.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing
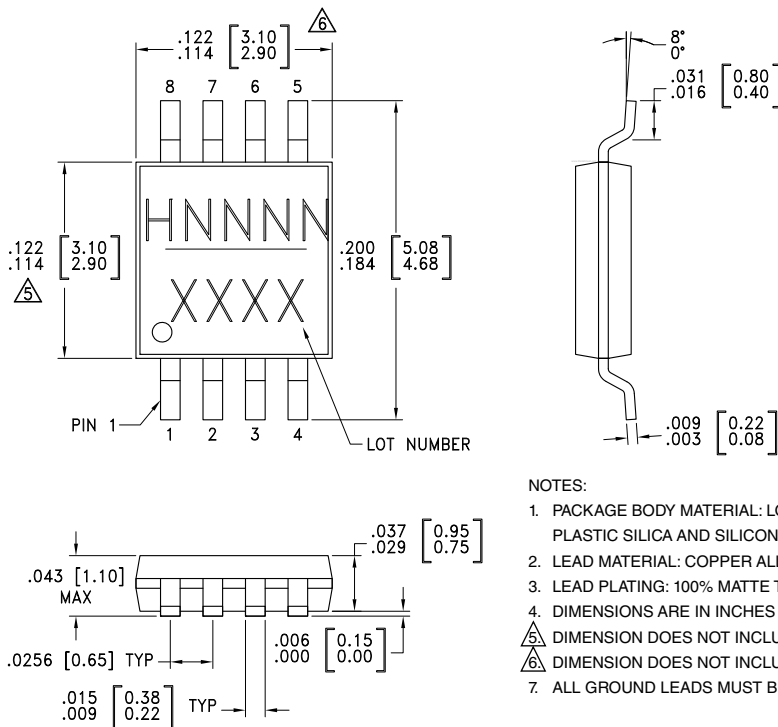
NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD MATERIAL: COPPER ALLOY
3. LEAD PLATING: 100% MATTE TIN
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
6. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
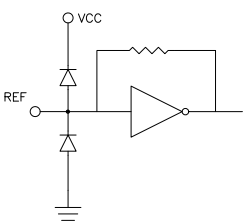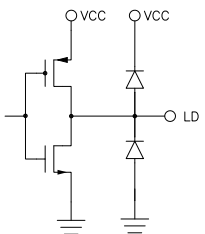7. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
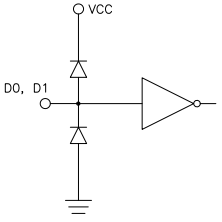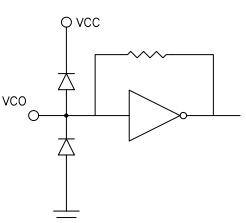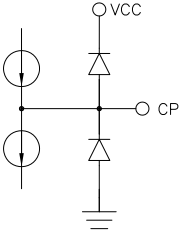
Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC1031MS8E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	1031 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

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6

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Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	VCC	Supply voltage Typical +3.3 V	
2	REFIN	Reference input, externally AC coupled reference frequency input	
3	LKDOP	Lock Detect output, CMOS drive	
4, 5	D0, D1	CMOS inputs used to specify integer-N division ratio	
6	VCOIN	VCO input, AC coupled VCO/VCXO input	
7	CP	Charge Pump output	
8	GND		

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Evaluation PCB
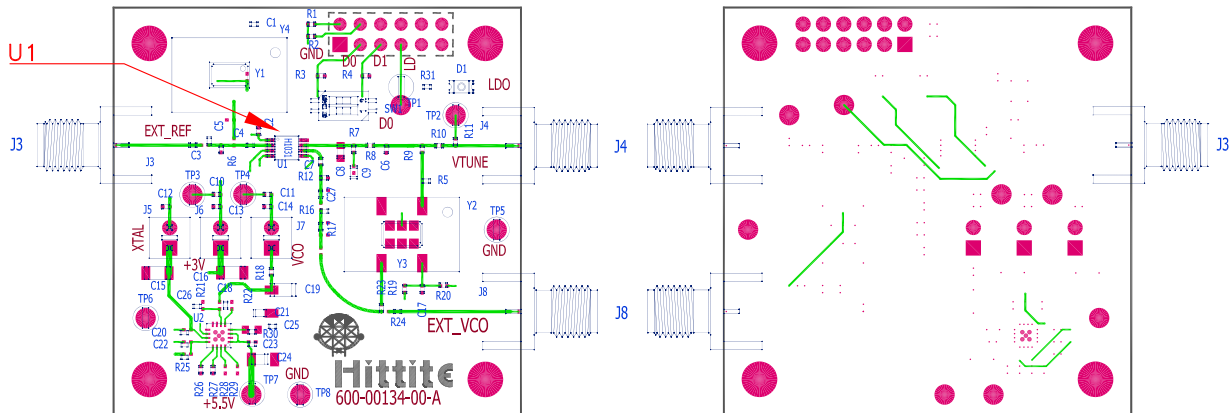
A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC1031MS8E Evaluation PCB	EVAL01-HMC1031MS8E

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8

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CLOCK GENERATORS - SMT

Evaluation PCB Schematic

Frequency Multiplication Truth Table

HMC1031MS8E Pins [Set by SW1 in Evaluation PCB Schematic]		PLL Feedback Division Ratio (N)
D0	D1	
0	0	Power Down Mode
1	0	1
0	1	5
1	1	10

Loop Filter Configuration Table

No.	Fref [MHz]	Fvco [MHz]	Div	BW [Hz]	C8	R7	C9
1	10	100	10	10	220 nF	7.5 kΩ	4.7 uF
2	10	50	5	100	100 nF	5.6 kΩ	1 uF
3	10	50	5	2k	300 pF	100 kΩ	3.9 nF

To view the Eval PCB Schematic please visit www.hittite.com and choose HMC1031MS8E from the "Search by Part Number" pull down menu.

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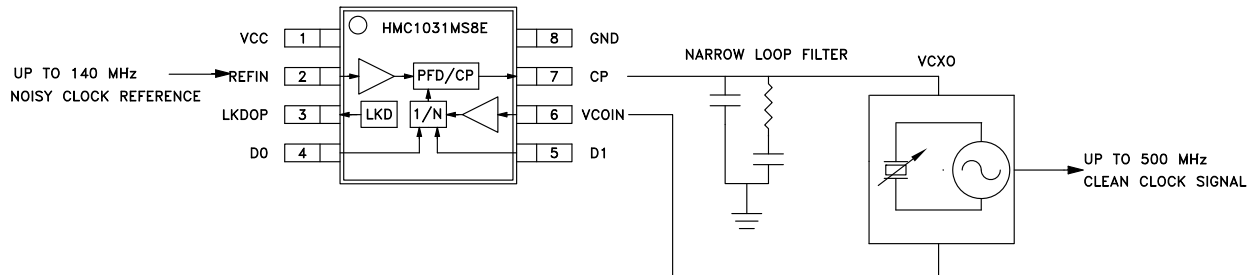
HMC1031MS8E Application Information

Figure 15. HMC1031MS8E Application Diagram

Jitter Attenuation

In some cases, reference clocks to the system may come from external noisy sources with high jitter. The HMC1031MS8E may be used to attenuate this incoming jitter and distribute a clean clock in the system. In such a scheme, a narrow loop filter is selected for the HMC1031MS8E. The device frequency locks to the external VCXO but the reference jitter is attenuated as defined by the set loop filter bandwidth. The final output frequency and phase noise characteristics outside the loop bandwidth is defined by the phase noise characteristics of the VCXO used. A low jitter clock reference yields better clocking performance, better LO performance of RF PLLVCOs, and improves the SNR performance of data converters (ADC/DAC).

Frequency Translation

Quite often, the reference clock in a Test & Measurement or a Communications system is a high accuracy OCXO (Oven Controlled Crystal Oscillator) with excellent long-term stability. The HMC1031MS8E may find applications when the OCXO frequency needs to be multiplied up to a higher rate to drive the primary clock inputs in a system. The device offers a very low power, small package and high performance method to multiply its incoming frequency in x1, x5 and x10 rates. Such multiplication is needed because the higher reference clocks improve Phase Noise, ADC/DAC SNR, clock generator jitter and PHY BERs. In this scheme, the HMC1031MS8E may be connected to an external low cost VCXO (e.g. at 50MHz or 100MHz), and lock this external VCXO to the excellent long-term stability of the OCXO.

Loop Bandwidths with HMC1031MS8E

In typical jitter attenuation applications, an incoming reference clock is frequency locked with a narrow PLL Loop Bandwidth such that its incoming noise is filtered out by the PLL and VCXO combination. The out of band phase noise of the PLL follows the VCXO that it's locked to. A narrow PLL loop bandwidth ensures that the output jitter is determined by the VCXO (or any other type of high quality factor VCO) and not affected by the spectral noise of the incoming clock beyond the set loop bandwidth.

Considering that the HMC1031MS8E will be used in narrow loop filter bandwidth configurations, the device is designed to have a low charge pump current of 50uA. This architecture offers advantages in low power consumption and loop filter design. Typically, narrow loop filter bandwidths require large filter capacitors. Thanks to the low charge pump current design of the HMC1031MS8E, smaller loop filter capacitor sizes may be used to implement narrow loop filters. It should be kept in mind that the HMC1031MS8E is designed to operate in only a few kHz loop bandwidths in its widest-loop bandwidth configuration.

Using VCO/VCXO's with Negative Tuning Slope

In its normal configuration, HMC1031MS8E will work with any VCO/VCXO that has a positive tuning slope. For any VCO/VCXO with negative tuning slope i.e where frequency decreases with increasing tuning voltage, the loop filter AC ground should be connected to VCC instead of GND.

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10