4 W, GaAs, pHEMT, MMIC Power Amplifier, 5.5 GHz to 8.5 GHz

Data Sheet **HMC1121**

FEATURES

- High saturated output power (P_{SAT}): 36.5 dBm at 30% power added efficiency (PAE)
- High output third-order intercept (IP3): 44 dBm typical
- High gain: 28 dB typical
- High output power for 1 dB compression (P1dB): 36 dBm typical
- Total supply current: 2200 mA at 7 V
- 40-lead, 6 mm × 6 mm LFCSP package: 36 mm^2

APPLICATIONS

- Point to point radios
- Point to multipoint radios
- Very small aperture terminals (VSATs) and satellite communications (SATCOMs)
- Military electronic warfare (EW) and electronic counter measures (ECM)

FUNCTIONAL BLOCK DIAGRAM

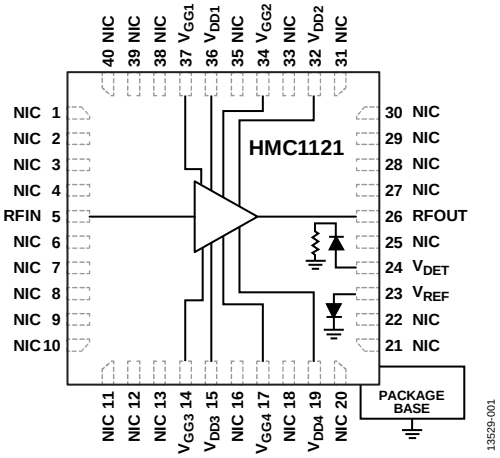

Figure 1.

GENERAL DESCRIPTION

The HMC1121 is a three-stage, gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), 4 W power amplifier with an integrated temperature compensated on-chip power detector that operates between 5.5 GHz and 8.5 GHz. The HMC1121 provides 28 dB of gain, 44 dBm output IP3, and 36.5 dBm of saturated output power at 30% PAE from a 7 V power supply.

The HMC1121 exhibits excellent linearity and it is optimized for high capacity, point to point and point to multipoint radio systems. The amplifier configuration and high gain make it an excellent candidate for last stage signal amplification preceding the antenna.

Ideal for supporting higher volume applications, the HMC1121 is provided in a 40-lead LFCSP package.

Rev. A

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REVISION HISTORY

10/2017—Rev. 0 to Rev. A

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Updated Outline Dimensions 15
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7/2016—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, V_{DD} = V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = 7 V, I_{DD} = 2200 mA, frequency range = 5.5 GHz to 7.5 GHz.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		5.5		7.5	GHz	
GAIN		24	27		dB	
Gain Variation over Temperature			0.01		dB/°C	
RETURN LOSS						
Input			17		dB	
Output			13		dB	
OUTPUT POWER						
For 1 dB Compression	P1dB	35	36		dBm	36 dBm = 4 W
Saturated	P_{SAT}		36.5		dBm	At 30% PAE
OUTPUT THIRD-ORDER INTERCEPT	IP3		44		dBm	Measurement taken at P_{OUT}/tone = 28 dBm
SUPPLY						
Voltage	V_{DD}	5		7.5	V	
Total Current	I_{DD}		2200		mA	Adjust the gate control voltage (V_{GG1} to V_{GG4}) between −2 V to 0 V to achieve an I_{DD} = 2200 mA typical

T_A = 25°C, V_{DD} = V_{DD1} = V_{DD2} = V_{DD3} = V_{DD4} = 7 V, I_{DD} = 2200 mA, frequency range = 7.5 GHz to 8.5 GHz.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		7.5		8.5	GHz	
GAIN		25	28		dB	
Gain Variation over Temperature			0.009		dB/°C	
RETURN LOSS						
Input			15		dB	
Output			13		dB	
OUTPUT POWER						
For 1 dB Compression	P1dB	35	36		dBm	36 dBm = 4 W
Saturated	P_{SAT}		36.5		dBm	At 30% PAE
OUTPUT THIRD-ORDER INTERCEPT	IP3		43		dBm	Measurement taken at P_{OUT}/tone = 28 dBm
SUPPLY						
Voltage	V_{DD}	5		7.5	V	
Total Current	I_{DD}		2200		mA	Adjust the gate control voltage (V_{GG1} to V_{GG4}) between −2 V to 0 V to achieve an I_{DD} = 2200 mA typical

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Drain Voltage Bias	8 V
RF Input Power (RFIN)[1]	24 dBm
Channel Temperature	175°C
Continuous Power Dissipation, P_{DISS} (T_A = 85°C, Derate 227 mW/°C Above 85°C)	20.5 W
Thermal Resistance (R_{TH}) Junction to Ground Paddle	4.4°C/W
Maximum Peak Reflow Temperature (MSL3)[2]	260°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
ESD Sensitivity (Human Body Model)	Class 1A, passed 250 V

[1] The maximum input power (P_{IN}) is limited to 24 dBm or to the thermal limits constrained by the maximum power dissipation.
[2] See the Ordering Guide section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

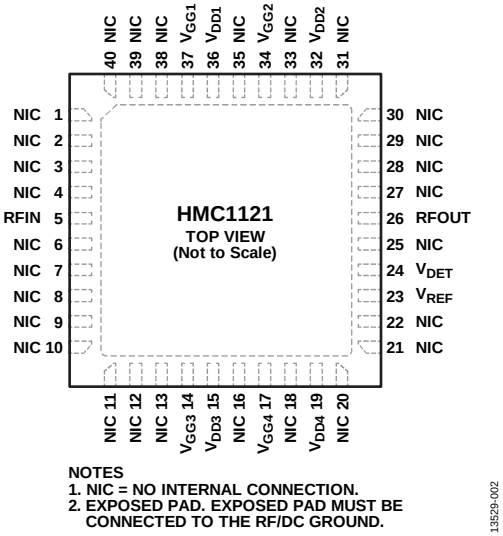


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 4, 6 to 13, 16, 18, 20 to 22, 25, 27 to 31, 33, 35, 38 to 40	NC	No Internal Connection. These pins and exposed ground pad must be connected to RF/dc ground.
5	RFIN	RF Input. This pin is ac-coupled and matched to 50 Ω. See Figure 3 for the RFIN interface schematic.
14, 17, 34, 37	V_{GG3}, V_{GG4}, V_{GG2}, V_{GG1}	Gate Controls for the Amplifier. Adjust V_{GG1} through V_{GG4} to achieve the recommended bias current. External bypass capacitors of 100 pF, 10 nF, and 4.7 µF are required. See Figure 5 for the V_{GG1} to V_{GG4} interface schematic.
15, 19, 32, 36	V_{DD3}, V_{DD4}, V_{DD2}, V_{DD1}	Drain Biases for the Amplifier. External bypass capacitors of 100 pF, 10 nF, and 4.7 µF are required. See Figure 8 for the V_{DD1} to V_{DD4} interface schematic.
23	V_{REF}	Voltage Reference. This pin is the dc bias of the diode biased through the external resistor and is used for the temperature compensation of V_{DET}. See Figure 7 for the V_{REF} interface schematic.
24	V_{DET}	Voltage Detection. This pin is the dc voltage representing the RF output power rectified by the diode that is biased through an external resistor. See Figure 4 for the V_{DET} interface schematic.
26	RFOUT	RF Output. This pin is ac-coupled and matched to 50 Ω. See Figure 6 for the RFOUT interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS

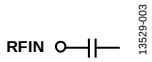


Figure 3. RFIN Interface Schematic

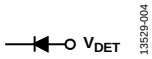


Figure 4. V_{DET} Interface Schematic

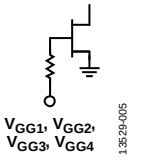


Figure 5. V_{GG1} to V_{GG4} Interface Schematic

Figure 6. RFOUT Interface Schematic

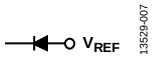


Figure 7. V_{REF} Interface Schematic

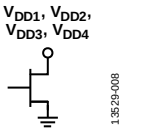


Figure 8. V_{DD1} to V_{DD4} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

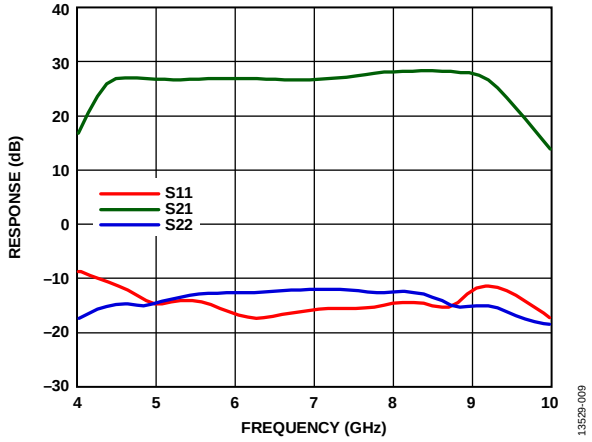


Figure 9. Response (Broadband Gain and Return Loss) vs. Frequency for S21, S11, and S22

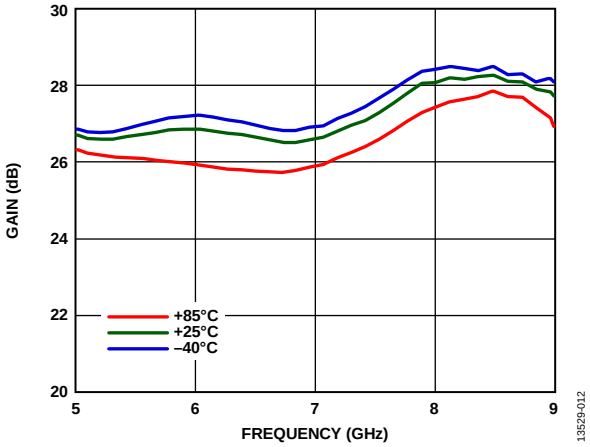


Figure 12. Gain vs. Frequency at Various Temperatures

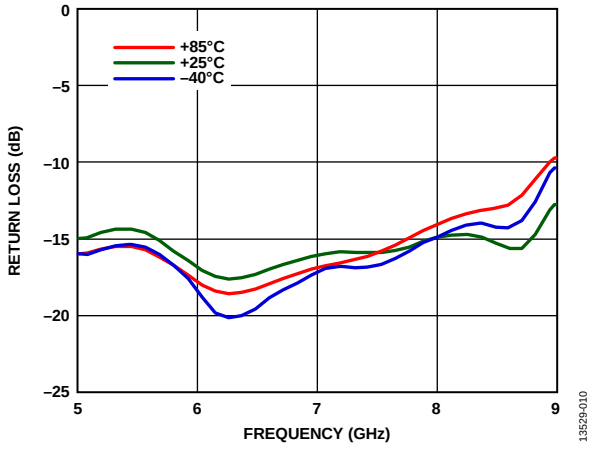


Figure 10. Input Return Loss vs. Frequency at Various Temperatures

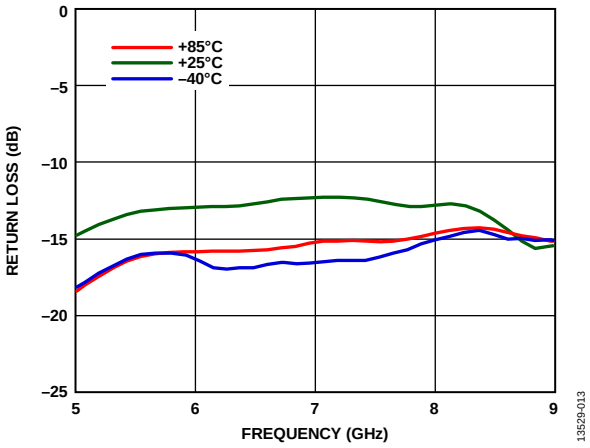


Figure 13. Output Return Loss vs. Frequency at Various Temperatures

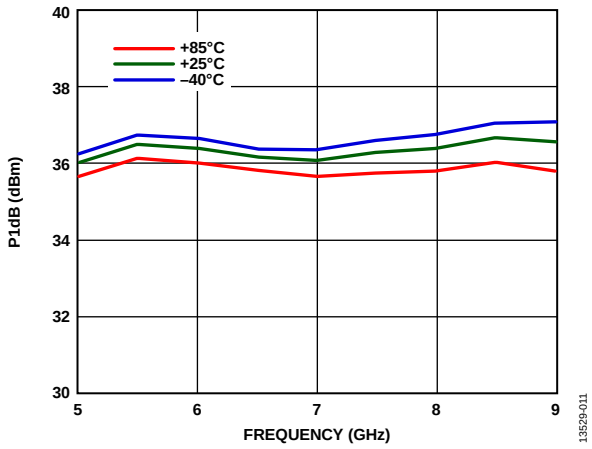


Figure 11. P1dB vs. Frequency at Various Temperatures

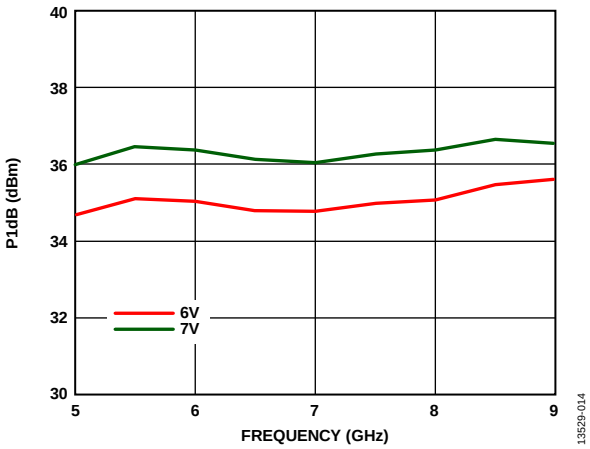


Figure 14. P1dB vs. Frequency at Various Supply Voltages

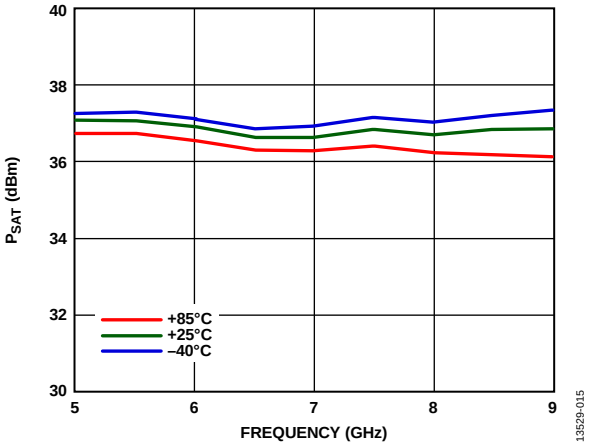


Figure 15. P_{SAT} vs. Frequency at Various Temperatures

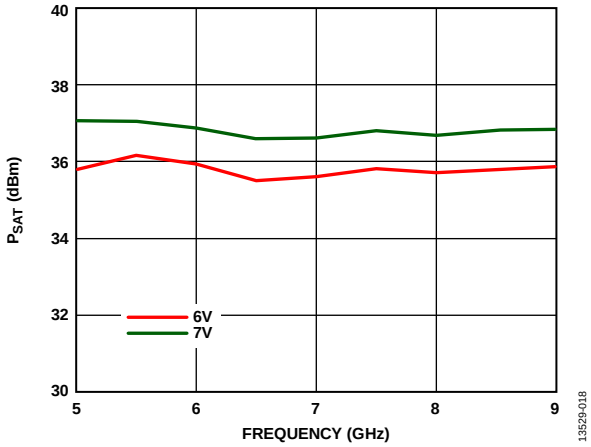


Figure 18. P_{SAT} vs. Frequency at Various Supply Voltages

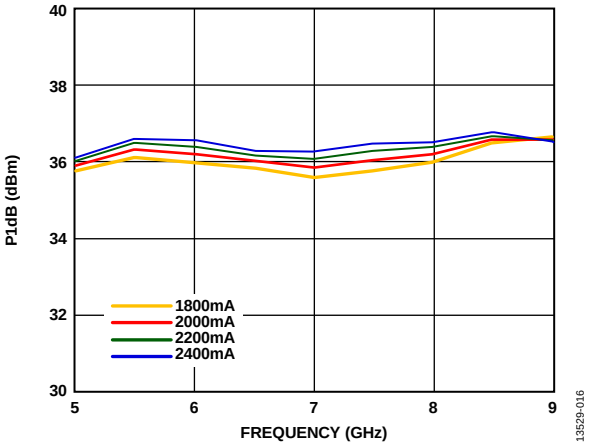


Figure 16. P1dB vs. Frequency at Various Supply Currents (I_{DD})

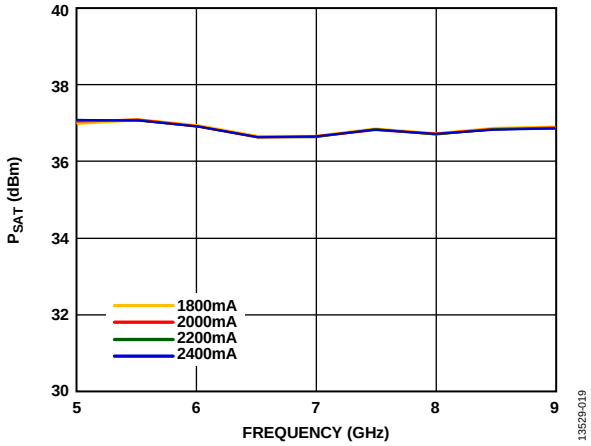


Figure 19. P_{SAT} vs. Frequency at Various Supply Currents (I_{DD})

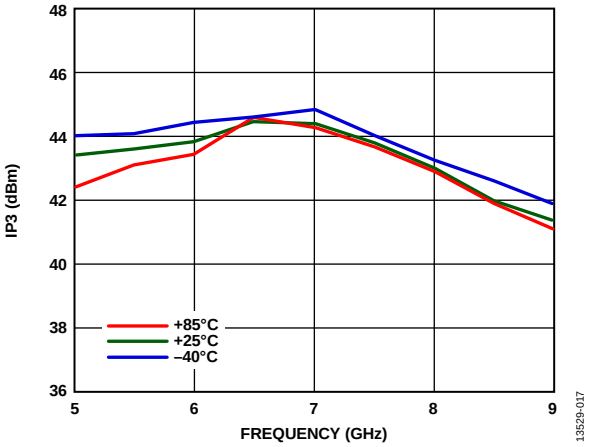


Figure 17. Output IP3 vs. Frequency at Various Temperatures, P_{OUT}/Tone = 28 dBm

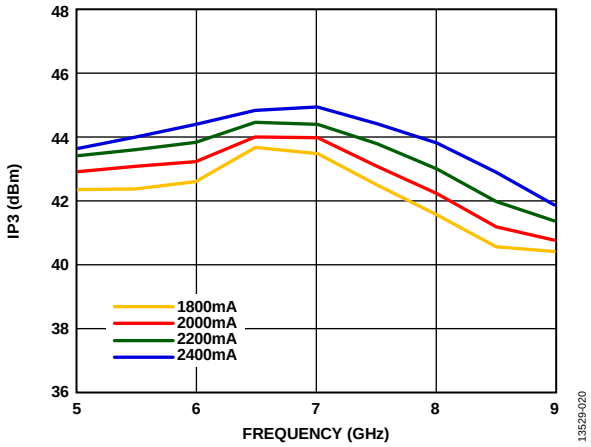


Figure 20. Output IP3 vs. Frequency at Various Supply Currents, P_{OUT}/Tone = 28 dBm

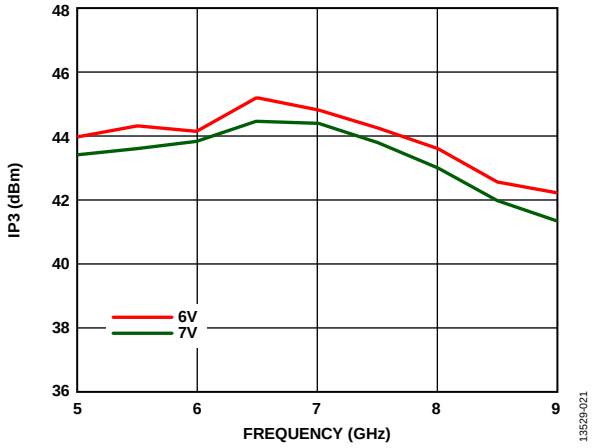


Figure 21. Output IP3 vs. Frequency at Various Supply Voltages, P_{OUT}/Tone = 28 dBm

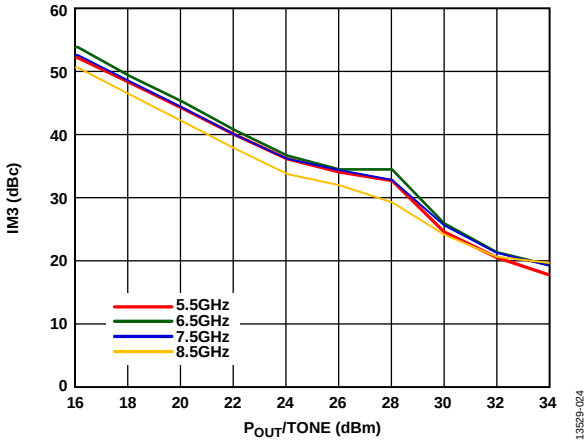


Figure 24. Output IM3 vs. P_{OUT}/Tone at V_{DD} = 6 V

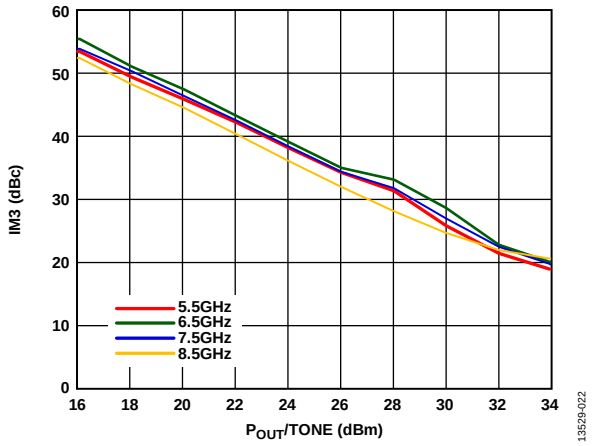


Figure 22. Output Third-Order Intermodulation (IM3) vs. P_{OUT}/Tone at V_{DD} = 7 V

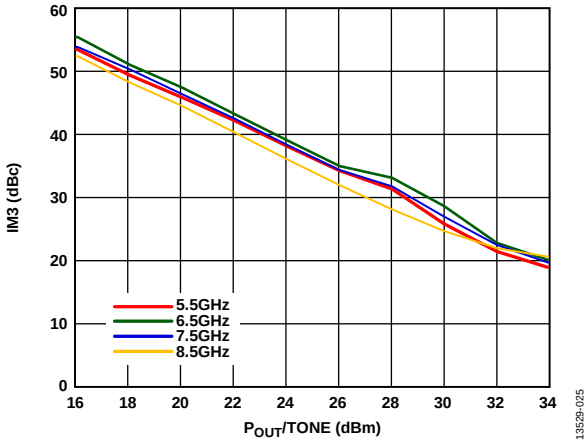


Figure 25. Output IM3 vs. P_{OUT}/Tone at V_{DD} = 8 V

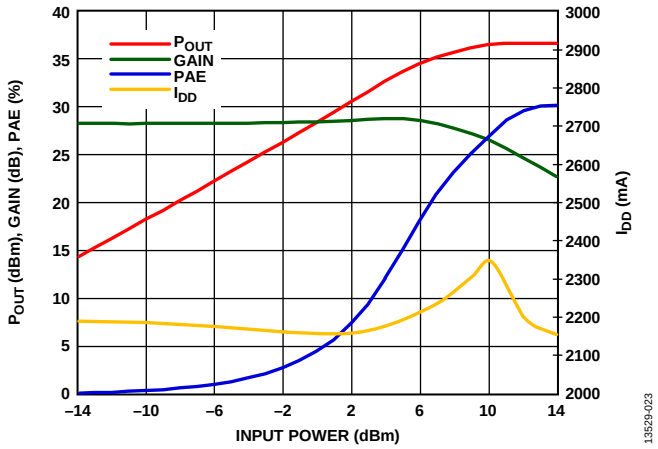


Figure 23. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at 7 GHz

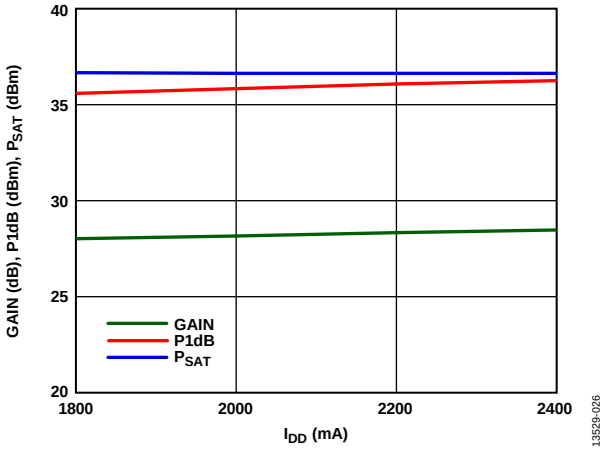


Figure 26. Gain, P1dB, and P_{SAT} vs. Supply Current (I_{DD}) at 7 GHz

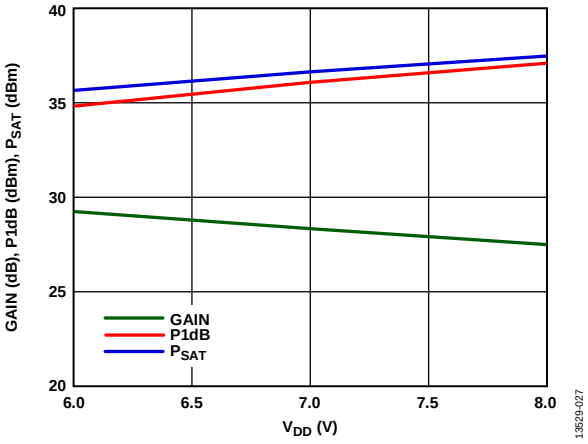


Figure 27. Gain, P1dB, and P_{SAT} vs. Supply Voltage (V_{DD}) at 7 GHz

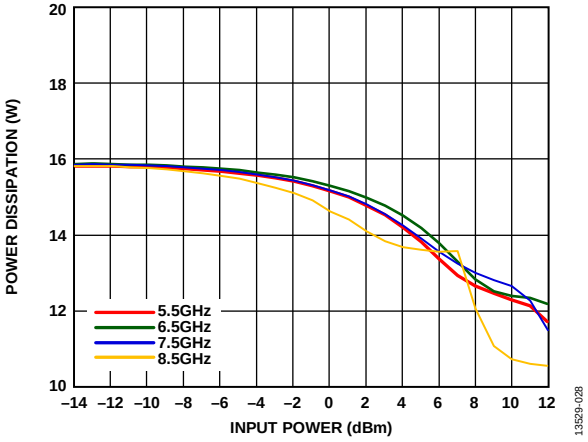


Figure 28. Power Dissipation vs. Input Power at T_A = 85°C

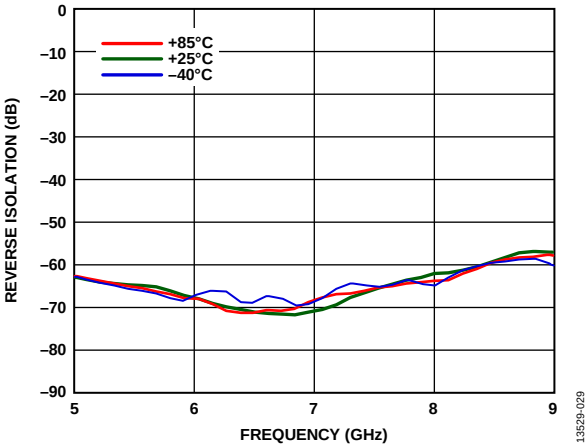


Figure 29. Reverse Isolation vs. Frequency at Various Temperatures

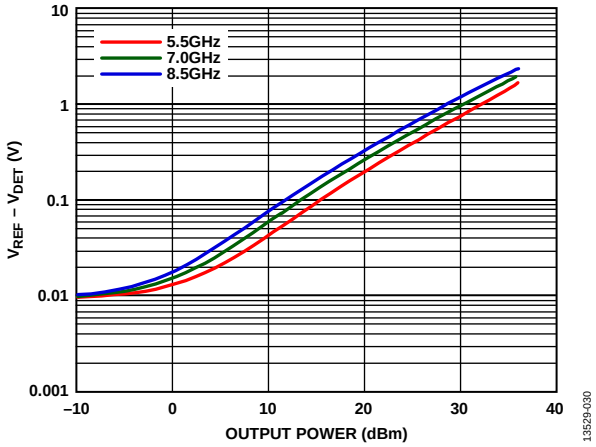


Figure 30. Detector Voltage ($V_{REF} - V_{DET}$) vs. Output Power at Various Frequencies

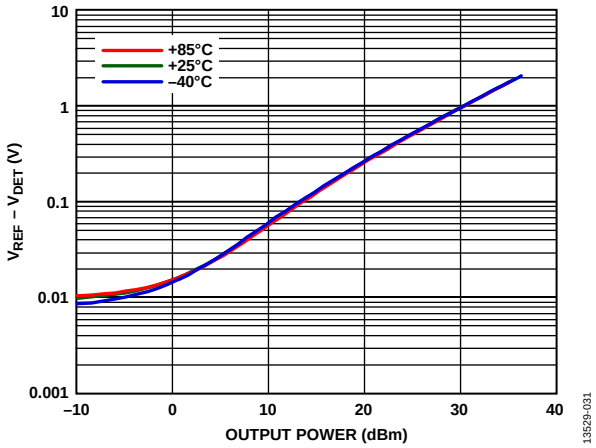


Figure 31. Detector Voltage ($V_{REF} - V_{DET}$) vs. Output Power at Various Temperatures, at 7 GHz

THEORY OF OPERATION

The HMC1121 is a three-stage, GaAs, pHEMT, MMIC, 4 W power amplifier consisting of three gain stages in series. A simplified block diagram is shown in Figure 32. The input signal is divided evenly into two; each of these two paths are amplified through three independent gain stages. The amplified signals are then combined at the output.

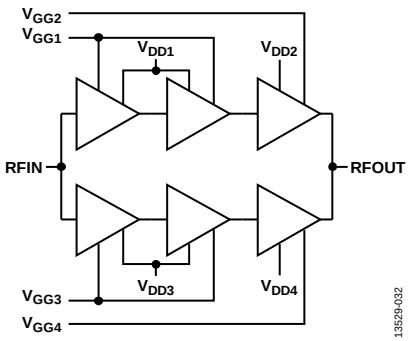


Figure 32. Simplified Block Diagram

The HMC1121 has single-ended input and output ports whose impedances are nominally matched to 50 Ω internally over the 5.5 GHz to 8.5 GHz frequency range. Consequently, it can directly insert into a 50 Ω system without the need for impedance matching circuitry. In addition, multiple HMC1121 amplifiers can be cascaded back to back without the need of external matching circuitry. Similarly, multiple HMC1121 amplifiers can be used with power dividers at the input and power combiners at the output to obtain higher output power levels.

The input and output impedances are sufficiently stable vs. variations in temperature and supply voltage that no impedance matching compensation is required.

It is critical to supply very low inductance ground connections to the ground pins as well as to the backside exposed pad to ensure stable operation.

To ensure the best performance out of the HMC1121, do not exceed the absolute maximum ratings.

APPLICATIONS INFORMATION

Figure 33 shows the basic connections for operating the HMC1121 and also see the Theory of Operation section for additional information. The RF input and RF output are ac-coupled by the internal dc block capacitors.

RECOMMENDED BIAS SEQUENCE

Follow the recommended bias sequencing to avoid damaging the amplifier.

During Power-Up

The recommended bias sequence during power-up is the following:

1. Connect to ground.
2. Set V_{GGx} to −2 V.
3. Set V_{DDx} to 7 V.
4. Increase V_{GGx} to achieve a typical I_{DD} = 2200 mA.
5. Apply the RF signal.

During Power-Down

The recommended bias sequence during power-down is the following:

1. Turn the RF signal off.
2. Decrease V_{GGx} to −2 V to achieve a typical I_{DD} = 0 mA.
3. Decrease V_{DDx} to 0 V.
4. Increase V_{GGx} to 0 V.

The bias conditions previously listed (V_{DDx} = 7 V, I_{DD} = 2200 mA), are the recommended operating point to acheive optimum performance. The data used in this datasheet is taken with the recommended bias conditions. When using the HMC1121 with different bias conditions, different performance may result than what is shown in the Typical Performance Characteristics section.

The V_{DET} and V_{REF} pins are the output pins for the internal power detector. The V_{DET} pin is the dc voltage output pin that represents the RF output power rectified by the internal diode, which is biased through an external resistor.

The V_{REF} pin is the dc voltage output pin that represents the reference diode voltage, which is biased through an external resistor. This voltage is then used to compensate for the temperature variation effects on both diodes. A typical circuit is shown in the Typical Application Circuit section that reads out the output voltage and represents the RF output power is shown in Figure 33.

TYPICAL APPLICATION CIRCUIT

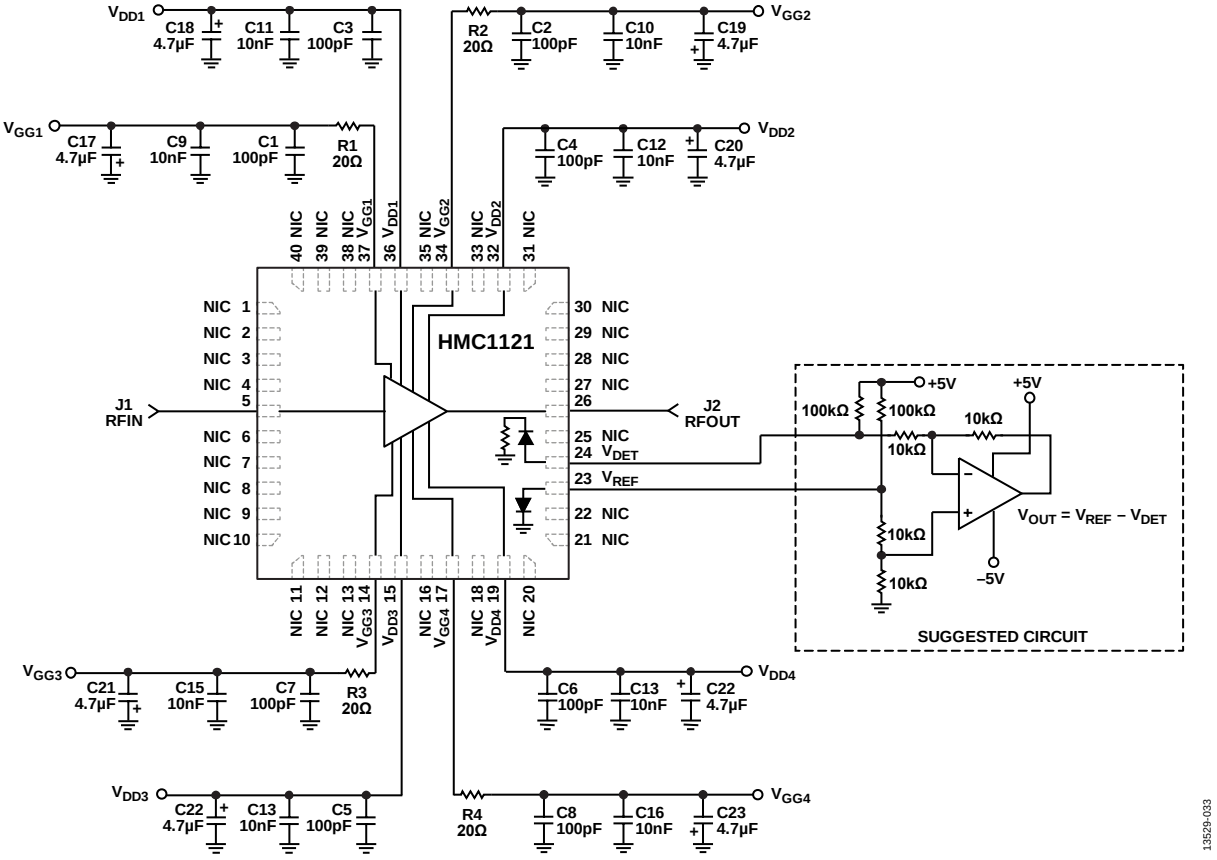


Figure 33. Typical Application Circuit

EVALUATION BOARD

The HMC1121 evaluation printed circuit board (PCB) is a 2-layer board that was fabricated using a Rogers 4350 and best practices for high frequency RF design. The RF input and RF output traces have a 50 Ω characteristic impedance. The PCB is attached to a heat sink by a SN96 solder, which provides a low thermal resistance path. Components are mounted using SN63 solder, allowing rework of the surface-mount components without compromising the circuit board to heat sink attachment.

The evaluation PCB and populated components operate over the −40°C to +85°C ambient temperature range. During operation, attach the evaluation PCB to a temperature controlled plate to control the temperature. For proper bias sequence, see the Applications Information section.

See Figure 35 for the HMC1121 evaluation board schematic. A fully populated and tested evaluation board, which is shown in Figure 34, is available from Analog Devices, Inc., upon request.

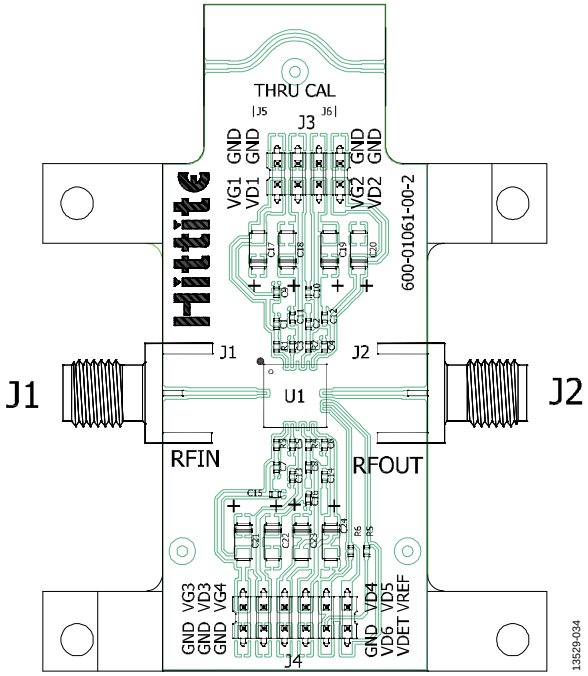


Figure 34. HMC1121 Evaluation Board

BILL OF MATERIALS

Table 5.

Item	Description
J1, J2	PCB mount SMA RF connector, Johnson PN 142-07010851
J3, J4	DC pins
J5, J6	RF connectors for thru line; not populated
C1 to C8	100 pF capacitors, 0402 package
C9 to C16	10 nF capacitors, 0402 package
C17 to C24	4.7 µF capacitor, Case A
R1 to R4	20 Ω resistors, 0402 package
R5, R6	100 kΩ resistors, 0402 package
U1	HMC1121LP6GE
Heat sink	Used for thermal transfer from the HMC1121LP6GE amplifier
PCB	600-01061-00 evaluation board; circuit board material: Rogers 4350

EVALUATION BOARD SCHEMATIC

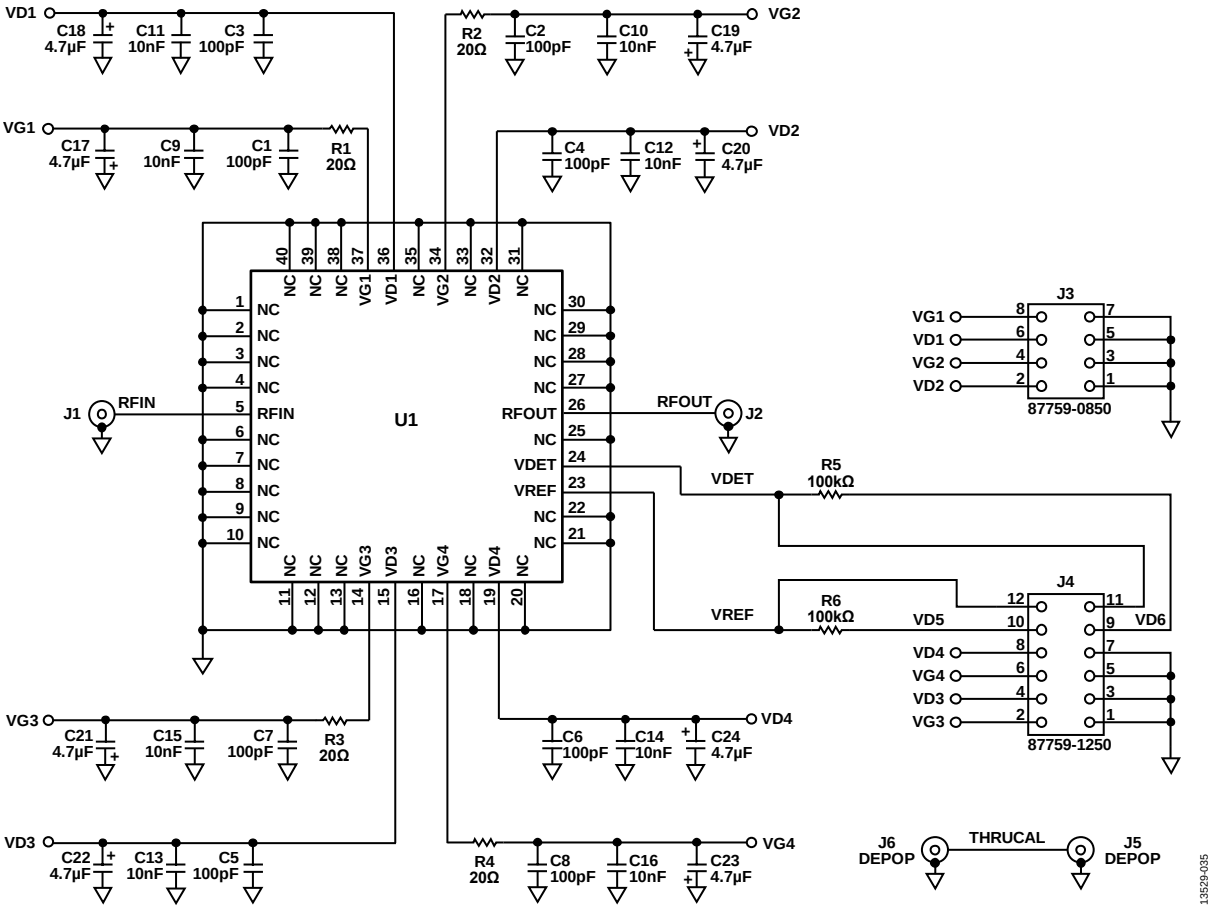
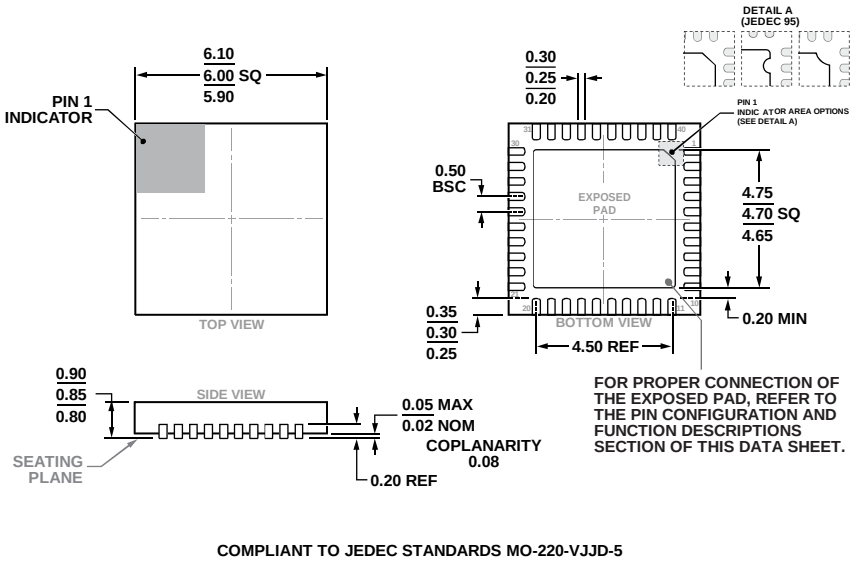


Figure 35. HMC1121 Evaluation Board Schematic

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-5

Figure 36. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.85 mm Package Height
(HCP-40-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature	MSL Rating[2]	Package Description[3]	Package Option
HMC1121LP6GE	−40°C to +85°C	MSL3	40-Lead Lead Frame Chip Scale Package [LFCSP]	HCP-40-1
HMC1121LP6GETR	−40°C to +85°C	MSL3	40-Lead Lead Frame Chip Scale Package [LFCSP]	HCP-40-1
EV1HMC1121LP6G			Evaluation Board	

[1] The HMC1121LP6GE and the HMC1121LP6GETR are RoHS-Compliant Parts.
[2] See the Absolute Maximum Ratings section for additional details.
[3] The HMC1121LP6GE and the HMC1121LP6GETR are low stress injection molded plastic and their lead finish is 100% matte Sn.