

v02 0316

HBT DIGITAL PHASE FREQUENCY DETECTOR 10 - 1300MHz

## **Typical Applications**

The HMC3716LPE is ideal for:

- Point-to-Point Radios
- Satellite Communication Systems
- Military Applications
- Sonet Clock Generation

#### Features

Ultra Low SSB Phase Noise Floor: -153dBc/Hz @ 10kHz offset @ 100MHz Integrated Output Resistors Improved Input Sensitivity Lock Detect and Invert Functionality 24-Pin 4 x 4mm SMT Package

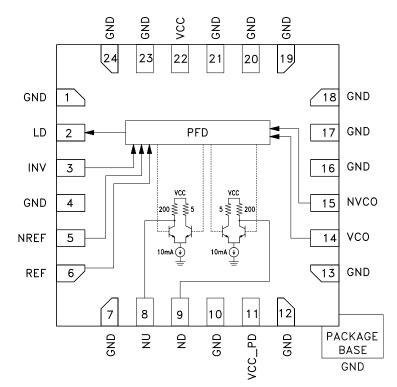
## **General Description**

The HMC3716LP4E is a digital phase frequency detector which operates from 10 to 1300MHz. It is intended for use in low phase noise synthesizer applications.

The combination of high frequency of operation along with its ultra low phase noise floor make possible synthesizers with wide loop bandwidth and low N resulting in fast switching and very low phase noise. When used in conjunction with a differential loop amplifier, the HMC3716LP4E generates output voltages that can be used to phase lock a VCO to a reference oscillator.

The device is packaged in a 24-pin, 4 x 4mm leadless QFN surface mount package with an exposed ground paddle for improved RF and thermal performance.

# **Functional Diagram**



Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

# HMC3716\* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

# COMPARABLE PARTS

View a parametric search of comparable parts.

# EVALUATION KITS

• HMC3716 Evaluation Board

# DOCUMENTATION

#### **Data Sheet**

 HMC3716: HBT Digital Phase Frequency Detector 10 -1300 MHz Data Sheet

### TOOLS AND SIMULATIONS $\square$

• Using the HMC Design Tool for Synthesizers with a PFD Output

# DESIGN RESOURCES

- HMC3716 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

# DISCUSSIONS

View all HMC3716 EngineerZone Discussions.

# SAMPLE AND BUY

Visit the product page to see pricing options.

# TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

# DOCUMENT FEEDBACK

Submit feedback for this data sheet.



# HBT DIGITAL PHASE FREQUENCY DETECTOR 10 - 1300MHz

# Electrical Specifications, $T_A = +25^{\circ}$ C, Vcc = 5.0V

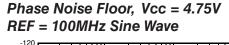
Parameter	Conditions	Min.	Тур.	Max.	Units
REF / VCO Input Frequency	Min must be Square Wave Max can be Sine or Square Wave	10	100	1300	MHz
Input Power Range		-10	5	+5	dBm
Output Voltage Swing (NU / ND)	Driving High-Z Load / Op-Amp		2		Vp-p
PFD Gain	Gain = Vpp / 2π Rad		0.32		V / Rad
SSB Phase Noise [1]	@ 10kHz Offset with 100 MHz REF / VCO @ +5 dBm		-153		dBc/Hz
Logic Input Voltage (INV)	CMOS / TTL Logic Low CMOS / TTL Logic High	0.0 1.8		1.1 5.0	V
Lock Detect Output Voltage	Filtering & 1kΩ Pull-Up Required CMOS / TTL Logic Low = Unlocked MOS / TTL Logic High = Locked	0.0 2.7		0.5 5.0	V
Lock Detect Sink Current			5		mA
Supply Voltage (Vcc)		4.75	5.00	5.25	V
Supply Current (Icc)	Vcc = 5.0V		115		mA
Temperature Range		-40		+85	°C

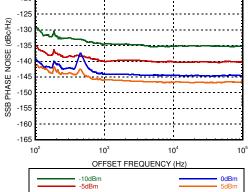
[1] Square wave input achieves best phase noise at lower REF/VCO frequencies (see comparison plots on preceding page)



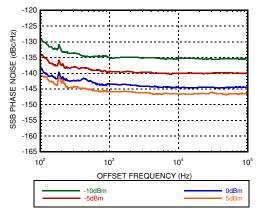
v02.0316

HBT DIGITAL PHASE FREQUENCY DETECTOR 10 - 1300MHz

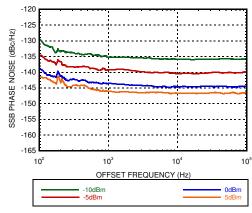




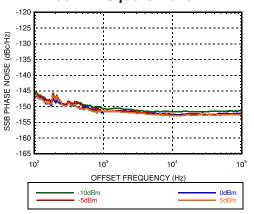
#### Phase Noise Floor, Vcc = 5.00V REF = 100MHz Sine Wave



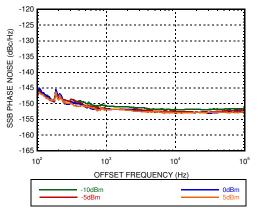
#### Phase Noise Floor, Vcc = 5.25V REF = 100MHz Sine Wave



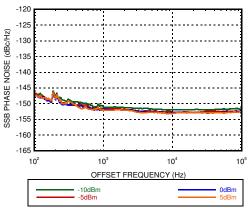
Phase Noise Floor, Vcc = 4.75V REF = 100MHz Square Wave



#### Phase Noise Floor, Vcc = 5.00V REF = 100MHz Square Wave



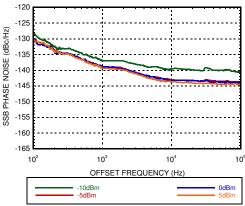
#### Phase Noise Floor, Vcc = 5.25V REF = 100MHz Square Wave



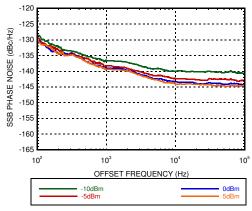


# HBT DIGITAL PHASE FREQUENCY DETECTOR 10 - 1300MHz

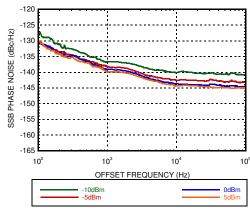
### Phase Noise Floor, Vcc = 4.75V REF = 1000MHz Sine Wave



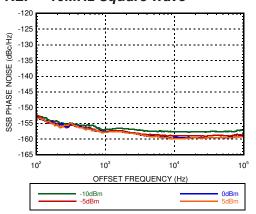
#### Phase Noise Floor, Vcc = 5.00V REF = 1000MHz Sine Wave



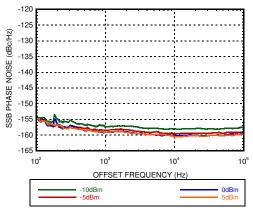
#### Phase Noise Floor, Vcc = 5.25V REF = 1000MHz Sine Wave



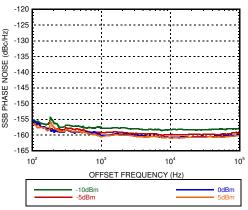
#### Phase Noise Floor, Vcc = 4.75V REF = 10MHz Square Wave



#### Phase Noise Floor, Vcc = 5.00V REF = 10MHz Square Wave



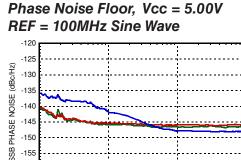
Phase Noise Floor, Vcc = 5.25V REF = 10MHz Square Wave

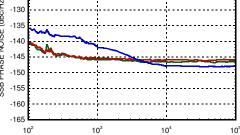




v02.0316

HBT DIGITAL PHASE FREQUENCY DETECTOR 10 - 1300MHz





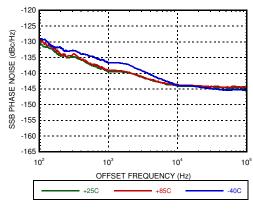
OFFSET FREQUENCY (Hz)

+85C

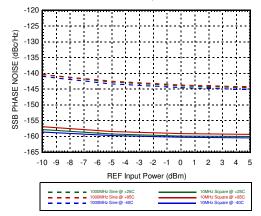
-40C

#### Phase Noise Floor, Vcc = 5.00V REF = 1000MHz Sine Wave

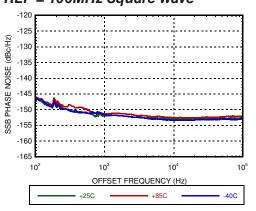
+25C



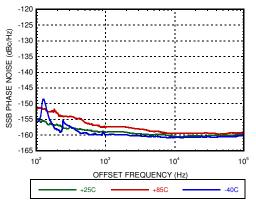
Phase Noise Floor, Vcc = 5.00V REF = 10 & 1000MHz, ≥10kHz offset



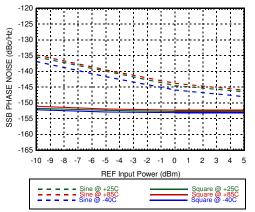
Phase Noise Floor, Vcc = 5.00V REF = 100MHz Square Wave



#### Phase Noise Floor, Vcc = 5.00V REF = 10MHz Square Wave



Phase Noise Floor, Vcc = 5.00V REF = 100MHz, ≥10kHz offset

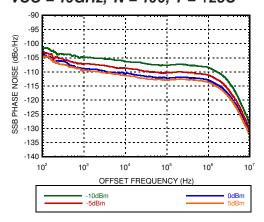


For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 Phone: 781-329-4700 • Order online at www.analog.com Application Support: Phone: 1-800-ANALOG-D



# HBT DIGITAL PHASE FREQUENCY DETECTOR 10 - 1300MHz

Typical PLL Performance, Vcc = 5.00VREF = 100MHz Square Wave VCO = 10GHz, N = 100, T = +25C



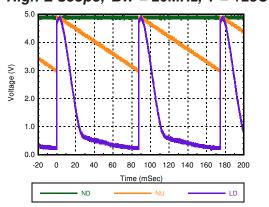
### Typical Supply Current vs. Vcc

Vcc (Vdc)	Icc (mA)
4.75	107
5.00	115
5.25	123

# **Reliability Information**

Junction Temperature To Maintain 1 Million Hour MTTF	135 °C
Nominal Junction Temperature (T = +85 °C)	99.3 °C
Thermal Resistance (junction to ground paddle)	24.9°C/W
Operating Temperature	-40 to +85 °C

PFD Outputs ND, NU, LD, Vcc = 5.00VForced PFD Difference  $\approx 11Hz$ High-Z Scope, BW = 20MHz, T = +25C



# Typical ND & NU Voltages, Vcc = +5V

Symbol	Characteristics	+25C			Linita
		Min.	Тур.	Max.	Units
Voh	Output High Voltage	4.9	5.0	5.1	V
Vol	Output Low Voltage	2.9	3	3.1	V

# Absolute Maximum Ratings

RF Input (Vcc= +5V)	+13 dBm	
Supply Voltage (Vcc)	+5.5V	
Logic Inputs (INV)	-0.5 to (0.5V + Vcc)	
PFD Outputs (ND, NU)	2.5 to (0.5V + Vcc)	
Storage Temperature	-65 to +150 °C	
ESD Sensitivity (HBM)	Class 1B	
ESD Sensitivity (CDM) Class C2		



Notes:

- 1. All data shown is typical and actual performance may vary depending upon implementation.
- 2. Phase Noise data taken utilizing 2-unit PLL cancellation method with VCO  $\geq$  2400MHz and healthy power level.
- 3. Only one PFD output will be active with a forced frequency difference, depending upon which input frequency is higher.
- 4. Without oscilloscope bandwidth limiting, there will be narrow pulses on NU, ND, & LD, at the input frequencies.
- These pulses may create spectral content, which is normally surpressed with the loop filter and lock detect filter.



# HBT DIGITAL PHASE FREQUENCY DETECTOR 10 - 1300MHz

# **Pin Descriptions**

Pin Number	Function	Description	Interface Schematic
1, 4, 7, 10, 12, 13, 16 - 21, 23, 24, Paddle	GND	Package bottom has an exposed metal paddle that must be connected to RF/DC ground.	GND ~
2	LD	Lock Detect Output Open collector pulsed output. Requires external 1kΩ Pullup to Vcc and filtering. Average "LOW" = UNLOCKED Avereage "HIGH" = LOCKED	$ \begin{array}{c} +5V \\ 1k \\ R=1k \\ C \\ 1000pF \\ \hline \end{array} $
3	INV	PFD INVERT Function to swap REF & VCO CMOS / TTL compatible Logic "LOW" = NORMAL Logic "HIGH" = INVERT	
11	Vcc_PD	Supply Voltage, +5.00V	Vcc ↔ Vcc_PD (*)
22	Vcc		<u> </u>
8	NU	Up Output Do not load output below 2.5V or damage can occur.	Vcc • 5 \$ 200 5 ND, NU
9	ND	Down Output Do not load output below 2.5V or damage can occur.	€ 10mA
5	NREF	Differential REF Inputs	Vcc •
6	REF	Pins are DC coupled, External DC blocks required	
14	VCO	Differential VCO Inputs	
15	NVCO	Pins are DC coupled, External DC blocks required	



v02.0316

# HBT DIGITAL PHASE FREQUENCY DETECTOR 10 - 1300MHz

## **PFD Functionality**

The phase frequency detector functionality of the HMC3716LP4E is such that it compares the rising edge the two input signals (REF / VCO). This information is then used to pulse the ND and NU outputs depending upon which input signal is greater in frequency.

Under normal operation the ND pin will be active when VCO frequency is greater than the REF frequency; NU would remain constant. Conversly, when the VCO frequency is lower than the REF frequency, then NU would be active and ND would remain constant. Here, the term "active" means that the output will on average, vary between 3 - 5V, and the term "remain constant" means that the output will remain at approximately 5V.

## **INVERT Functionality**

The INV pin effectively swaps the REF and VCO input signals, such that the NU and ND pin responses are swapped. This has the advantage of easily correcting a layout issue if the loop filter op-amp inputs were swapped.

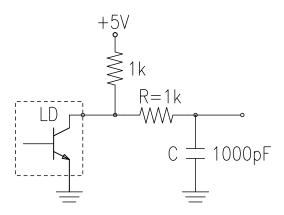
A logic "LOW" on this pin will configure the device for normal operation, and a logic "HIGH" cause the input signals to swap. The evaluation board has a  $10k\Omega$  resistor pull up resistor to 5V. A jumper must be installed connecting the INV pin to ground for normal operation.

## Lock Detect Functionality

The LD pin is an open collector pulsed output transistor. It requires an external 1k pull up resistor to Vcc (5V), as well as a simple RC filter.

Since the pin will produce very narrow pulses at each zero crossing of the REF and VCO input signals, filtering is necessary to create an average voltage which can be used to drive an LED or system input logic. When the device is "LOCKED", that transistor will effectively be "OFF", and the filtered output voltage will be "HIGH".

Below is an example of an RC filter for the lock detect pin. The value of resistor "R" should be greater than  $100\Omega$  to limit any surge current from flowing when the output transistor is "ON". The value of capacitor "C" should be selected such that the filter cutoff is much less than the REF frequency, but not excessively large (slow) that it will inhibit detection of lock status.



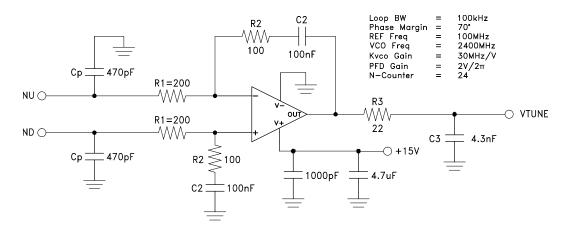


v02.0316

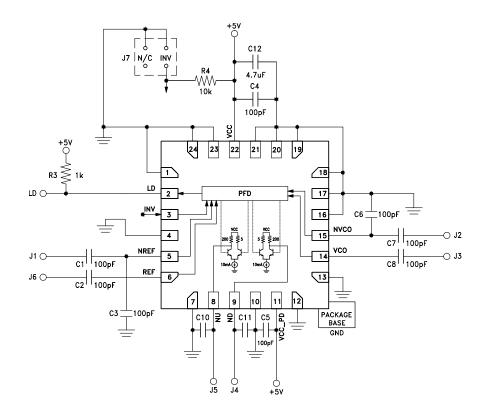
# HBT DIGITAL PHASE FREQUENCY DETECTOR 10 - 1300MHz

# **Typical Loop Filter**

A diffential op-amp loop filter is required in order to integrate the ND and NU pulses into a usable tune voltage to drive the oscillator in a PLL. The loop filter synthesis can be performed using a variety of simulation tools. Below is an example of a third-order filter produced with the listed PLL parameters for loop bandwidth, etc.



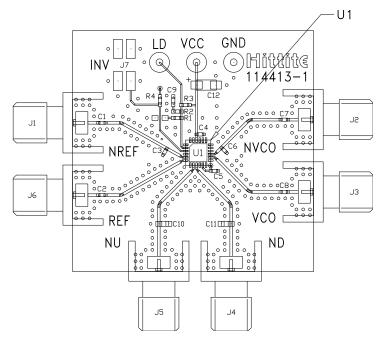
# **Evaluation PCB Circuit**





# HBT DIGITAL PHASE FREQUENCY DETECTOR 10 - 1300MHz

### **Evaluation PCB**



The circuit board used in the application should use RF circuit design techniques. Signal lines should have  $50\Omega$  impedance while the package ground leads and backside ground paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes.

Item	Description		
PCB [2]	114413 Eval Board		
U1	HMC3716LP4E, PFD w/ Lock Detect and Invert functions		
J1 - J6	PCB Mount SMA RF Connector		
J7	2mm, 4-pin DC Header (cut to fit)		
Qty 1	2mm Shunt/Jumper		
C1 - C8	100pF Ceramic Capacitor, 5%, 50V, 0402		
C12	4.7µF, Tantalum Capacitor, 16V, 20%, 3216		
R3	1kΩ Resistor, 5%, 1/10W, 0402		
R4	10kΩ Resistor, 5%, 1/10W, 0402		
R1, R2, C9 - C11	Do Not Install		

### List of Materials for Evaluation PCB EV1HMC3716LP4 [1]

[1] Reference this part number when ordering complete PCB

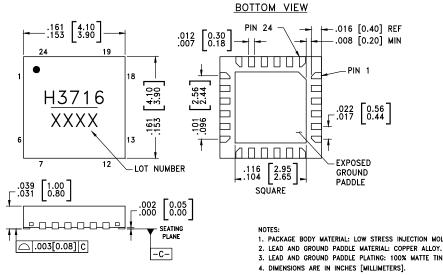
[2] Circuit Board Material: Rogers 4350



## HMC3716LP4E v02.0316

# **HBT DIGITAL PHASE FREQUENCY DETECTOR** 10 - 1300MHz

## **Outline Drawing**



1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.

- LEAD SPACING TOLERANCE IS NON-CUMULATIVE. 5.
  - CHARACTERS TO BE HELVETICA MEDIUM, .025 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
- 6. 7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.

8. PACKAGE WARP SHALL NOT EXCEED 0.05n

- 9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
- 10. REFER TO ADI APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

## Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking <sup>[2]</sup>
HMC3716LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 <sup>[1]</sup>	<u>H3716</u> XXXX

[1] Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX