HMC641

v01.0108

GaAs MMIC SP4T NON-REFLECTIVE SWITCH, DC - 18 GHz

Typical Applications

The HMC641 is ideal for:

- Telecom Infrastructure
- Microwave Radio & VSAT
- Military & Space Hybrids
- Test Instrumentation

Features

Broadband Performance: DC - 18 GHz

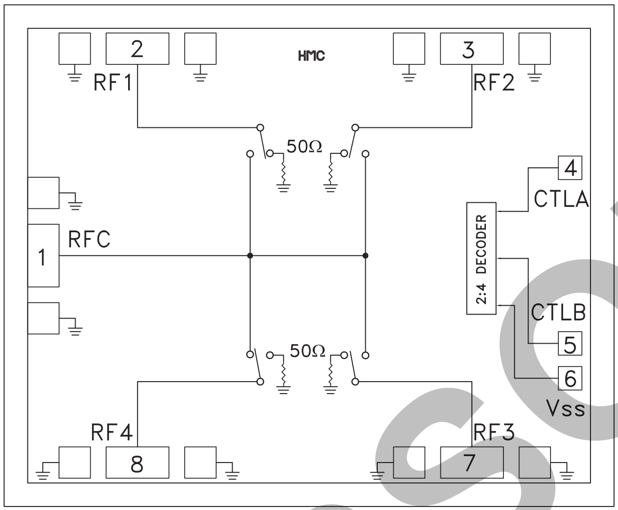
High Isolation: 42 dB @ 12 GHz

Low Insertion Loss: 2.1 dB @ 12 GHz

Integrated 2:4 TTL Decoder

Small Size: 1.92 x 1.60 x 0.10 mm

Functional Diagram



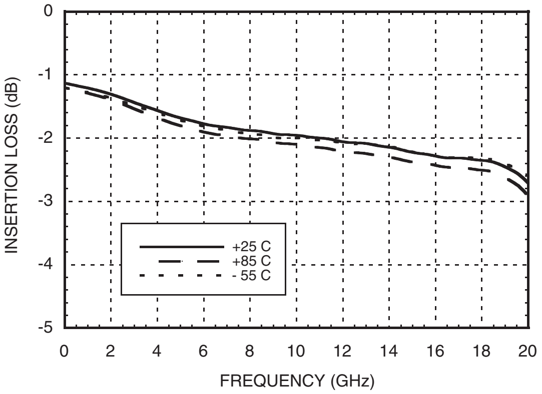
General Description

The HMC641 is a broadband non-reflective GaAs PHEMT SP4T switch chip. Covering DC to 18 GHz, this switch offers high isolation and low insertion loss and extends the frequency coverage of Hittite's SP4T switch product line. This switch also includes an on board binary decoder circuit which reduces the number of required logic control lines to two. The switch operates using a negative control voltage of 0/-5V, and requires a fixed Vss bias of -5V. All data is tested with the chip in a 50 Ohm test fixture connected via one 3.0 x 0.5 mil gold ribbon of minimal length on each RF port.

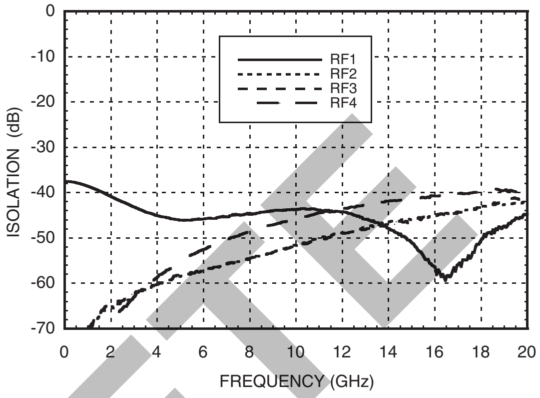
Electrical Specifications, T_A = +25° C, With 0/-5V Control, Vss= -5V, 50 Ohm System

Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	DC - 12 GHz DC - 18 GHz		1.8 2.8	2.1 3.1	dB dB
Isolation (RFC to RF1 - RF4)	DC - 12 GHz DC - 18 GHz	39 37	42 40		dB dB
Return Loss "On State"	DC - 12 GHz DC - 18 GHz	12 11	15 14		dB dB
Return Loss "Off State"	DC - 18 GHz	12	15		dB
Input Power for 1 dB Compression	2.05- 18 GHz	21	24		dBm
Input Third Order Intercept (Two-Tone Input Power= +14 dBm Each Tone)	0.05 - 18 GHz	37	40		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	DC - 18GHz		14 95		ns ns

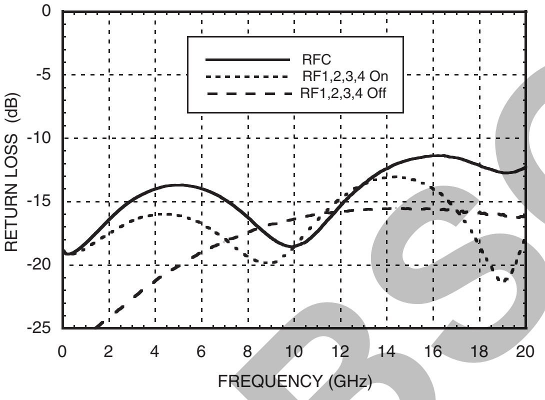
Insertion Loss vs. Temperature



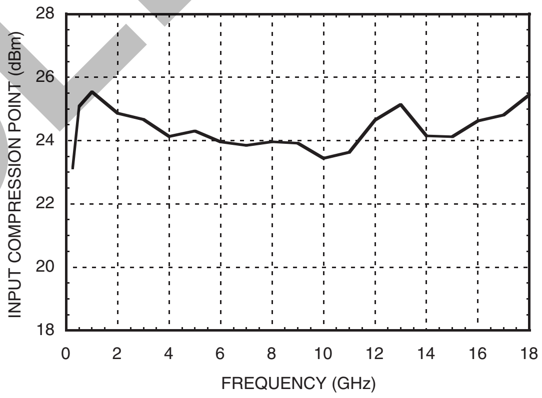
Isolation



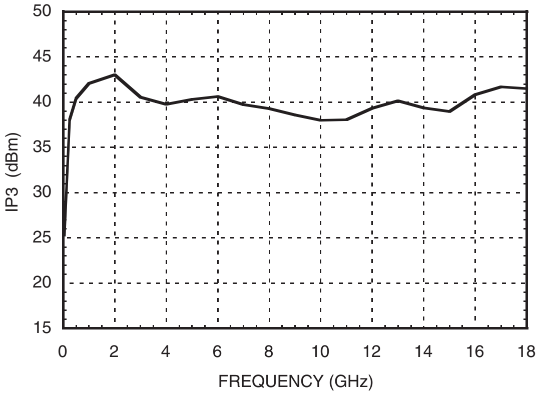
Return Loss



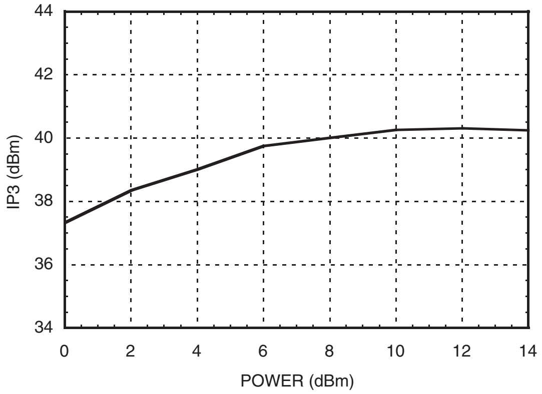
1 dB Input Compression Point



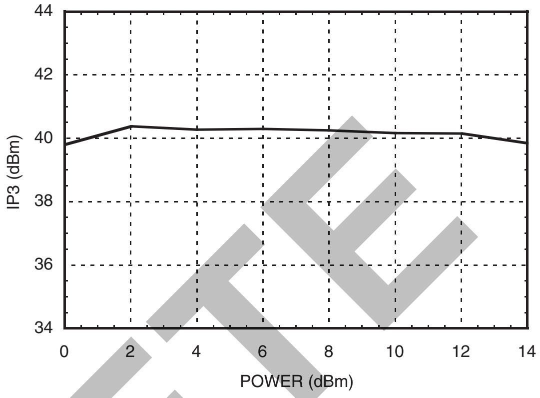
Input Third Order Intercept Point @ +14 dBm Tone Power



IP3 vs. Input Tone Power @ 500 MHz



IP3 vs. Input Tone Power @ 12 GHz



Absolute Maximum Ratings

Bias Voltage Range (Vss)	-7 Vdc
Control Voltage Range (A & B)	Vss -0.5V to +1 Vdc
Channel Temperature	150 °C
Thermal Resistance Channel to die bottom (Insertion Loss Path)	188 °C/W
Thermal Resistance Channel to die bottom (Terminated Path)	222 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C
Maximum Input Power	+24 dBm

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Truth Table

Control Input		Signal Path State
A	B	RFC to:
High	High	RF1
Low	High	RF2
High	Low	RF3
Low	Low	RF4

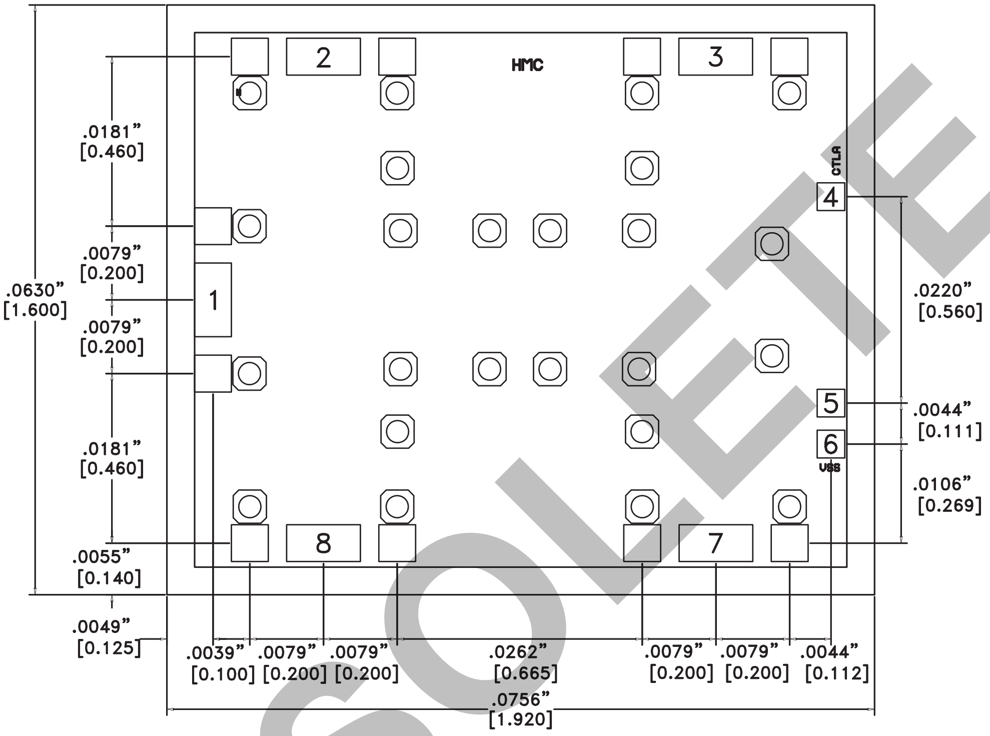
Bias Voltage & Current

Vss Range= -5.0 Vdc ±10%		
Vss (Vdc)	Iss (Typ) (mA)	Iss (Max) (mA)
-5	3	6

TTL/CMOS Control Voltages

State	Bias Condition
Low	-3V to 0 Vdc @ 60 uA Typ.
High	-5 to -4.2 Vdc @ 5 uA Typ.

Outline Drawing



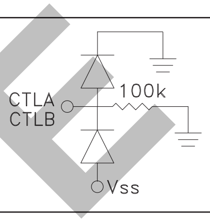
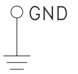
Die Packaging Information [1]

Standard	Alternate
WP-18 (Waffle Pack)	[2]

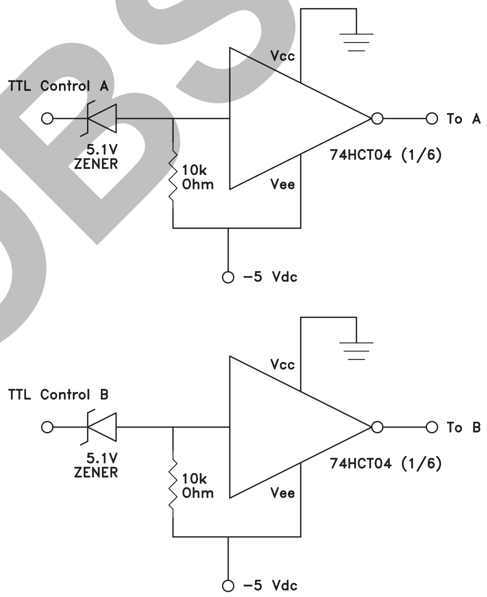
[1] Refer to the "Packaging Information" section for die packaging dimensions.
[2] For alternate packaging information contact Hittite Microwave Corporation.

NOTES:
1. DIMENSIONS IN INCHES [MILLIMETERS].
2. DIE THICKNESS IS 0.004".
3. TYPICAL BOND PAD IS 0.004" SQUARE.
4. TYPICAL BOND PAD SPACING IS 0.006" CENTER TO CENTER.
5. BOND PAD METALLIZATION: GOLD.
6. BACKSIDE METALLIZATION: GOLD.
7. BACKSIDE METAL IS GROUND.
8. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS.

Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1, 2, 3, 7, 8	RFC, RF1, RF2, RF3, RF4	These pads are DC coupled and matched to 50 Ohms. Blocking capacitors are required if RF line potential is not equal to 0V.	
4	CTLA	See Truth Table and Control Voltage Table.	
5	CTLB	See Truth Table and Control Voltage Table.	
6	Vss	Supply Voltage -5.0 Vdc ± 10%.	
Die Bottom	GND	Die Bottom must be connected to RF/DC ground.	

TTL Interface Circuit



Note:
Control inputs A and B can be driven directly with TTL logic with -5 Volts applied to the HCT logic gates Vee pin and to Vss Pad of the RF Switch.

Assembly Diagram