HMC642ALC5

v00.0415

GaAs MMIC 6-BIT DIGITAL PHASE SHIFTER, 9 - 12.5 GHz

Typical Applications

The HMC642ALC5 is ideal for:

- EW Receivers
- Weather & Military Radar
- Satellite Communications
- Beamforming Modules
- Phase Cancellation

Features

Low RMS Phase Error: 4.5°

Low Insertion Loss: 7 dB

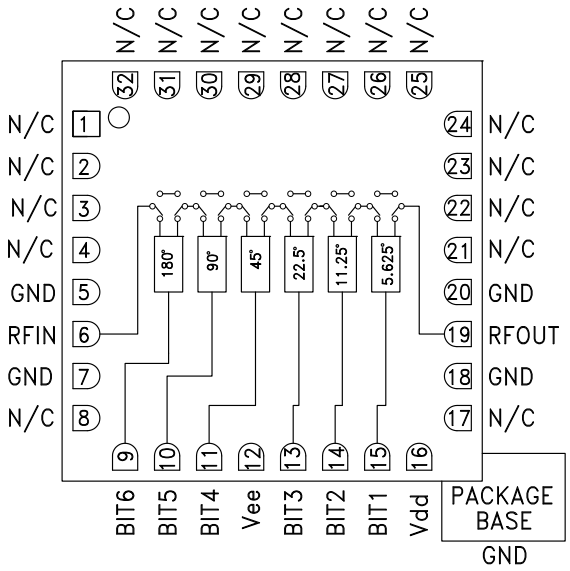
High Linearity: +35 dBm

Positive Control Logic

360° Coverage, LSB = 5.625°

32 Lead 5x5mm SMT Package: 25mm²

Functional Diagram



General Description

The HMC642ALC5 is a 6-bit digital phase shifter which is rated from 9 to 12.5 GHz, providing 360 degrees of phase coverage, with a LSB of 5.625 degrees. The HMC642ALC5 features very low RMS phase error of 4.5 degrees and extremely low insertion loss variation of ±0.4 dB across all phase states. This high accuracy phase shifter is controlled with positive control logic of 0/+5V The HMC642ALC5 is housed in a compact 5x5 mm ceramic leadless SMT package and is internally matched to 50 Ohms with no external components.

Electrical Specifications

T_A = +25° C, Vss= -5V, Vdd= +5V , control Voltage = 0/ +5V, 50 Ohm System

Parameter	Min.	Typ.	Max.	Units
Frequency Range	9		12.5	GHz
Insertion Loss*		7	10	dB
Input Return Loss*		14		dB
Output Return Loss*		11		dB
Phase Error*		±10	+18/-10	deg
RMS Phase Error		4.5		deg
Insertion Loss Variation*		±0.4		dB
Input Power for 1 dB Compression		30		dBm
Input Third Order Intercept		35		dBm
Control Voltage Current		<250		µA
Bias Control Current		<12		mA

*Note: Major States Shown

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Application Support: Phone: 1-800-ANALOG-D

HMC642A* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC642A Evaluation Board

DOCUMENTATION

Data Sheet

- HMC642ALC5: GaAs MMIC 6-Bit Digital Phase Shifter, 9-12.5 GHz Data Sheet

DESIGN RESOURCES

- HMC642A Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC642A EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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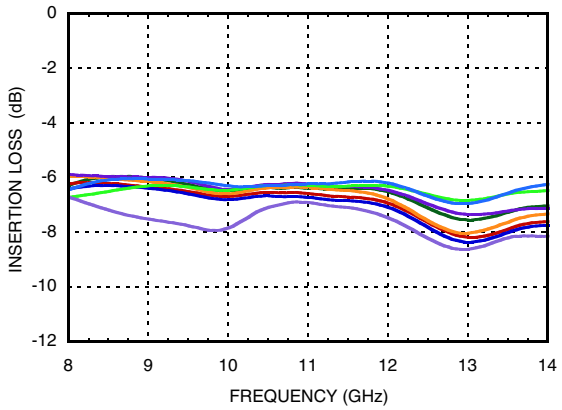
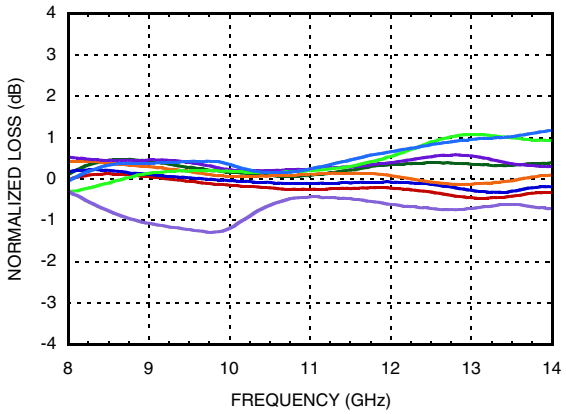
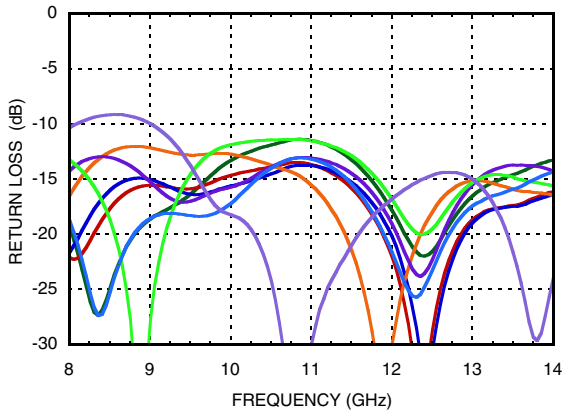
Insertion Loss, Major States Only



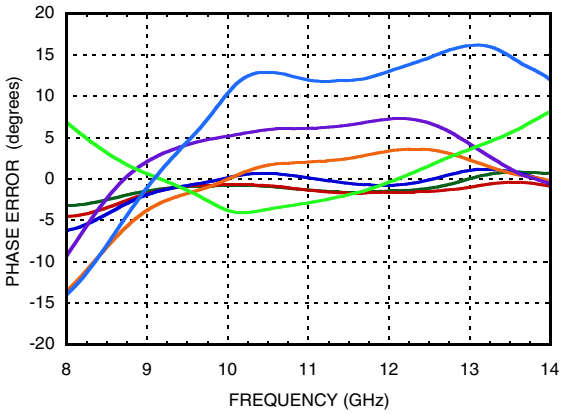
Normalized Loss, Major States Only



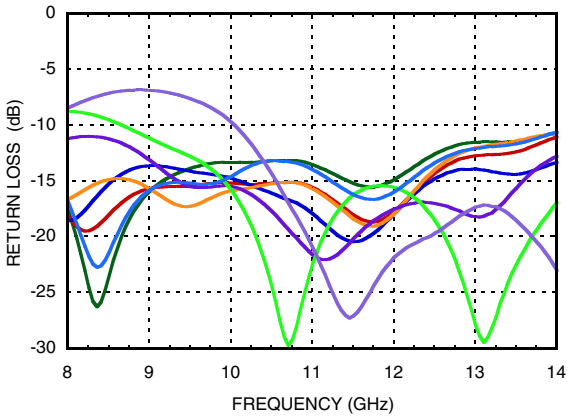
Input Return Loss, Major States Only



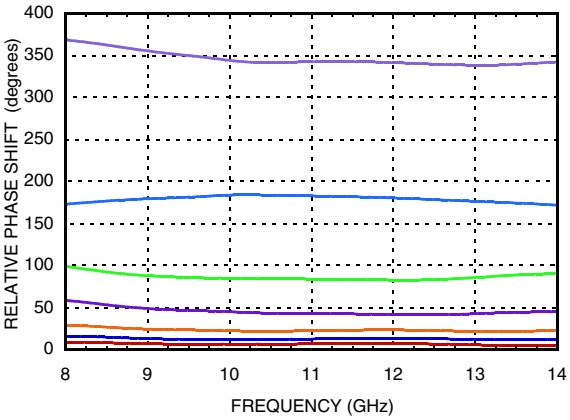
Phase Error, Major States Only



Output Return Loss, Major States Only



Relative Phase Shift Major States Including All Bits



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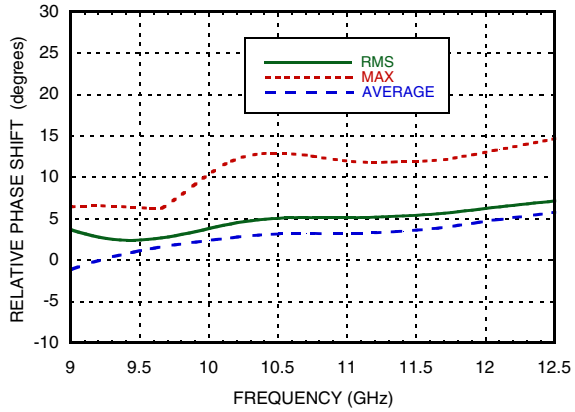
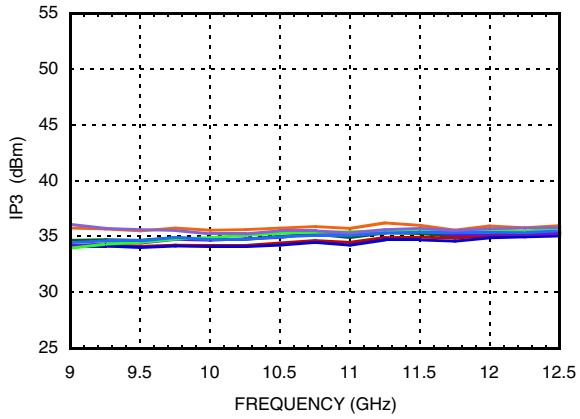
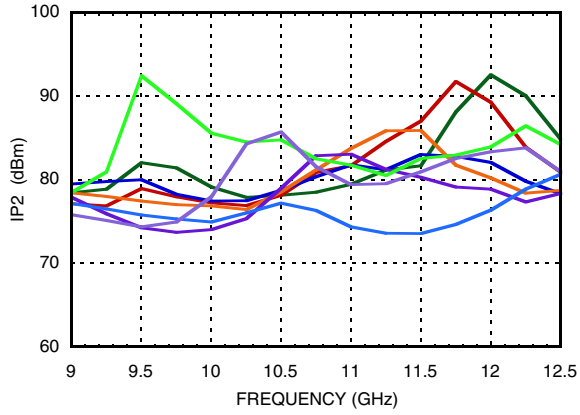
Relative Phase Shift, RMS, Average, Max, All States



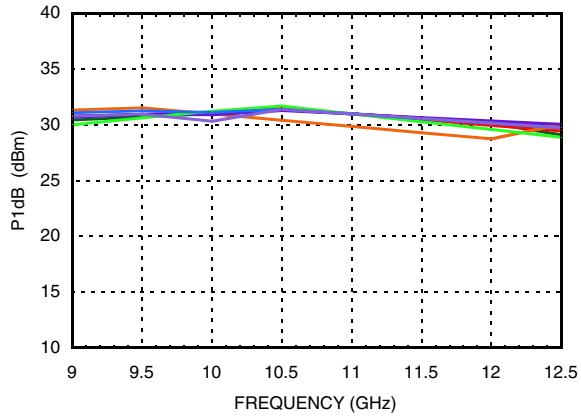
Input IP3, Major States Only



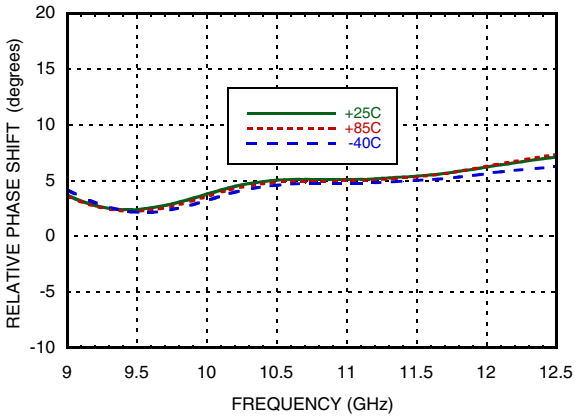
Input IP2, Major States Only



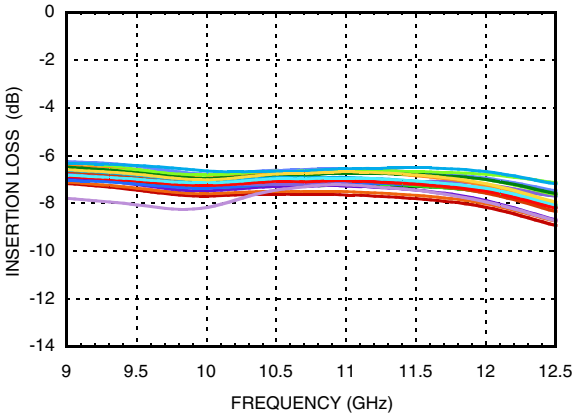
Input P1dB, Major States Only



RMS Phase Error vs. Temperature



Insertion Loss vs. Temperature, Major States Only



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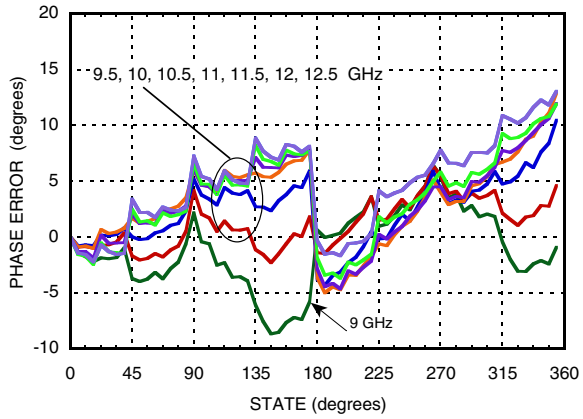
Phase Error vs. State



Bias Voltage & Current

Vdd	Idd
5.0	5.6mA
Vss	Iss
-5.0	5.6mA

Control Voltage

State	Bias Condition
Low (0)	0 to 0.2 Vdc
High (1)	Vdd ±0.2 Vdc @ 35 µA Typ.

Absolute Maximum Ratings

Input Power (RFIN)	29 dBm (T= +85 °C)
Bias Voltage Range (Vdd)	-0.2 to +12.5V
Bias Voltage Range (Vss)	+0.2 to -12V
Channel Temperature (Tc)	150 °C
Thermal Resistance (channel to ground paddle)	190 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class1A Passed 250V

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Truth Table

Control Voltage Input						Phase Shift (Degrees) RFIN - RFOUT
Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	
0	0	0	0	0	0	Reference*
1	0	0	0	0	0	5.625
0	1	0	0	0	0	11.25
0	0	1	0	0	0	22.5
0	0	0	1	0	0	45.0
0	0	0	0	1	0	90.0
0	0	0	0	0	1	180.0
1	1	1	1	1	1	354.375

Any combination of the above states will provide a phase shift approximately equal to the sum of the bits selected.
*Reference corresponds to monotonic setting

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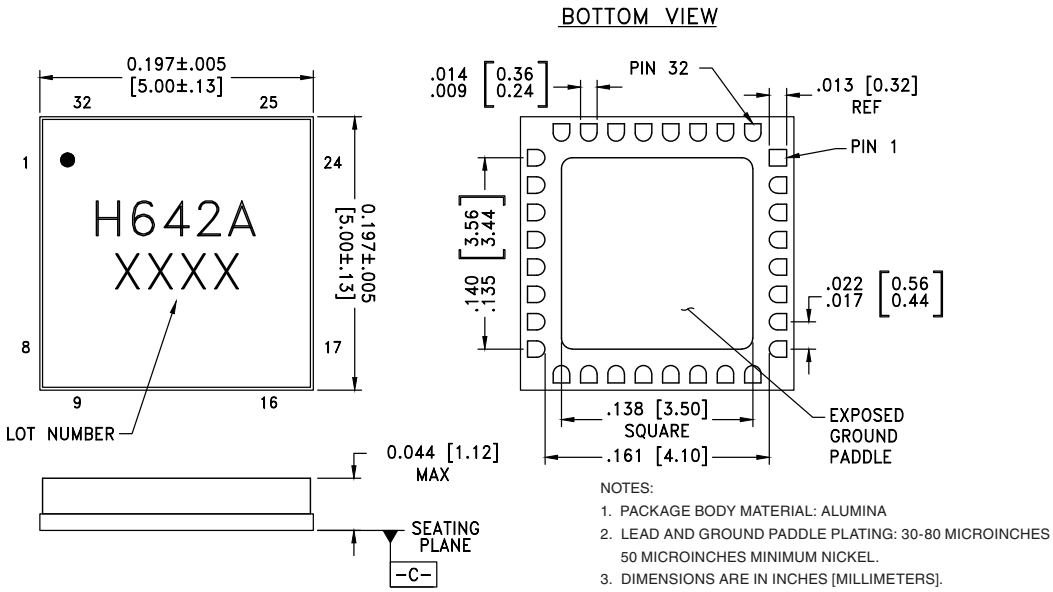
Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. CLASSIFIED AS MOISTURE SENSITIVITY LEVEL (MSL) 1.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC642ALC5	Alumina White	Gold over Nickel	MSL3 [1]	H642A XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1 - 4, 8,17 21 - 32	N/C	No connection required. These pins may be connected to RF/DC ground without affecting performance.	
5, 7, 18, 20	GND	These pins and exposed ground paddle must be connected to RF/DC ground.	GND
6	RFIN	This port is DC coupled and matched to 50 Ohms.	RFIN
9 - 11, 13 - 15	BIT6, BIT5, BIT4, BIT3, BIT2, BIT1	Control Input. See truth table and control voltage tables.	
12	Vss	Voltage supply.	
16	Vdd	Voltage supply.	
19	RFOUT	This port is DC coupled and matched to 50 Ohms.	RFOUT

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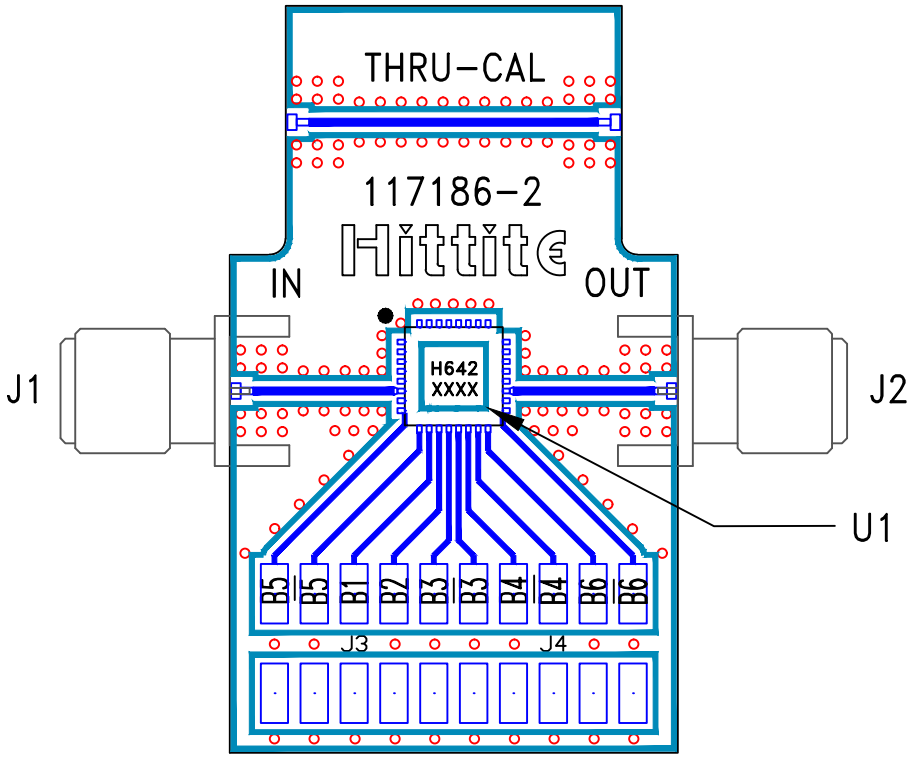
Evaluation PCB



List of Materials for Evaluation PCB EV1HMC642ALC5 [1][3]

Item	Description
J1 - J2	PCB Mount SMA RF Connector
J3 - J4	Molex Header 2mm
U1	HMC642ALC5 6-Bit Digital Phase Shifter
PCB [2]	117186 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

[3] Please refer to part's pin description and functional diagram for pin out assignments on evaluation board.

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.

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