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13 Gbps, D-Type Flip-Flop

Typical Applications

The HMC673LC3C is ideal for:

- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 13 Gbps
- Digital Logic Systems up to 13 GHz

Features

Supports High Data Rates: up to 13 Gbps

Differential & Singe-Ended Operation

Fast Rise and Fall Times: 24 / 22 ps

Low Power Consumption: 210 mW typ.

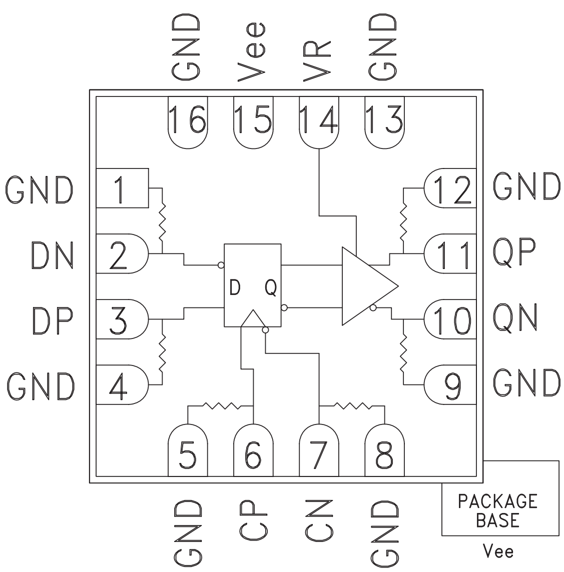
Programmable Differential
Output Voltage Swing: 400 - 1100 mV

Propagation Delay: 55 ps

Single Supply: -3.3V

16 Lead Ceramic 3x3mm SMT Package: 9mm²

Functional Diagram



General Description

The HMC673LC3C is a D-type Flip Flop designed to support data transmission rates of up to 13 Gbps, and clock frequencies as high as 13 GHz. During normal operation, data is transferred to the outputs on the positive edge of the clock. Reversing the clock inputs allows for negative-edge triggered applications. All input signals to the HMC673LC3C are terminated with 50 Ohms to ground on-chip, and maybe either AC or DC coupled. The differential outputs of the HMC673LC3C may be either AC or DC coupled. Outputs can be connected directly to a 50 Ohm to ground terminated system, while DC blocking capacitors may be used if the terminating system is 50 Ohms to a non-ground DC voltage. The HMC673LC3C operates from a single -3.3V dc supply and is available in a ceramic RoHS compliant 3x3 mm SMT package.

Electrical Specifications, T_A = +25°C, Vee = -3.3V

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		-3.6	-3.3	-3.0	V
Power Supply Current			62		mA
Maximum Data Rate			13		Gbps
Maximum Clock Rate			13		GHz
Input High Voltage		-0.5		0.5	V
Input Low Voltage		-1.0		0.0	V
Input Return Loss	Frequency <13 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		550		mVpp
	Differential, peak-to-peak		1100		mVpp
Output High Voltage			-10		mV
Output Low Voltage			-570		mV
Output Rise / Fall Time	Differential, 20% - 80%		24 / 22		ps

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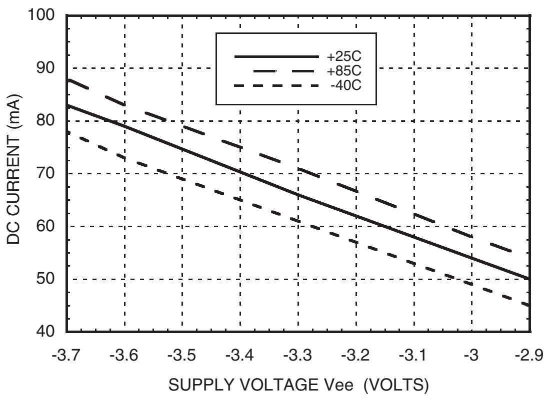
Electrical Specifications, (continued)

Parameter	Conditions	Min.	Typ.	Max	Units
Output Return Loss	Frequency <13 GHz		10		dB
Random Jitter Jr	rms [1]			0.2	ps rms
Deterministic Jitter, Jd	peak-to-peak, 2^{15}-1 PRBS input [2]		2		ps, pp
Propagation Delay Clock to Data, td			55		ps
Clock Phase Margin	13 GHz		320		deg
Set Up & Hold Time, t_{SH}			6		ps

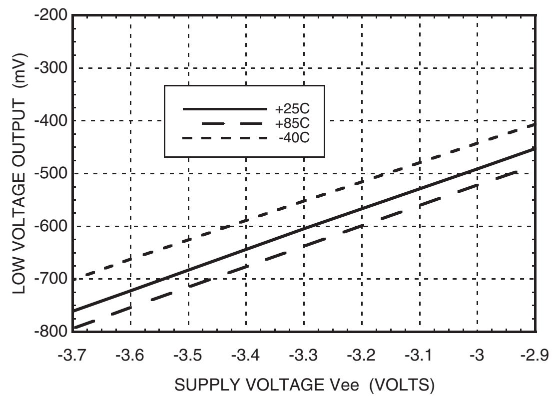
[1] Upper limit of random jitter, JR, determined by measuring and integrating output phase noise with a sinusodal input at 5, 10, and 13.5 GHz over temperature

[2] Deterministic jitter calculated by simultaneously measuring the jitter of a 200 mV, 12.5 GHz, 2^{15}-1 PRBS input, and a single-ended output

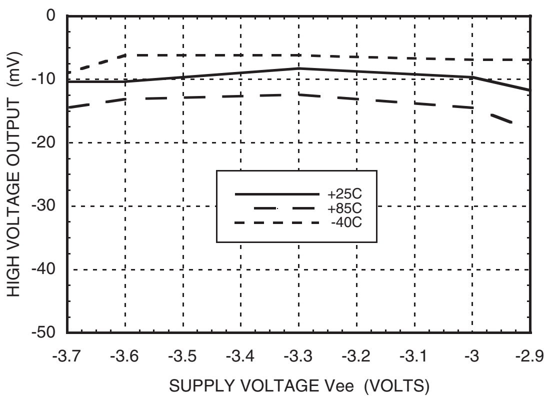
DC Current vs. Supply Voltage [1]



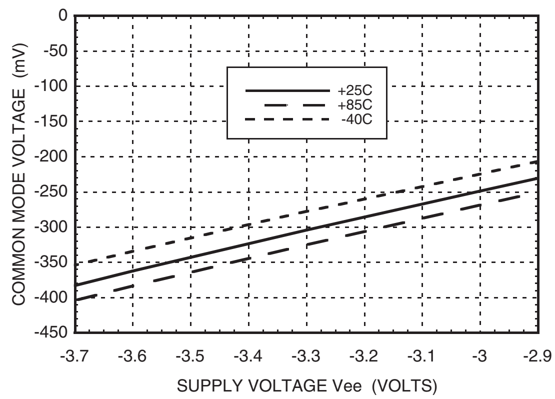
Output Low Voltage vs. Supply Voltage [1] [2]



Output High Voltage vs. Supply Voltage [1] [2]



Common Mode Voltage vs. Supply Voltage [1] [2]



[1] VR = 0.0V [2] Frequency = 1 GHz

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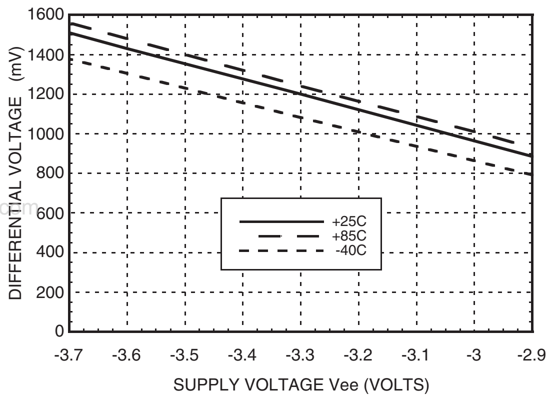
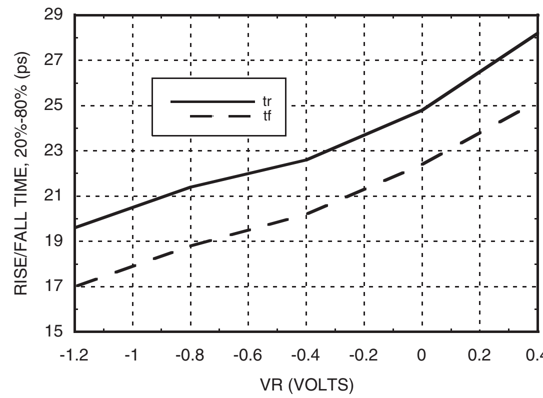
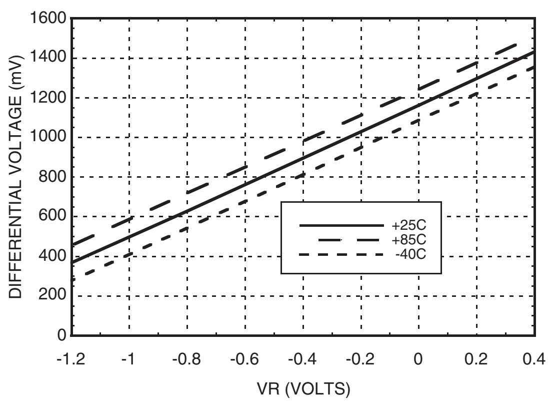
Output Differential vs. Supply Voltage [1] [2]



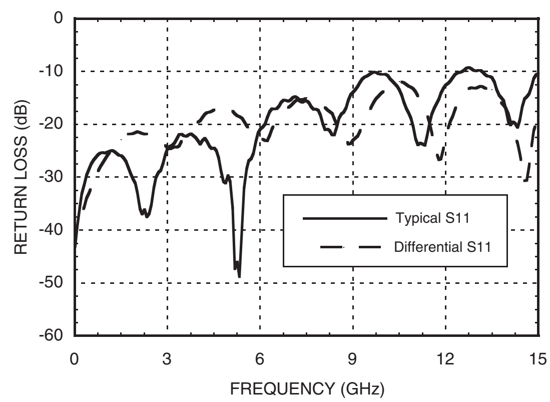
Rise / Fall Time vs. VR [3]



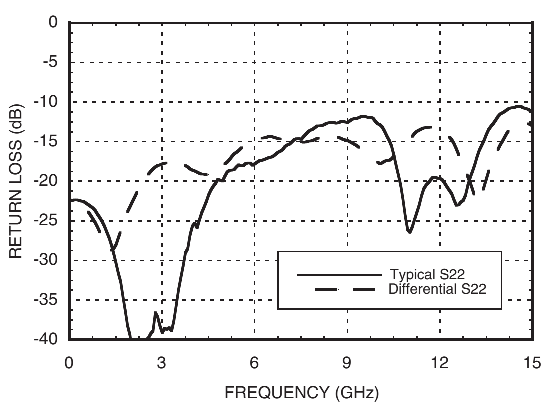
Output Differential vs. VR [2]



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



[1] VR = 0.0V [2] Frequency = 1 GHz [3] Frequency = 5 GHz

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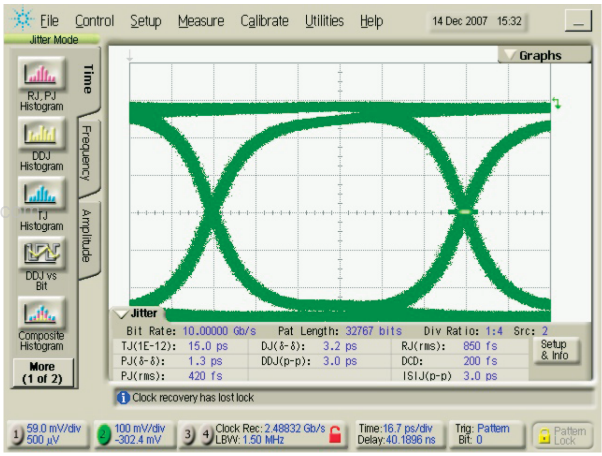
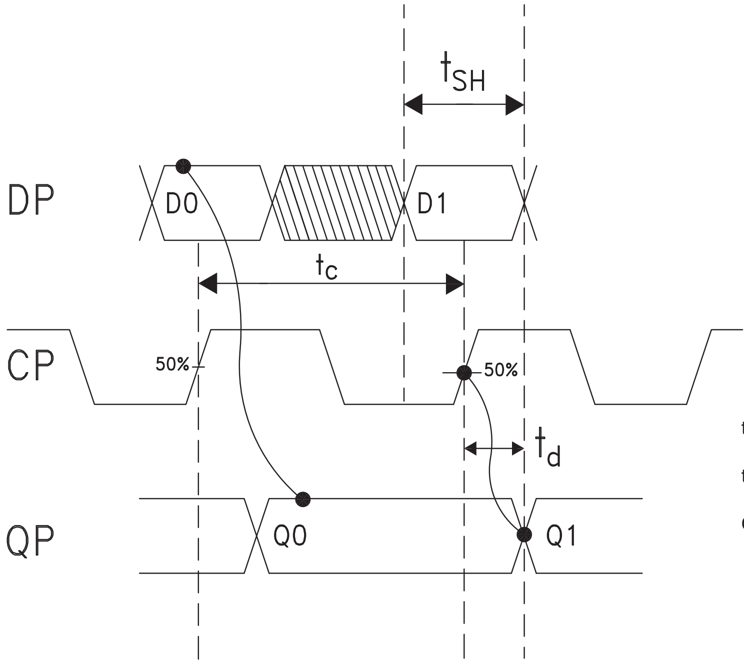
Eye Diagram



[1] Test Conditions:
Pattern generated with an Agilent N4901B Serial BERT
Eye diagram data presented on an Infinium DCA 86100A
Rate = 10.0 GB/s
Pseudo Random Code = 2^{15} -1
Vin = 400 mVpp differential

[2] Vertical Scale = 100 mV/Div

Timing Diagram



$t_C = \frac{1}{f_{clock}}$

t_{SH} = Setup and Hold Time

CPM = Clock Phase Margin = 360° $\frac{t_C - t_{SH}}{t_C}$

Truth Table

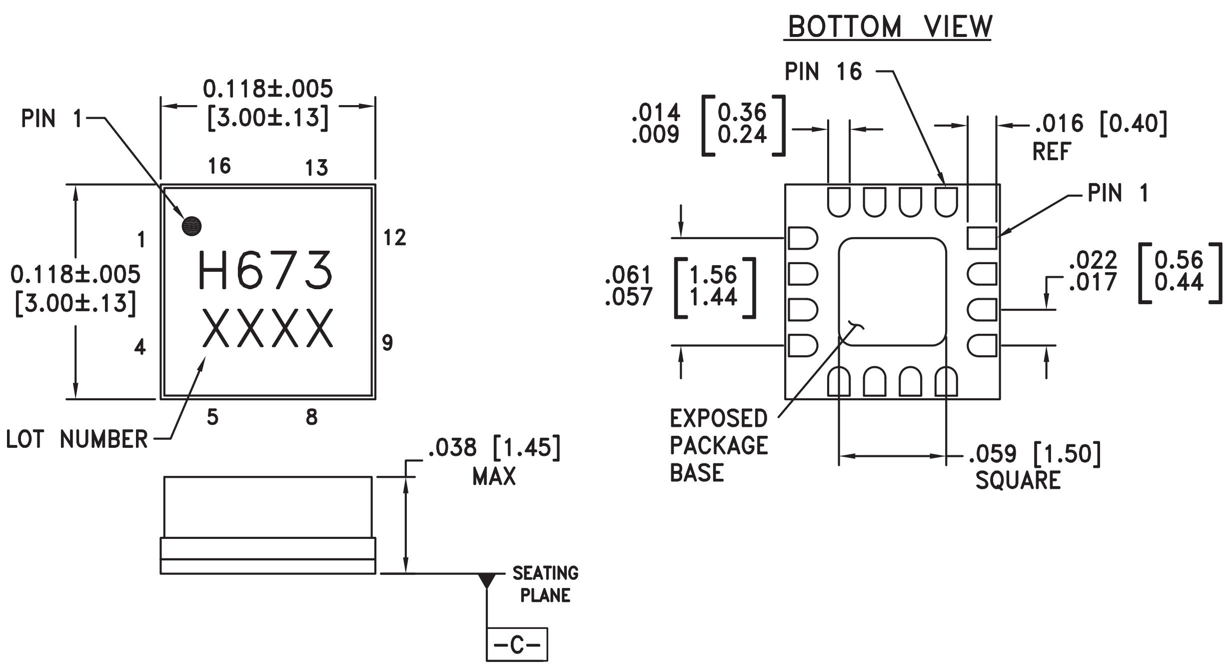
Input		Outputs
D	C	Q
L	L -> H	L
H	L -> H	H
Notes: D = DP - DN C = CP - CN Q = QP - QN	H - Negative voltage level L - Positive voltage level	

Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75V to +0.5V
Input Signals	-2V to +0.5V
Output Signals	-1.5V to +1V
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C

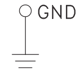
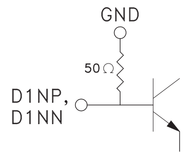
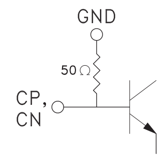
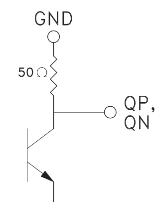
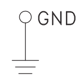
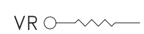
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. GROUND PADDLE MUST BE SOLDERED TO Vee.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3	DN, DP	Data Inputs	
6, 7	CP, CN	Clock Inputs	
10, 11	QN, QP	Data Outputs	
13, 16	GND	Supply Ground	
14	VR	Output level control. Output level may be adjusted by either applying a voltage to VR per “Output Differenital vs. VR” plot, or by tying VR to GND with a resister per the following equation: $V_0(R) = 1.2 / (2.1 + R)$, R in kΩ	
15, Package Base	Vee	Negative Supply	

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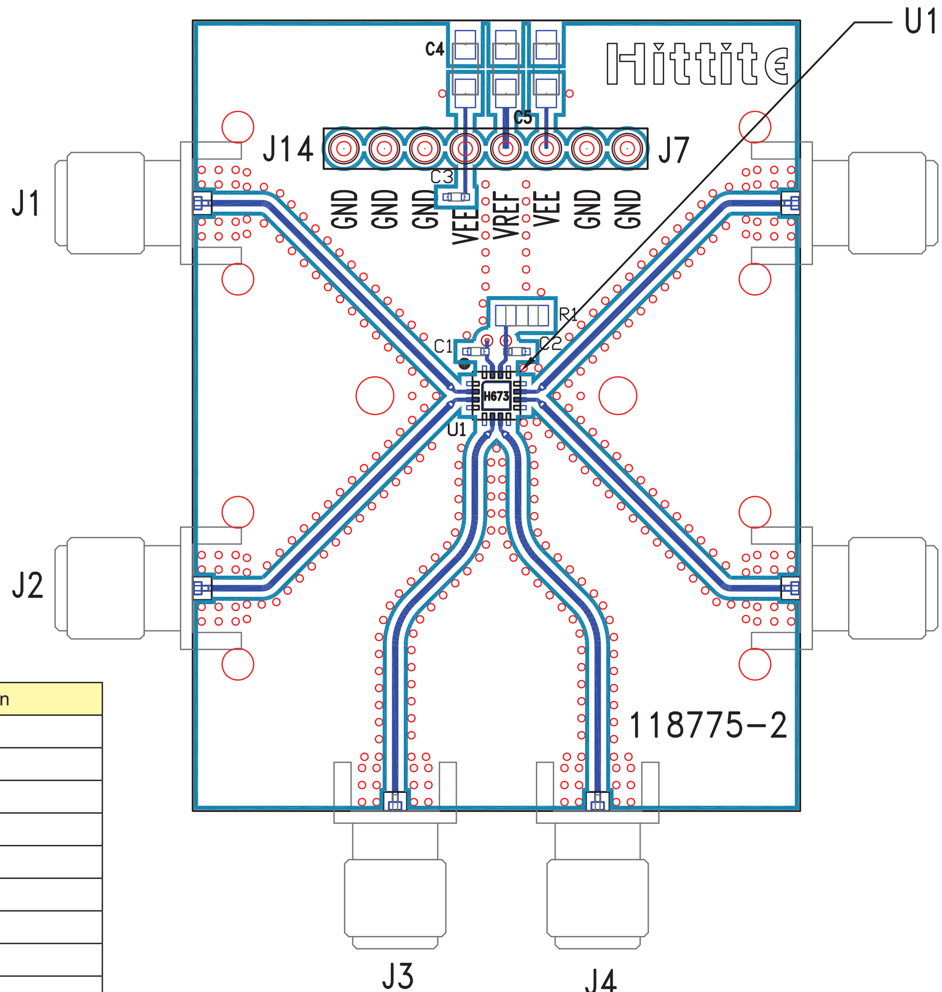
Evaluation PCB



Item	Description
J1	DN
J2	DP
J3	CP
J4	CN
J5	QP
J6	QN
J7, J8, J12 - J14	GND
J10	VR
J11	Vee

List of Materials for Evaluation PCB 118777 [1]

Item	Description
J1 - J6	PCB Mount SMA RF Connectors
J7 - J14	DC Pin
C1 - C3	100 pF Capacitor, 0402 Pkg.
C4 - C5	4.7 µF Capacitor, Tantalum
R1	10 Ohm Resistor, 0603 Pkg.
U1	HMC673LC3C High Speed Logic, D-Type Flip-Flop
PCB [2]	118775 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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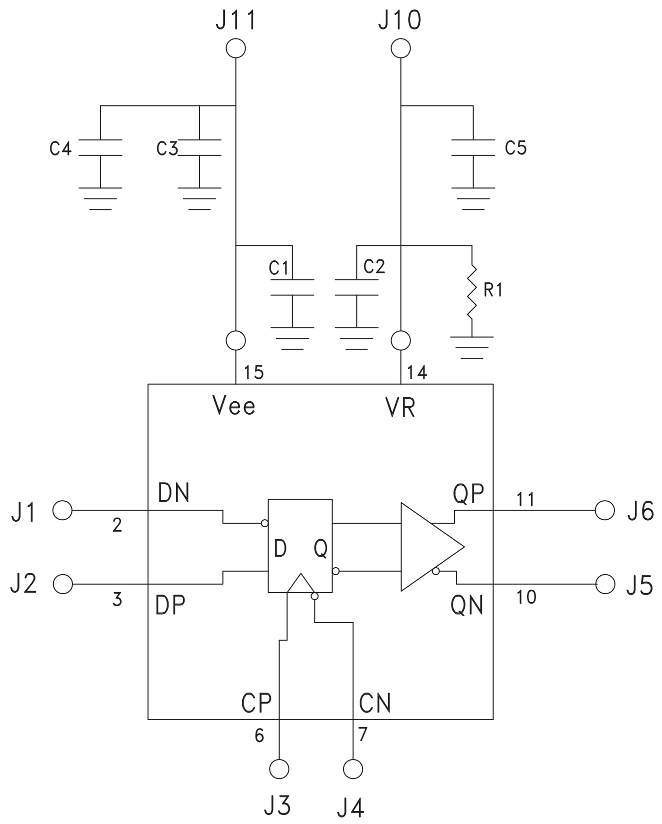
Application Circuit



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