

Typical Applications

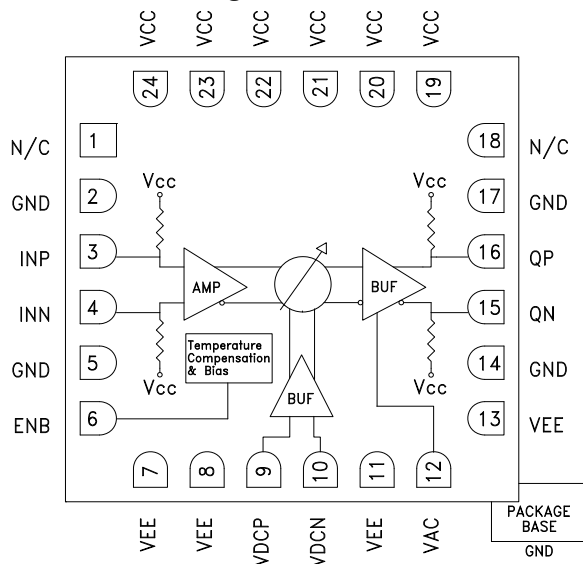
The HMC911LC4B is ideal for:

- Synchronization of clock and data
- Transponder design
- Serial Data Transmission up to 32 Gbps
- Broadband Test & Measurement
- RF ATE Applications

Features

- Very Wide Bandwidth: DC - 24 GHz
- Continuous Adjustable Delay Range: 70 ps
- Single-Ended or Differential Operation
- Adjustable Differential Output
Swing: up to 800mVp-p
- Delay Control Modulation Bandwidth: 1.6 GHz
- Single Supply: +3.3V
- 24 Lead Ceramic 4x4mm SMT Package: 16mm²

Functional Diagram



General Description

The HMC911LC4B is a broadband time delay with 0 to 70 ps continuously adjustable delay range. The delay control is linearly monotonic with respect to the differential delay control voltage (VDCP, VDCN) and the control input has a modulation bandwidth of 1.6 GHz. The device provides a differential output voltage with constant amplitude for single-ended or differential input voltages above the input sensitivity level, while the output voltage swing may be adjusted using the VAC control pin. The HMC911LC4B features internal temperature compensation and bias circuitry to minimize delay variations with temperature. All RF input and outputs of the HMC911LC4B are internally terminated with 50 Ohms to Vcc, and may either be AC or DC coupled. Output pins can be connected directly to a 50 Ohm to Vcc terminated system, while DC blocking capacitors must be used if the terminated system input is 50 Ohms to a DC voltage other than Vcc. The HMC911LC4B is available in RoHS-compliant 4x4 mm SMT package.

Electrical Specifications, $T_A=+25^\circ\text{C}$, $V_{CC}=3.3\text{V}$, $V_{AC}=2.6\text{V}$, $V_{EE}=GND=0\text{V}$

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supply Voltage	$\pm 5\%$ Tolerance	3.13	3.3	3.47	V
Power Supply Current		460		530	mA
Time Delay Range	VDCP=3.9V, VDCN=3.3V @ 10 GHz	62	70	71	ps
	VDCP=3.9V, VDCN=3.3V @ 18 GHz	64	70	73	ps
	VDCP=3.9V, VDCN=3.3V @ 22 GHz	66	70	75	ps
Phase Shift Range	VDCP=3.9V, VDCN=3.3V @ 10 GHz	210		250	Deg
	VDCP=3.9V, VDCN=3.3V @ 18 GHz	400		475	Deg
	VDCP=3.9V, VDCN=3.3V @ 22 GHz	515		595	Deg
Maximum Data Rate		32			Gbps
Maximum Clock Frequency		24			GHz



BROADBAND ANALOG TIME DELAY, DC - 24 GHz

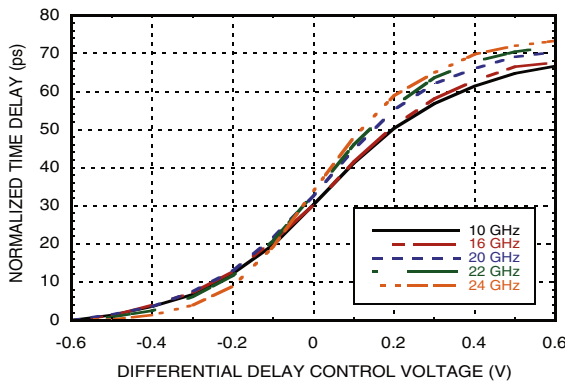
Electrical Specifications, $T_A=+25^\circ\text{C}$, $V_{CC}=3.3\text{V}$, $V_{AC}=2.6\text{V}$, $V_{EE}=\text{GND}=0\text{V}$ (Continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
Delay Control Modulation Bandwidth			1.6		GHz
Delay Control Voltage (VDCP, VDCN)		$V_{CC}-0.6$		$V_{CC}+0.6$	V
Input Low Voltage	VIL	$V_{CC}-500$	$V_{CC}-200$	$V_{CC}-25$	mV
Input High Voltage	VIH	$V_{CC}+25$	$V_{CC}+200$	$V_{CC}+500$	mV
Input Amplitude	Single-ended, peak-to-peak	50		1000	mVp-p
	Differential, peak-to-peak	100		2000	mVp-p
Output Amplitude Control Voltage (VAC)		1.7	2.6	2.7	V
Output Amplitude	Single-ended @ 10 GHz	370		640	mVpp
	Single-ended @ 18 GHz	350		640	mVpp
	Single-ended @ 20 GHz	340		640	mVpp
Harmonic Suppression* ($f_{in}-2f_{in}$) (f_{in} is the fundamental frequency)	VDCP=VDCN=3.3V @ 10 GHz	21		32	dBc
	VDCP=VDCN=3.3V @ 20 GHz	19		30	dBc
Input Return Loss	frequency < 24 GHz		9		dB
Output Return Loss	frequency < 24 GHz		10		dB
RMS Jitter	32 Gbps 10101... data		0.3		ps, pp
Rise Time, $t_r^{[1]}$			15		ps
Fall Time, $t_f^{[1]}$			14		ps
Propagation Delay, t_d	VDCP=2.7V, VDCN=3.3V (relative to zero time delay)		480		ps
Time Delay Voltage Sensitivity			116		ps/V
Time Delay Temperature Sensitivity	VDCP=VDCN=3.3V @ 18 GHz		0.04		ps/ $^\circ\text{C}$

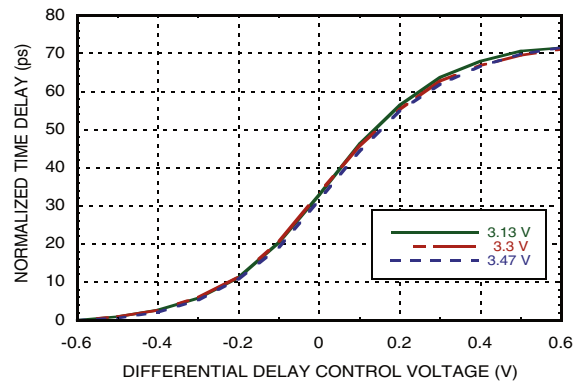
* Harmonic suppression measurements are taken for single-ended inputs and outputs

[1] V_{input} = Differential 400mVp-p, f_{data} = 22.5 Gbps PRBS 2²³-1

**Time Delay vs.
Delay Control Voltage** [1][2][3]



**Time Delay vs.
Delay Control Voltage @ 22GHz** [1][2][3]



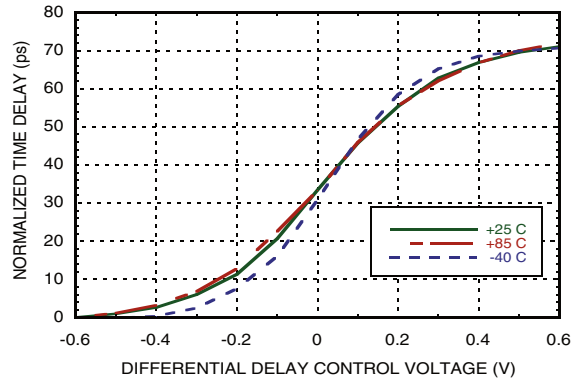
[1] $V_{AC} = 2.6\text{V}$, $V_{DCN}=3.3\text{V}$ [2] On the x-axis differential control voltage represents $V_{DCP}-V_{DCN}$ voltage

[3] $V_{CC}=3.3\text{V}$

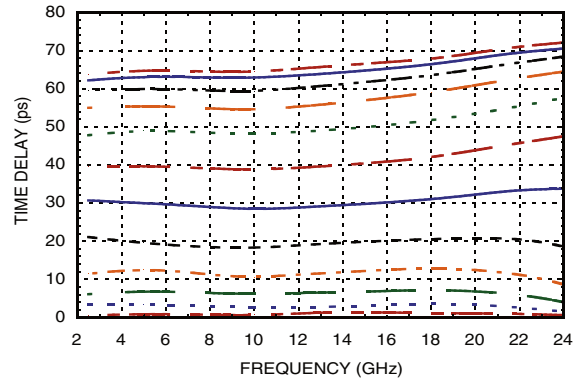


BROADBAND ANALOG TIME DELAY, DC - 24 GHz

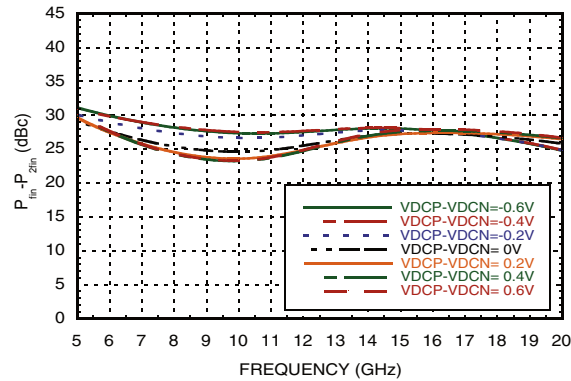
Time Delay vs. Delay Control Voltage @ 22GHz [1][2][3][4]



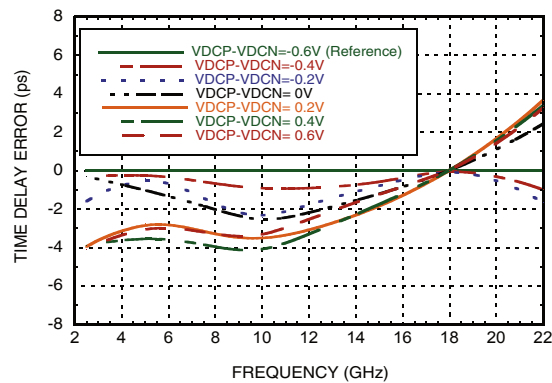
Time Delay vs. Frequency @VDCP=2.7V to 3.9V with 0.1V step [1][3]



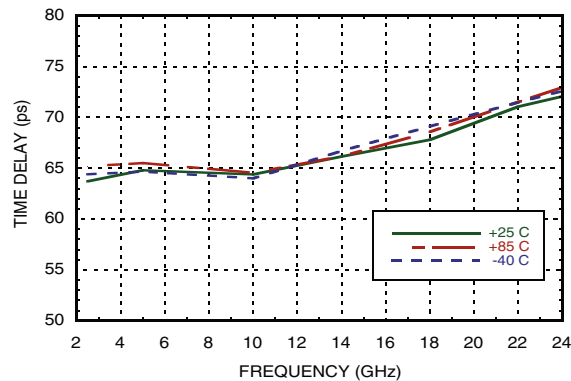
Second Harmonics vs. Frequency [1][3][4]



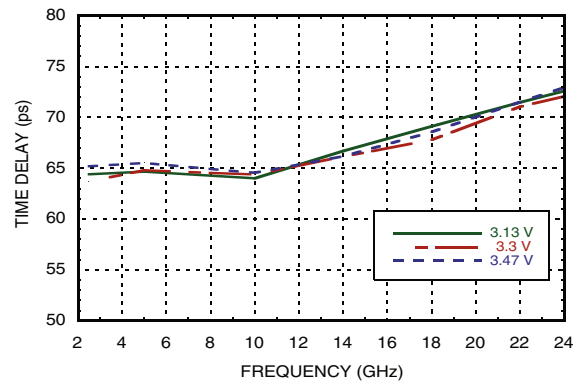
Time Delay Error vs. Frequency @ Fmean=18GHz [1][3]



Programmable Max. Time Delay Range vs. Frequency [1][3][5]



Programmable Max. Time Delay Range vs. Frequency [1][3][5]

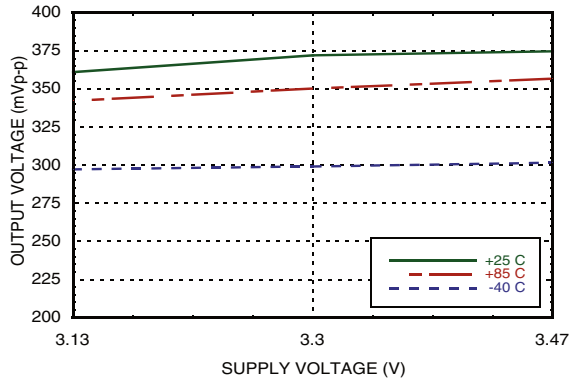


[1] VAC = 2.6V, VDCN=3.3V [2] On the x-axis differential control voltage represents VDCP-VDCN voltage
 [3] VCC=3.3V [4] fin is the fundamental frequency [5] VDCP=3.9V

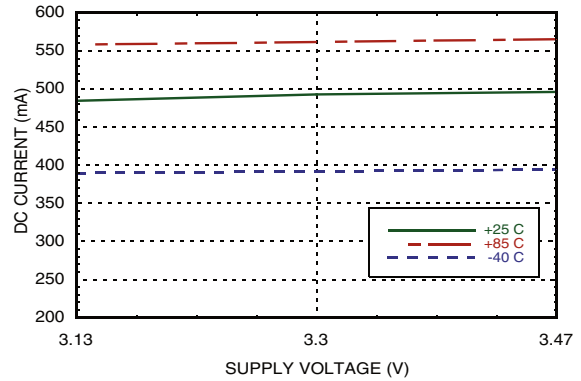


BROADBAND ANALOG TIME DELAY, DC - 24 GHz

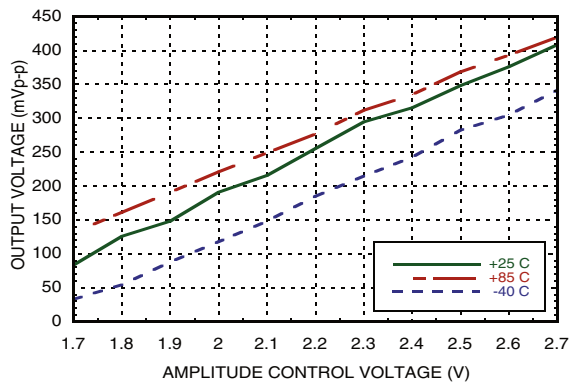
Single-Ended Output Swing vs. Supply Voltage [1][2][3]



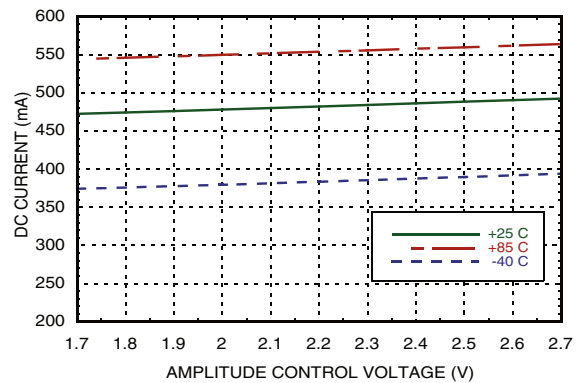
DC Current vs. Supply Voltage [1][2][3]



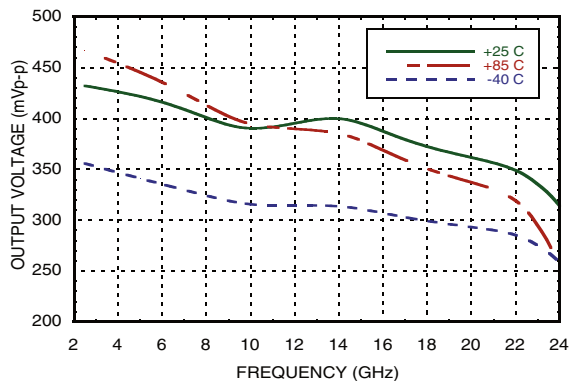
Single-Ended Output Swing vs. VAC [2][4][5]



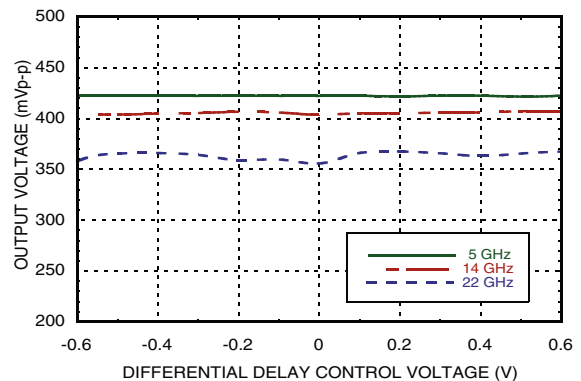
DC Current vs. VAC [2][4][5]



Single-Ended Output Swing vs. Frequency [1][2][4]



Single-Ended Output Swing vs. Delay Control Voltage [1][2][4][6]



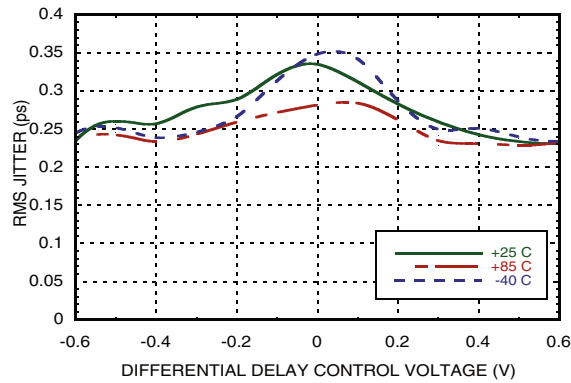
[1] VAC = 2.6V [2] VDCP= VDCN=3.3V [3] Input Frequency: 18 GHz
 [4] VCC=3.3V [5] Input Frequency: 10 GHz [6] On the x-axis differential control voltage represents VDCP-VDCN voltage

BROADBAND ANALOG TIME DELAY, DC - 24 GHz



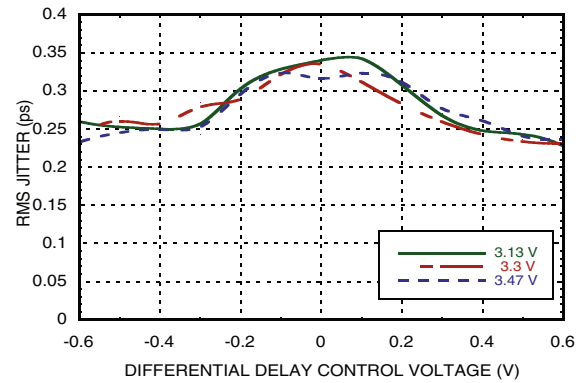
RMS Jitter vs. Delay Control Voltage

@ 18GHz [1][2][3][4]

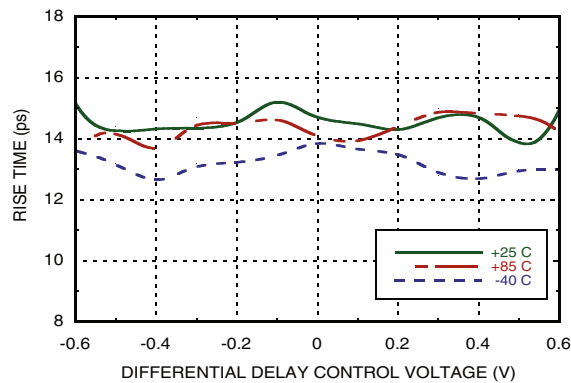


RMS Jitter vs. Delay Control Voltage

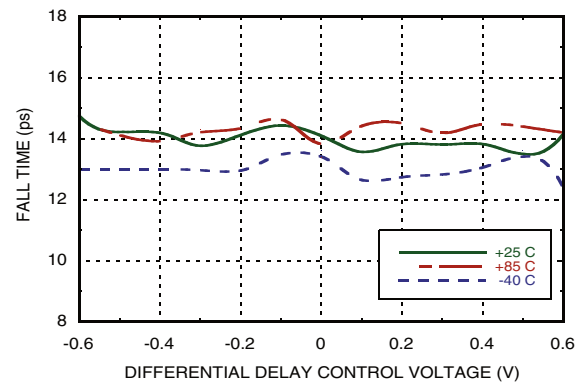
@ 18GHz [1][2][3][4]



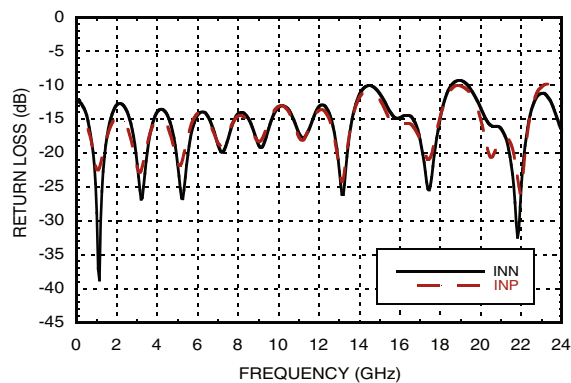
Rise Time vs. Delay Control Voltage [1][2][3][4][6]



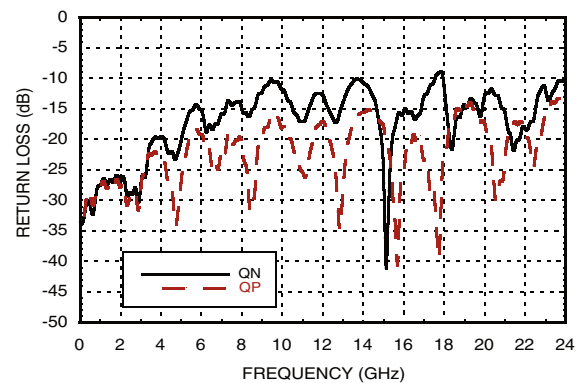
Fall Time vs. Delay Control Voltage [1][2][3][4][6]



Input Return Loss vs. Frequency [1][2][3]



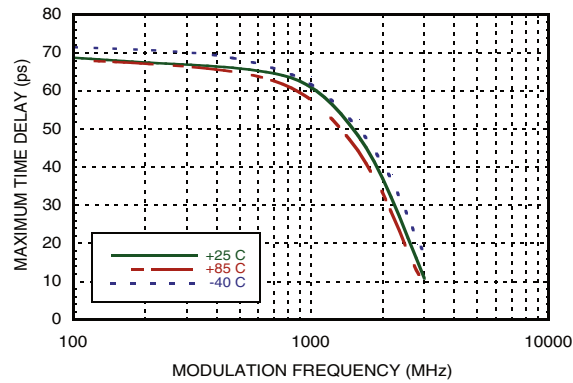
Output Return Loss vs. Frequency [1][2][3]



[1] VAC = 2.6V [2] VDCN=3.3V [3] VCC=3.3V
 [4] On the x-axis differential control voltage represents VDCP-VDCN voltage
 [5] Source jitter was not deembedded [6] Input Data Rate: 22.5 Gbps PRBS 2²³-1 [7] VDCP=3.3V



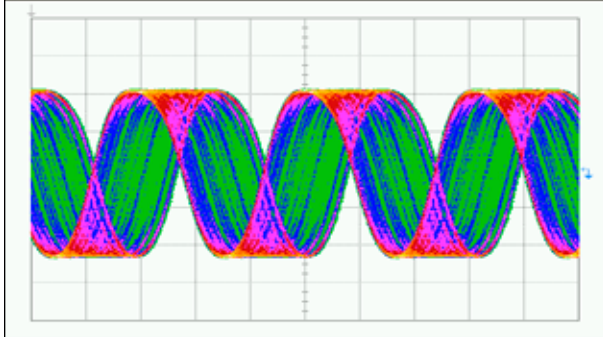
**Delay Modulation Amplitude vs.
Modulation Frequency ^{[1][2][3]}**



[1] VAC = 2.6V [2] VCC=3.3V
[3] Input Data Rate: 10Gbps PRBS 2²³-1, +6 dBm input power was applied to VDCP and VDCN terminated with 50 Ohms.

**BROADBAND ANALOG
TIME DELAY, DC - 24 GHz**

Output Eye Diagram Continuous Snapshot for 16 GHz Input

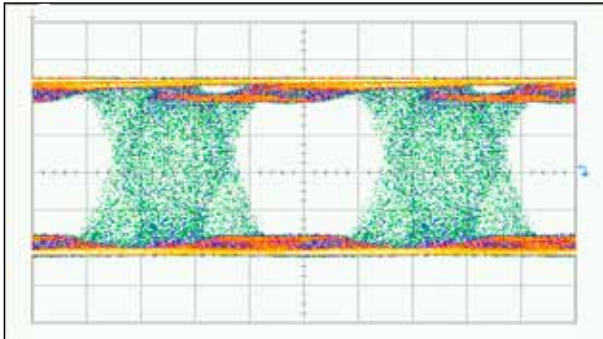


Time Scale: 20 ps/div
Amplitude Scale: 99.1 mV/div

Test Conditions:
VCC = 3.3V, VAC = 2.6V,
VDCP is varied from 2.7V to 3.3V
(%50 of the whole delay range)
Input Data: Single ended 400 mVp-p 16 GHz clock signal

Measurement Result:
Time Delay = 37 ps

Output Eye Diagram Continuous Snapshot for 10 Gbps Input



Time Scale: 20 ps/div
Amplitude Scale: 96.4 mV/div

Test Conditions:
VCC = 3.3V, VAC = 2.6V,
VDCP = 1200 mVp-p @ 1800 MHz
VDCN is 50 Ohms terminated

Input Data: Differential 400 mVp-p 10 Gbps NRZ
PRBS 2²³-1 pattern

Measurement Result:
Time Delay = 45.2 ps



BROADBAND ANALOG TIME DELAY, DC - 24 GHz

Absolute Maximum Ratings

Power Supply Voltage (V_{CC})	-0.5V to +3.75V
Input Voltage (V_{IN})	$V_{CC}-1.2V$ to $V_{CC}+0.6V$
Output Voltage (V_{OUT})	$V_{CC}-1.2V$ to $V_{CC}+0.6V$
Delay Control Voltage (V_{DCP} , V_{DCN})	0V to $V_{CC}+0.6V$
Power Down Pin (ENB)	0V to $V_{CC}+0.6V$
Amplitude Control Voltage (V_{AC})	0V to $V_{CC}+0.6V$
Channel Temperature (T_c)	125 °C
Continuous Pdiss ($T = 85$ °C) (derate 54.96 mW/°C above 85 °C)	2.2 W

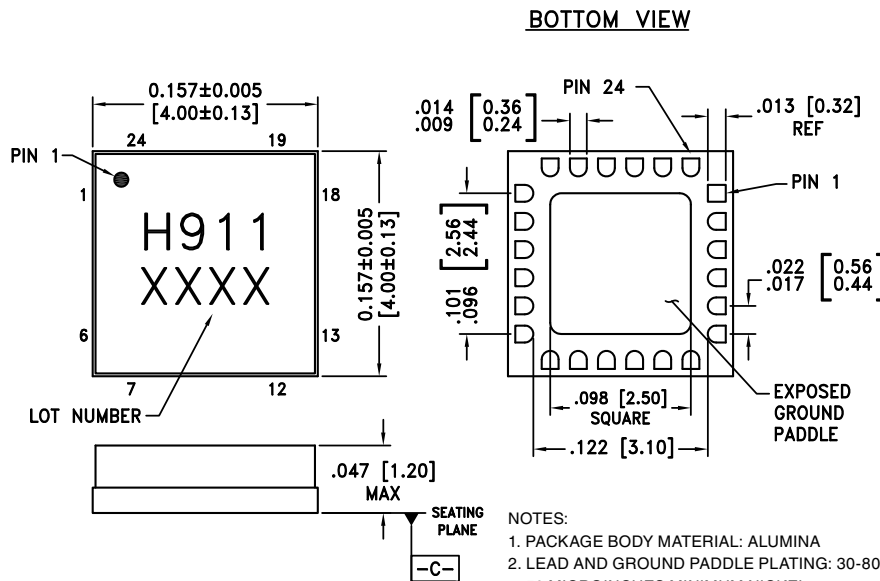
Absolute Maximum Ratings (continued)

Thermal Resistance (junction to ground paddle)	18.2 °C/W
Storage Temperature	-65 to +125 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1B



**ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS**


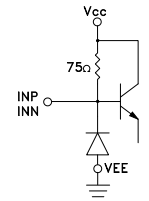
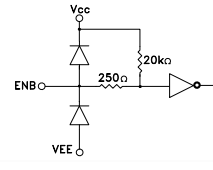
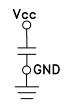
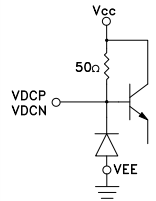
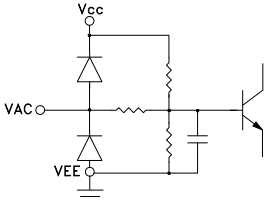
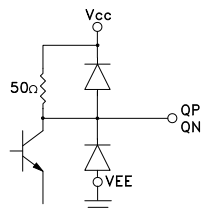
Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. CHARACTERS TO BE BLACK INK MARKED WITH .018"MIN to .030"MAX HEIGHT REQUIREMENTS. UTILIZE MAXIMUM CHARACTER HEIGHT BASED ON LID DIMENSIONS AND BEST FIT. LOCATE APPROX. AS SHOWN.
6. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
7. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Pin Descriptions

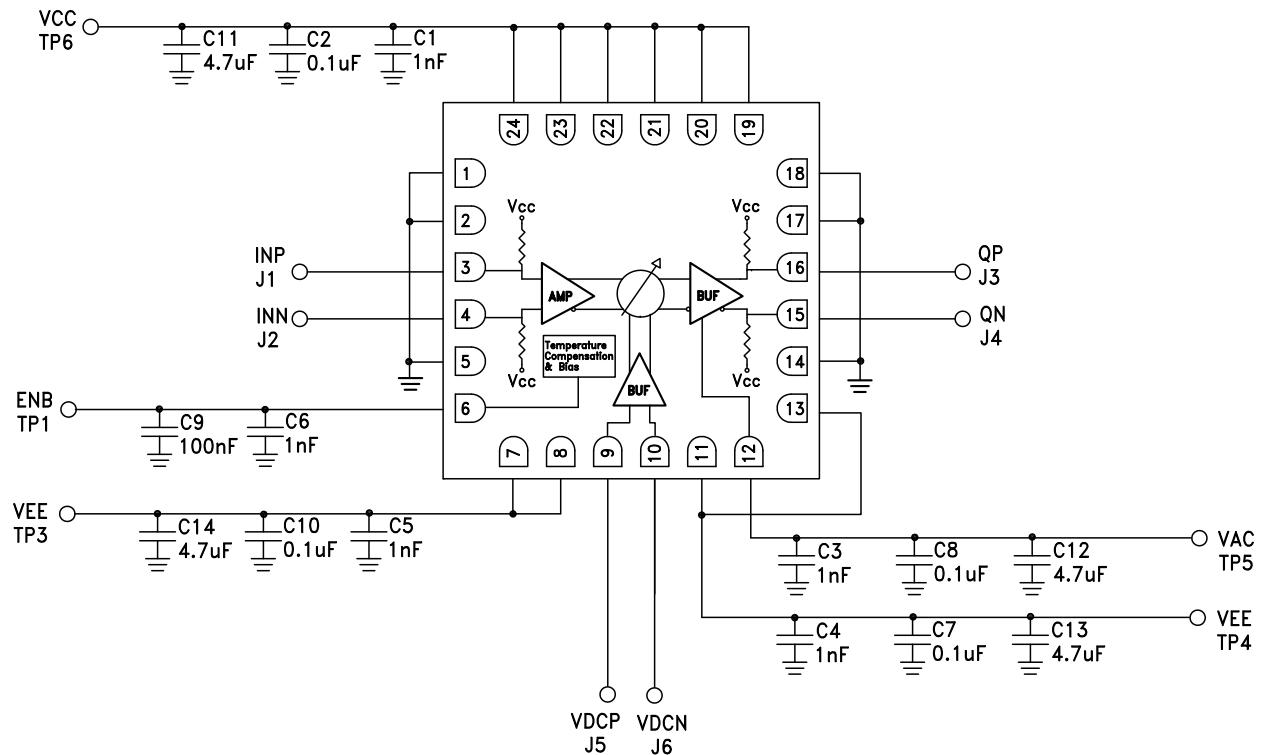
Pin Number	Function	Description	Interface Schematic
1, 18	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
2, 5, 14, 17, Package Bottom	GND	Signal grounds should be connected to 0V. Ground paddle must be connected to DC ground	
3-4	INP, INN	Differential Signal Inputs	
6	ENB	Enable pin for the time delay. For normal operation; leave the pin open or apply +3.3V. To disable the part apply 0V. When disabled total current consumption drops to 15mA.	
7, 8, 11, 13	VEE	Supply grounds should be connected to 0V.	
9, 10	VDCP VDCN	Differential time delay control pins.	
12	VAC	Output amplitude control pin.	
15, 16	QN, QP	Differential Signal Outputs	



Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
19 - 24	VCC	Positive supply	

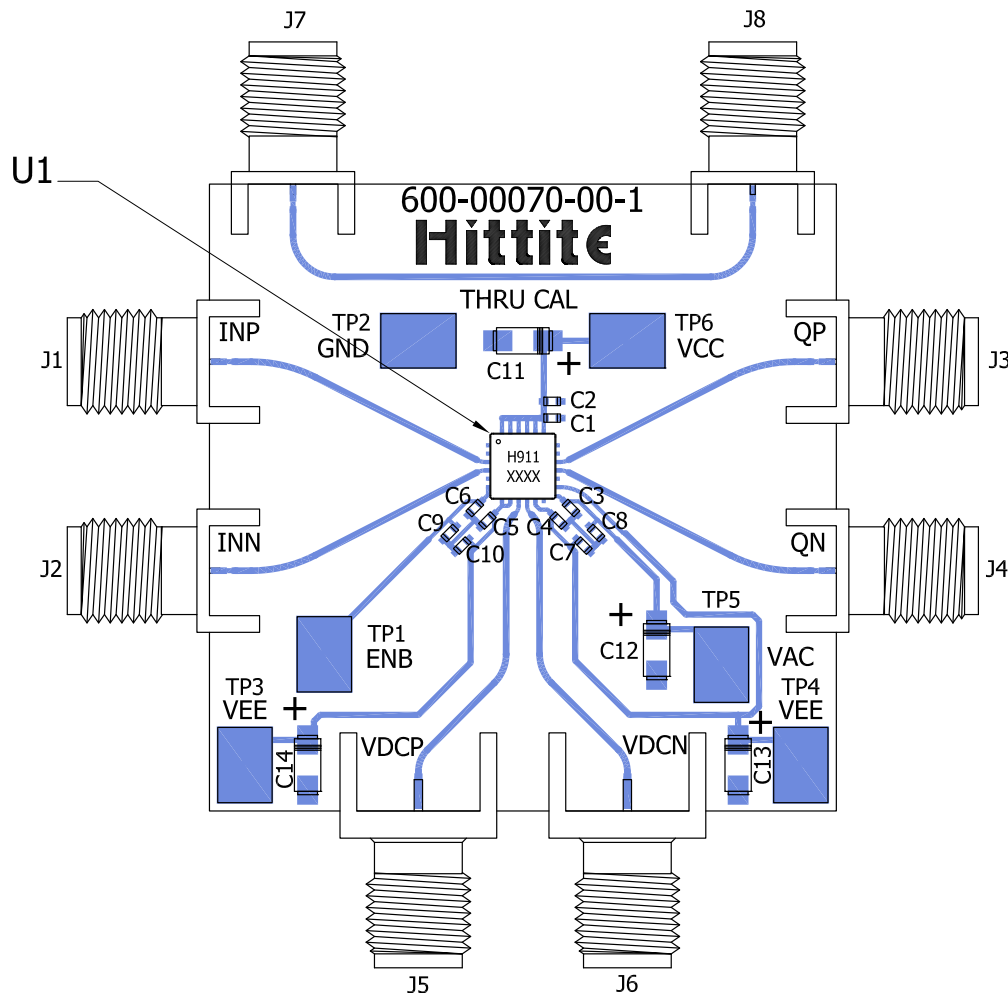
Application Circuit





**BROADBAND ANALOG
TIME DELAY, DC - 24 GHz**

Evaluation PCB



List of Materials for Evaluation PCB EVAL01-HMC911LC4B^[1]

Item	Description
J1 - J4	K Connector
J5 - J6	SMA Connector
TP1 - TP6	DC Test Point
C1, C3 - C6	1000 pF Capacitor, 0402 Pkg.
C2, C7 - C10	0.1 μF Capacitor, 0402 Pkg.
C11 - C14	4.7 μF Capacitor, Tantalum
U1	HMC911LC4B Analog Phase Shifter
PCB [2]	600-00070-00 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25 FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.