OCTAL 13/12-BIT 20/40/50 MSPS A/D CONVERTER

Features

- 50 MSPS Maximum Sampling Rate
- Ultra Low Power Dissipation
  - 23 mW/Channel at 20MSPS
  - 35 mW/Channel at 40MSPS
  - 41 mW/Channel at 50MSPS
- 72.2 dB SNR at 8 MHz FIN
- 0.5 µs Startup from Sleep, 15 µs from Power Down
- Reduced Power Dissipation Modes Available
- Internal Reference Circuitry with No External Components Required
- Coarse and Fine Gain Control
- Internal Offset Correction
- 1.8V Supply Voltage
- Serial LVDS Output
- 12 and 14-bit Output Available
- 64 Lead 9 x 9 mm SMT Package

Typical Applications

- Medical Imaging
- Wireless Infrastructure
- Test and Measurement
- Instrumentation

Pin Compatible Parts

- HMCAD1101
- HMCAD1102

Functional Diagram

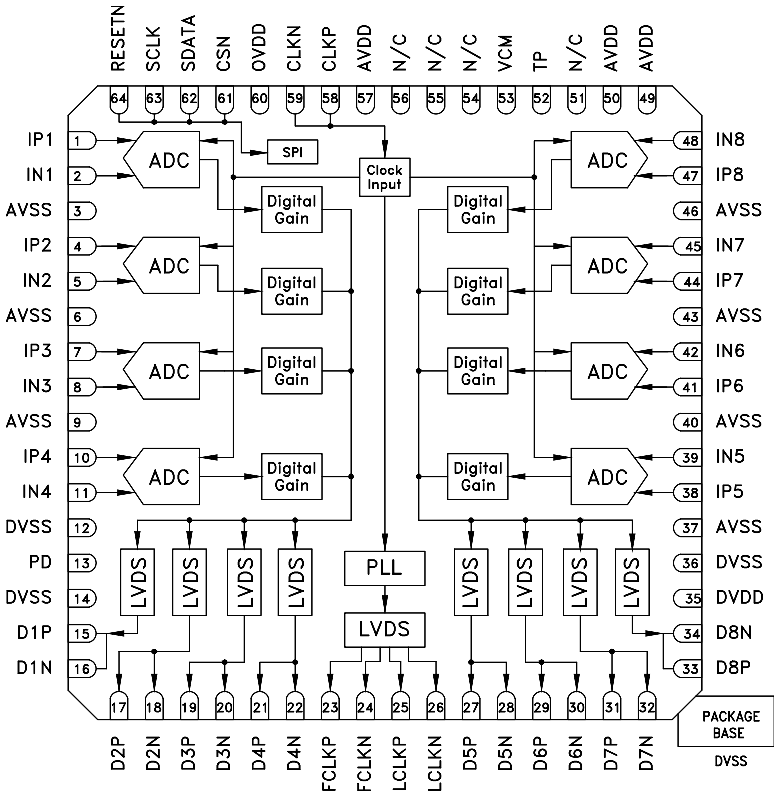

Figure 1. Functional Block Diagram

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OCTAL 13/12-BIT 20/40/50 MSPS A/D CONVERTER

General Description

HMCAD1100 is a high performance low power octal analog-to-digital converter (ADC). The ADC is based on a proprietary structure and employs internal reference circuitry, a serial control interface and serial LVDS output data. Data and frame synchronization output clocks are supplied for data capture at the receiver.

Various modes and configuration settings can be applied to the ADC through the serial control interface (SPI). Each channel can be powered down independently and data format can be selected through this interface. A full chip idle mode can be set by a single external pin. Register settings determine the exact function of this external pin.

There are two options for the serial LVDS outputs, 12- bit or 14-bit. In 12-bit mode, the LSB bit from the ADCs are removed in the output stream. In 14-bit mode, a ‘0’ is added in the LSB position.

The HMCAD1100 is designed to easily interface with field-programmable gate arrays (FPGAs) from several vendors.

The very low start up times for the HMCAD1100 allows significant power reduction in duty-cycled systems, by utilizing the Sleep Modes or Power Down Mode when the receive path is idle.

Electrical Specifications

DC Electrical Specifications

AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, 50MSPS clock, 50% clock duty cycle, -1 dBFS 8 MHz input signal, 14 bit output, unless otherwise noted

Parameter	Description	Min	Typ	Max	Unit
DC accuracy					
No Missing Codes		Guaranteed			
Offset Error	Offset error after internal digital offset correction		1		LSB
Gain Error				±6	%FS
Gain Matching	Gain matching between channels. ±3sigma value at worst case conditions		±0.5		%FS
DNL	Differential nonlinearity (12-bit level)		±0.2		LSB
INL	Integral nonlinearity (12-bit level)		±0.6		LSB
V_{CM}	Common mode voltage output		$V_{AVDD}/2$		
Analog Input					
Input Common Mode	Analog input common mode voltage	V_{CM} -0.1		V_{CM} +0.2	V
Full Scale Range	Differential input voltage range		2		Vpp
Input Capacitance	Differential input capacitance		2		pF
Bandwidth	Input Bandwidth	500			MHz
Power Supply					
Analog Supply Voltage		1.7	1.8	2	V
Digital Supply Voltage	Digital and output driver supply voltage	1.7	1.8	2	V
OVDD Supply Voltage	Digital CMOS Input Supply Voltage	1.7	1.8	3.6	V
Temperature					
Operating Temperature	Operating free-air temperature	-40		85	°C

AC Electrical Specifications - 20 MSPS

AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, 20 MSPS clock, 50% clock duty cycle, -1 dBFS 8 MHz input signal, 14 bit output, unless otherwise noted

Parameter	Description	Min	Typ	Max	Unit
Performance					
SNR	Signal to Noise Ratio				
	F_{IN} = 8 MHz	70	72.2		dBFS
	F_{IN} = 30 MHz		71.5		dBFS
SINAD	Signal to Noise and Distortion Ratio				
	F_{IN} = 8 MHz	69	71.5		dBFS
	F_{IN} = 30 MHz		70.7		dBFS
SFDR	Spurious Free Dynamic Range				
	F_{IN} = 8 MHz	75	82		dBc
	F_{IN} = 30 MHz		77		dBc
HD2	Second order Harmonic Distortion				
	F_{IN} = 8 MHz	85	95		dBc
	F_{IN} = 30 MHz		95		dBc
HD3	Third order Harmonic Distortion				
	F_{IN} = 8 MHz	75	82		dBc
	F_{IN} = 30 MHz		77		dBc
ENOB	Effective number of Bits				
	F_{IN} = 8 MHz		11.6		bits
	F_{IN} = 30 MHz		11.5		bits
Crosstalk	Signal applied to 7 channels (F_{IN0}). Measurement taken on one channel with full scale at F_{IN1}. F_{IN1} = 8 MHz, F_{IN0} = 9.9 MHz		95		dBc
Power Supply					
Analog Supply Current			47		mA
Digital Supply Current	Digital and output driver supply		54		mA
Analog Power Dissipation			84		mW
Digital Power Dissipation			97		mW
Total Power Dissipation			180		mW
Power Down Dissipation	Power down mode dissipation		10		µW
Sleep Mode Dissipation	Deep sleep mode power dissipation		30		mW
Sleep Channel Mode Dissipation	Power dissipation with all channels in sleep channel mode (Light sleep)		46		mW
Sleep Channel Savings	Power dissipation savings per channel off		17		mW
Clock Inputs					
Max. Conversion Rate		20			MSPS
Min. Conversion Rate				15	MSPS

AC Electrical Specifications - 40 MSPS

AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, 40 MSPS clock, 50% clock duty cycle, -1 dBFS 8 MHz input signal, 14 bit output, unless otherwise noted

Parameter	Description	Min	Typ	Max	Unit
Performance					
SNR	Signal to Noise Ratio				
	F_{IN} = 8 MHz	70	72.2		dBFS
	F_{IN} = 30 MHz		71.5		dBFS
SINAD	Signal to Noise and Distortion Ratio				
	F_{IN} = 8 MHz	69	71.5		dBFS
	F_{IN} = 30 MHz		70.7		dBFS
SFDR	Spurious Free Dynamic Range				
	F_{IN} = 8 MHz	75	82		dBc
	F_{IN} = 30 MHz		77		dBc
HD2	Second order Harmonic Distortion				
	F_{IN} = 8 MHz	85	95		dBc
	F_{IN} = 30 MHz		95		dBc
HD3	Third order Harmonic Distortion				
	F_{IN} = 8 MHz	75	82		dBc
	F_{IN} = 30 MHz		77		dBc
ENOB	Effective number of Bits				
	F_{IN} = 8 MHz		11.6		bits
	F_{IN} = 30 MHz		11.5		bits
Crosstalk	Signal applied to 7 channels (F_{IN0}). Measurement taken on one channel with full scale at F_{IN1}. F_{IN1} = 8 MHz, F_{IN0} = 9.9 MHz		95		dBc
Power Supply					
Analog Supply Current			90		mA
Digital Supply Current	Digital and output driver supply		67		mA
Analog Power Dissipation			162		mW
Digital Power Dissipation			120		mW
Total Power Dissipation			280		mW
Power Down Dissipation	Power down mode dissipation		10		µW
Sleep Mode Dissipation	Deep sleep mode power dissipation		41		mW
Sleep Channel Mode Dissipation	Power dissipation with all channels in sleep channel mode (Light sleep)		71		mW
Sleep Channel Savings	Power dissipation savings per channel off		26		mW
Clock Inputs					
Max. Conversion Rate		40			MSPS
Min. Conversion Rate				20	MSPS

AC Electrical Specifications - 50 MSPS

AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, 50 MSPS clock, 50% clock duty cycle, -1 dBFS 8 MHz input signal, 14 bit output, unless otherwise noted

Parameter	Description	Min	Typ	Max	Unit
Performance					
SNR	Signal to Noise Ratio				
	F_{IN} = 8 MHz	70	72.2		dBFS
	F_{IN} = 30 MHz		71.5		dBFS
SINAD	Signal to Noise and Distortion Ratio				
	F_{IN} = 8 MHz	69	71.5		dBFS
	F_{IN} = 30 MHz		70.7		dBFS
SFDR	Spurious Free Dynamic Range				
	F_{IN} = 8 MHz	75	82		dBc
	F_{IN} = 30 MHz		77		dBc
HD2	Second order Harmonic Distortion				
	F_{IN} = 8 MHz	85	95		dBc
	F_{IN} = 30 MHz		95		dBc
HD3	Third order Harmonic Distortion				
	F_{IN} = 8 MHz	75	82		dBc
	F_{IN} = 30 MHz		77		dBc
ENOB	Effective number of Bits				
	F_{IN} = 8 MHz		11.6		bits
	F_{IN} = 30 MHz		11.5		bits
Crosstalk	Signal applied to 7 channels (F_{IN0}). Measurement taken on one channel with full scale at F_{IN1}. F_{IN1} = 8 MHz, F_{IN0} = 9.9 MHz		95		dBc
Power Supply					
Analog Supply Current			111		mA
Digital Supply Current	Digital and output driver supply		73		mA
Analog Power Dissipation			200		mW
Digital Power Dissipation			132		mW
Total Power Dissipation			331		mW
Power Down Dissipation	Power down mode dissipation		10		µW
Sleep Mode Dissipation	Deep sleep mode power dissipation		46		mW
Sleep Channel Mode Dissipation	Power dissipation with all channels in sleep channel mode (Light sleep)		83		mW
Sleep Channel Savings	Power dissipation savings per channel off		31		mW
Clock Inputs					
Max. Conversion Rate		50			MSPS
Min. Conversion Rate				20	MSPS

Digital and Switching Specifications

AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, unless otherwise noted

Parameter	Description	Min	Typ	Max	Unit
Clock Inputs					
Duty Cycle		20		80	% high
Compliance		CMOS, LVDS, LVPECL			
Input range, diff	Differential input swing	±200			mVpp
Input range, sine	Differential input swing, sine wave clock input	±800			mVpp
Input range, CMOS	Voltage input range CMOS (CLKN connected to ground)		V_{OVDD}		
Input common mode voltage	Keep voltages within ground and voltage of OVDD	0.3		V_{OVDD} -0.3	V
Input capacitance	Differential		2		pF
Logic inputs (CMOS)					
V_{HI}	High Level Input Voltage. $V_{OVDD} \geq 3.0V$	2			V
V_{HI}	High Level Input Voltage. V_{OVDD} = 1.7V – 3.0V	$0.8 \cdot V_{OVDD}$			V
V_{LI}	Low Level Input Voltage. $V_{OVDD} \geq 3.0V$	0		0.8	V
V_{LI}	Low Level Input Voltage. V_{OVDD} = 1.7V – 3.0V	0		$0.2 \cdot V_{OVDD}$	V
I_{HI}	High Level Input leakage Current			±10	µA
I_{LI}	Low Level Input leakage Current			±10	µA
C_I	Input Capacitance		3		pF
Data outputs (LVDS)					
Compliance		LVDS			
V_{OUT}	Differential output voltage		350		mV
V_{CM}	Output common mode voltage		1.2		V
Output coding	Default/optional	Offset Binary/ 2's complement			
Timing Characteristics					
Aperture delay			0.8		ns
Aperture jitter			<0.5		ps
T_{SU}	Start up time from Power Down Mode and Deep Sleep Mode to Active Mode. References have reached 99% of final value. See section "Clock Frequency"	260		992	clock cycles
	Start up time from Power Down Mode and Deep Sleep Mode to Active Mode in µs.		15		µs
T_{SLPCH}	Start up time from Sleep Channel Mode to Active Mode		0.5		µs
T_{OVR}	Out of range recovery time		1		clock cycles
T_{LAT}	Pipeline delay	14			clock cycles
LVDS Output Timing Characteristics					
t_{data}	LCLK to data delay time (excluding programmable phase shift)		250		ps
T_{PROP}	Clock propagation delay.	$7^*T_{LVDS} + 2.6$	$7^*T_{LVDS} + 3.5$	$7^*T_{LVDS} + 4.2$	ns
	LVDS bit-clock duty-cycle	45		55	%LCLK cycle
	Frame clock cycle-to-cycle jitter			2.5	%LCLK cycle
T_{EDGE}	Data rise- and fall time 20% to 80%		0.4		ns
$T_{CLKEDGE}$	Clock rise- and fall time 20% to 80%		0.4		ns

Absolute Maximum Ratings

Applying voltages to the pins beyond those specified in Table 1 could cause permanent damage to the circuit.

Table 1: Absolute Maximum Ratings

Pin	Reference pin	Rating
AVDD	AVSS	-0.3V to +2.3V
DVDD	DVSS	-0.3V to +2.3V
OVDD	AVSS	-0.3V to +3.9V
AVSS / DVSS	DVSS / AVSS	-0.3V to +0.3V
Analog inputs and outputs	AVSS	-0.3V to +2.3V
CLKx	AVSS	-0.3V to +3.9V
LVDS outputs	DVSS	-0.3V to +2.3V
Digital inputs	DVSS	-0.3V to +3.9V

Table 2: Maximum Temperature Ratings

Operating Temperature	-40 to +85 °C
Storage Temperature	-60 to +150 °C
Maximum Junction Temperature	110 °C
Thermal Resistance (Rth)	25 °C/W
Soldering Profile Qualification	J-STD-020
ESD Sensivity HBM	Class 1C
ESD Sensivity CDM	Class III

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration and Description

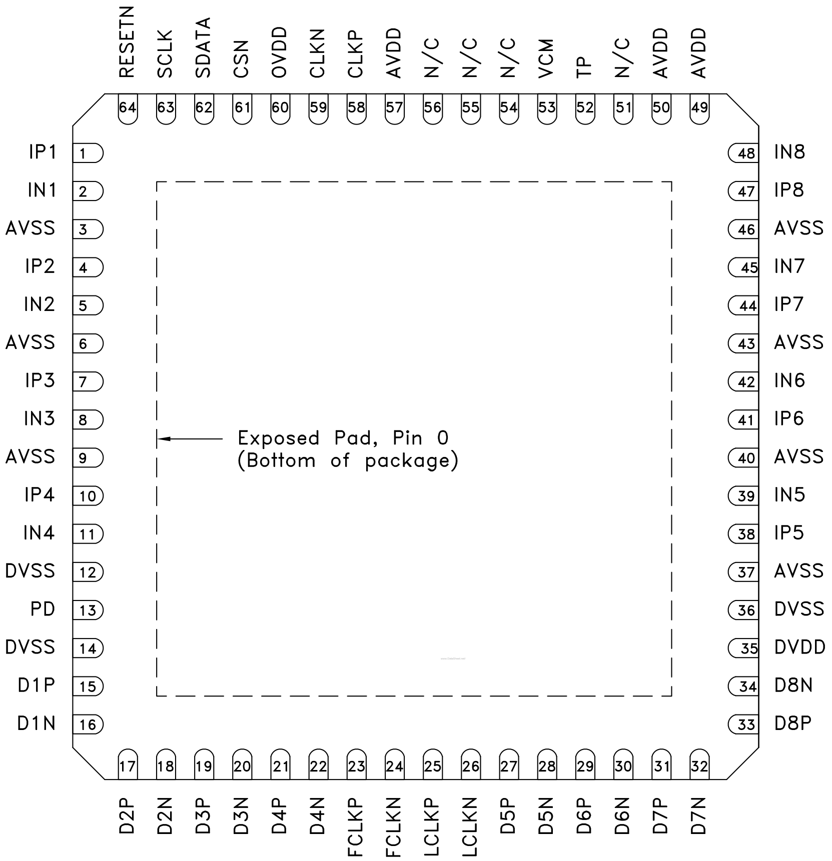

Figure 2. Package Diagram

Table 3: Pin Descriptions

Pin Number	Function	Description
49, 50, 57	AVDD	Analog power supply, 1.8V
60	OVDD	Digital CMOS Inputs supply voltage
3, 6, 9, 37, 40, 43, 46	AVSS	Analog ground
1	IP1	Positive differential input signal, channel 1
2	IN1	Negative differential input signal, channel 1
4	IP2	Positive differential input signal, channel 2
5	IN2	Negative differential input signal, channel 2
7	IP3	Positive differential input signal, channel 3
8	IN3	Negative differential input signal, channel 3
10	IP4	Positive differential input signal, channel 4
11	IN4	Negative differential input signal, channel 4
38	IP5	Positive differential input signal, channel 5
39	IN5	Negative differential input signal, channel 5
41	IP6	Positive differential input signal, channel 6
42	IN6	Negative differential input signal, channel 6

Table 3: Pin Descriptions

Pin Number	Function	Description
44	IP7	Positive differential input signal, channel 7
45	IN7	Negative differential input signal, channel 7
47	IP8	Positive differential input signal, channel 8
48	IN8	Negative differential input signal, channel 8
0, 12, 14, 36	DVSS	Digital ground
35	DVDD	Digital and I/O power supply, 1.8V
13	PD	Power-down input. Activate after applying power in order to initialize the ADC correctly. Alternatively use the SPI power down feature
15	D1P	LVDS channel 1, positive output
16	D1N	LVDS channel 1, negative output
17	D2P	LVDS channel 2, positive output
18	D2N	LVDS channel 2, negative output
19	D3P	LVDS channel 3, positive output
20	D3N	LVDS channel 3, negative output
21	D4P	LVDS channel 4, positive output
22	D4N	LVDS channel 4, negative output
27	D5P	LVDS channel 5, positive output
28	D5N	LVDS channel 5, negative output
29	D6P	LVDS channel 6, positive output
30	D6N	LVDS channel 6, negative output
31	D7P	LVDS channel 7, positive output
32	D7N	LVDS channel 7, negative output
33	D8P	LVDS channel 8, positive output
34	D8N	LVDS channel 8, negative output
23	FCLKP	LVDS frame clock (1X), positive output
24	FCLKN	LVDS frame clock (1X), negative output
25	LCKP	LVDS bit clock, positive output
26	LCKN	LVDS bit clock, negative output
51	NC	Not connected
52	TP	Test pin, leave unconnected or connect to ground
53	VCM	Common mode output pin, 0.5*AVDD
54	NC	Not connected
55	NC	Not connected
56	NC	Not connected
58	CLKP	Positive differential input clock
59	CLKN	Negative differential input clock.
61	CSN	Chip select enable. Active low
62	SDATA	Serial data input
63	SCLK	Serial clock input
64	RESETN	Reset SPI interface. Active low

Serial Interface

The HMCAD1100 configuration registers can be accessed through a serial interface formed by the pins SDATA (serial interface data), SCLK (serial interface clock) and CSN (chip select, active low). The following occurs when CSN is set low:

- Serial data are shifted into the chip
- At every rising edge of SCLK, the value present at SDATA is latched
- SDATA is loaded into the register every 24th rising edge of SCLK

Multiples of 24-bit words data can be loaded within a single active CSN pulse. If more than 24 bits are loaded into SDATA during one active CSN pulse, only the first 24 bits are kept. The excess bits are ignored. Every 24-bit word is divided into two parts:

- The first eight bits form the register address
- The remaining 16 bits form the register data

Acceptable SCLK frequencies are from 20 MHz down to a few hertz. Duty-cycle does not have to be tightly controlled.

Timing Diagram

Figure 4 shows the timing of the serial port interface. Table 5 explains the timing variables used in figure 4.

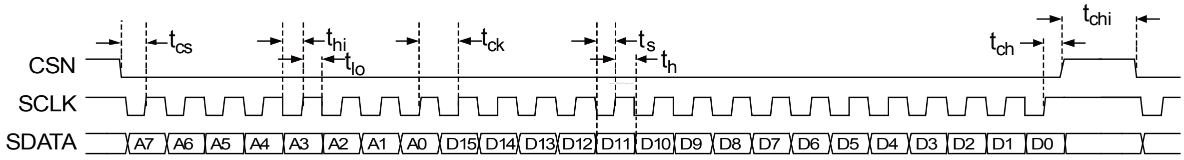

Figure 3. Serial Port Interface timing

Table 4: Serial Port Interface timing definitions

Parameter	Description	Minimum Value	Unit
t_{cs}	Setup time between CSN and SCLK	8	ns
t_{ch}	Hold time between CSN and SCLK	8	ns
t_{hi}	SCLK high time	20	ns
t_{lo}	SCLK low time	20	ns
t_{ck}	SCLK period	50	ns
t_s	Data setup time	5	ns
t_h	Data hold time	5	ns

Start up Initialization

As part of the HMCAD1100 power-on sequence both a reset and a power down cycle have to be applied to ensure correct start-up initialization. Make sure that the supply voltages are properly settled before the start up initialization is being performed. Reset can be done in one of two ways:

1. By applying a low-going pulse (minimum 20 ns) on the RESETN pin (asynchronous).
2. By using the serial interface to set the 'rst' bit high. Internal registers are reset to default values when this bit is set. The 'rst' bit is self-reset to zero. When using this method, do not apply any low-going pulse on the RESETN pin.

Power down cycling can be done in one of two ways:

1. By applying a high-going pulse (minimum 20 ns) on the PD pin (asynchronous).

2. By cycling the SPI register 0Fhex ‘pd’ bit to high (reg value ‘0200’hex) and then low (reg value ‘0000’hex).

Timing Diagrams

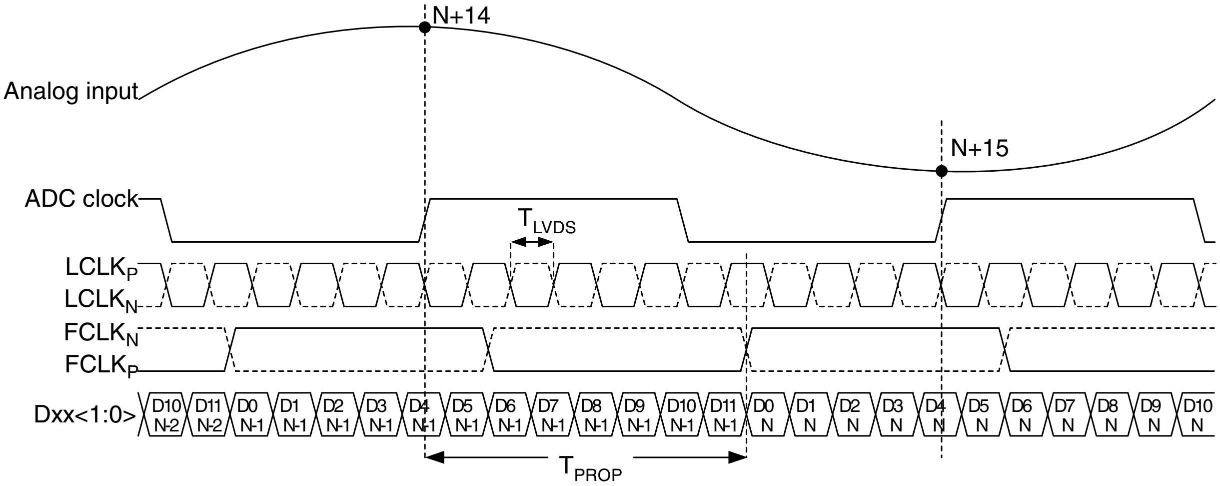

Figure 4. LVDS timing 12 bit output, DDR mode

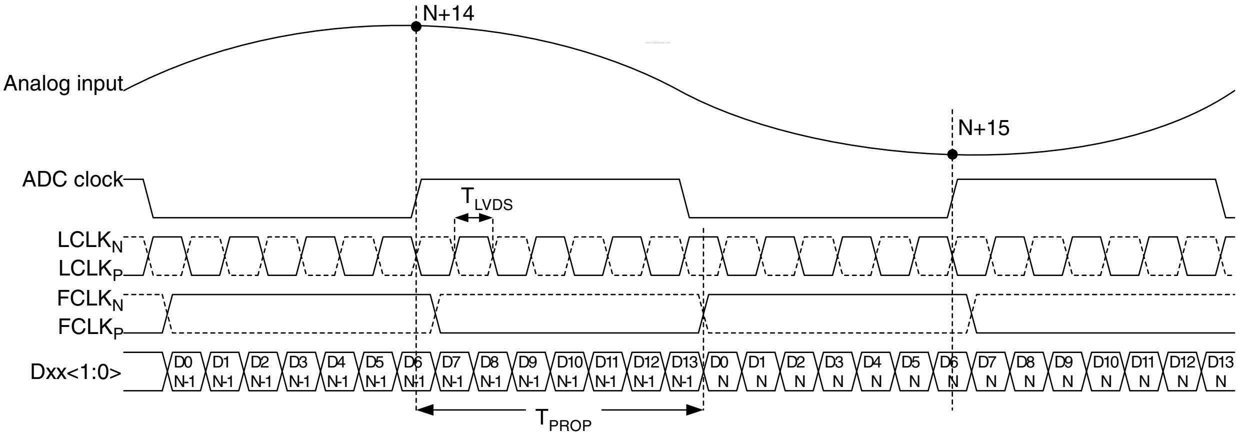

Figure 5. LVDS timing 14 bit output, DDR mode

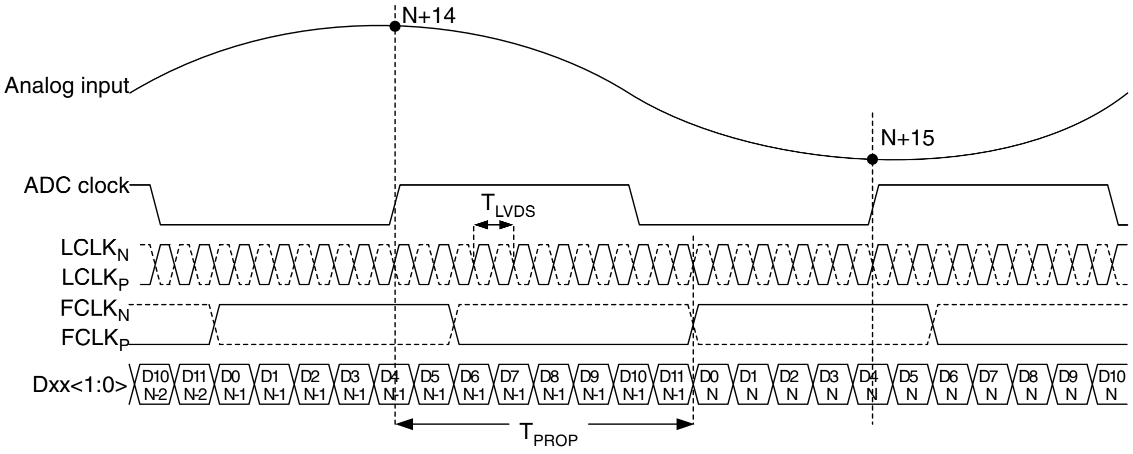

Figure 6. LVDS timing 12 bit output, SDR mode

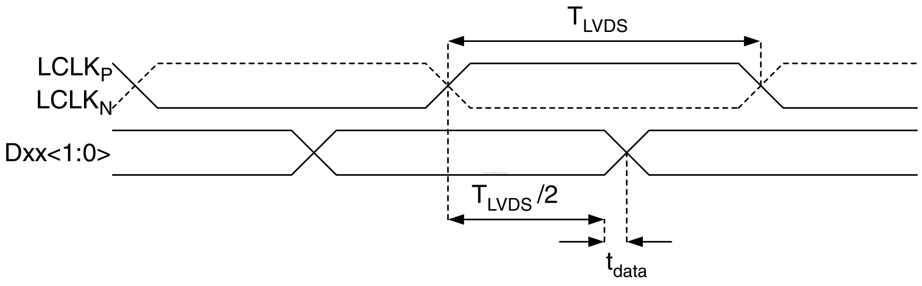

Figure 7. LVDS data timing, DDR mode

Serial Register Map

Table 5: Summary of functions supported by the serial interface

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
rst	Self-clearing software reset	Inactive																X	00
pd_ch <8:1>	Channel-specific power-down	Inactive									X	X	X	X	X	X	X	X	0F
sleep	Go to sleep-mode	Inactive								X									
pd	Go to power-down	Inactive							X										
pd_pin_cfg <1:0>	Configures the PD pin for sleep-modes	PD pin configured for power-down mode					X	X											
ilvds_lclk <2:0>	LVDS current drive programmability for LCLKP and LCLKN pins	3.5 mA drive														X	X	X	11
ilvds_ frame<2:0>	LVDS current drive programmability for FCLKP and FCLKN pins	3.5 mA drive										X	X	X					
ilvds_dat <2:0>	LVDS current drive programmability for output data pins	3.5 mA drive						X	X	X									

Table 5: Summary of functions supported by the serial interface

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
en_lvds_term	Enables internal termination for LVDS buffers	Termination disabled		X															12
term_lclk <2:0>	Programmable termination for LCLKN and LCLKP buffers	Termination disabled		1												X	X	X	
term_frame <2:0>	Programmable termination for FCLKN and FCLKP buffers	Termination disabled		1								X	X	X					
term_dat <2:0>	Programmable termination for output data buffers	Termination disabled		1				X	X	X									
invert_ch <8:1>	Swaps the polarity of the analog input pins	IPx is positive input									X	X	X	X	X	X	X	X	24
en_ramp	Enables a repeating full-scale ramp pattern on the outputs	Inactive										X	0	0					25
dual_custom_pat	Enables the mode wherein the output toggles between two defined codes	Inactive										0	X	0					
single_custom_pat	Enables the mode wherein the output is a constant specified code	Inactive										0	0	X					
bits_custom1 <13:0>	Bits for the single custom pattern and for the first code of the dual custom pattern. <0> is the LSB	Inactive	X	X	X	X	X	X	X	X	X	X	X	X	X	X			26
bits_custom2 <13:0>	Bits for the second code of the dual custom pattern	Inactive	X	X	X	X	X	X	X	X	X	X	X	X	X	X			27
gain_ch1 <3:0>	Programmable gain for channel 1	0dB gain													X	X	X	X	2A
gain_ch2 <3:0>	Programmable gain for channel 2	0dB gain									X	X	X	X					
gain_ch3 <3:0>	Programmable gain for channel 3	0dB gain					X	X	X	X									
gain_ch4 <3:0>	Programmable gain for channel 4	0dB gain	X	X	X	X													
gain_ch5 <3:0>	Programmable gain for channel 5	0dB gain	X	X	X	X													2B
gain_ch6 <3:0>	Programmable gain for channel 6	0dB gain					X	X	X	X									
gain_ch7 <3:0>	Programmable gain for channel 7	0dB gain									X	X	X	X					
gain_ch8 <3:0>	Programmable gain for channel 8	0dB gain													X	X	X	X	
phase_ddr <1:0>	Controls the phase of LCLK output relative to data	90 degrees										X	X						42
pat_deskew	Enables deskew pattern mode	Inactive															0	X	45
pat_sync	Enables sync pattern mode	Inactive															X	0	

Table 5: Summary of functions supported by the serial interface

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
btc_mode	Binary two's complement format for ADC output data	Straight offset binary														X			46
msb_first	Serialized ADC output data comes out with MSB first	LSB-first output													X				
en_sdr	Enable SDR output mode. LCLK becomes a 12X/14X input clock	DDR output mode												X					
fall_sdr	Rising edge of LCLK comes in the middle of the data window in SDR mode	Rising edge			X									1					
perfm_cntrl <2:0>	ADC performance control	Nominal														X	X	X	50
ext_vcm_bc <1:0>	VCM buffer driving strength control	Nominal											X	X					
lvds_pd_mode	Controls LVDS power down mode	High z mode																X	52
lvds_num_bits	Sets the number of LVDS output bits	12 bit															X		53
lvds_advance	Advance LVDS data bits and frame clock by one clock cycle	Inactive											0	X					
lvds_delay	Delay LVDS data bits and frame clock by one clock cycle	Inactive											X	0					
fs_cntrl <5:0>	Fine adjust ADC full scale range	0% change											X	X	X	X	X	X	55
clk_freq <1:0>	Input clock frequency	65 MHz															X	X	56

Description of Serial Registers

Software Reset

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
rst	Self-clearing software reset	Inactive																X	00

Setting the *rst* register bit to '1', resets all internal registers including the *rst* register bit itself.

Power-Down Modes

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
pd_ch <8:1>	Channel-specific power-down.	Inactive									X	X	X	X	X	X	X	X	0F
sleep	Go to sleep-mode.	Inactive								X									
pd	Go to power-down.	Inactive							X										
pd_pin_cfg <1:0>	Configures the PD pin for sleep-modes.	PD pin configured for power-down mode					X	X											
lvds_pd_mode	Controls LVDS power down mode	High z mode																X	52

There are several ways to power down HMCAD1100, from sleep modes with short start up time to full power down with extremely low power dissipation. There are two sleep modes, both with the LVDS clocks (FCLK, LCLK) running, such that the synchronization with the receiver is maintained. The first is a light sleep mode (*pd_ch<8:1>*) with short start up time, and the second a deep sleep mode (sleep) with the same start up time as full power down.

Setting *pd_ch<n>* = '1', sets channel <n> of the ADC in sleep mode. This is a light sleep mode with short start up time.

Setting sleep = '1', powers down all channels, but keeps FCLK and LCLK running to maintain LVDS synchronization. The start up time is the same as for complete power down. Power consumption is significantly lower than for setting *pd_ch*<8:1>='FFhex'.

Setting pd = '1' completely powers down the chip, including the band-gap reference circuit. Start-up time from this mode is significantly longer than from the *pd_ch<n>* mode. The synchronization with the LVDS receiver is lost since LCLK and FCLK outputs are put in high-Z mode.

Setting *pdn_pin_cfg*<1:0> = 'x1' configures the circuit to enter sleep channel mode (all channels off) when the PD pin is set high. This is equal to setting *pd_ch<8:1>*='FFhex'. The channels can not be powered down separately using the PD pin. Setting *pdn_pin_cfg*<1:0> = '10' configures the circuit to enter (deep) sleep mode when PD pin is set high (equal to setting sleep='1'. When *pdn_pin_cfg* <1:0>= '00', which is the default, the circuit enters power down mode when the PD pin is set high.

The *lvds_pd_mode* register configures whether the LVDS data output drivers are powered down or kept alive in sleep and sleep channel modes. LCLK and FCLK drivers are not affected by this register, and are always on in sleep and sleep channel modes. If *lvds_pd_mode* is set low (default), the LVDS output is put in high Z mode, and the driver is completely powered down. If lvds_pd_mode is set high, the LVDS output is set to constant 0, and the driver is still on during sleep and sleep channel modes.

LVDS Drive Strength Programmability

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
ilvds_lclk <2:0>	LVDS current drive programmability for LCLKP and LCLKN pins.	3.5 mA drive														X	X	X	11
ilvds_frame <2:0>	LVDS current drive programmability for FCLKP and FCLKN pins.	3.5 mA drive										X	X	X					
ilvds_dat <2:0>	LVDS current drive programmability for output data pins.	3.5 mA drive						X	X	X									

The current delivered by the LVDS output drivers can be configured as shown in table 6. The default current is 3.5 mA, which is what the LVDS standard specifies.

Setting the *ilvds_lclk*<2:0> register controls the current drive strength of the LVDS clock output on the LCLKP and LCLKN pins.

Setting the *ilvds_frame*<2:0> register controls the current drive strength of the frame clock output on the FCLKP and FCLKN pins.

Setting the *ilvds_dat*<2:0> register controls the current drive strength of the data outputs on the D[8:1]P and D[8:1]N pins.

Table 6: LVDS Output Drive Strength for LCLK, FCLK and Data

ilvds_*<2:0>	LVDS drive strength
000	3.5 mA (default)
001	2.5 mA
010	1.5 mA
011	0.5 mA
100	7.5 mA
101	6.5 mA
110	5.5 mA
111	4.5 mA

LVDS Internal Termination Programmability

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
en_lvds_ term	Enables internal termination for LVDS buffers	Termination disabled		X															12
term_lclk <2:0>	Programmable termination for LCLKN and LCLKP buffers	Termination disabled		1												X	X	X	
term_frame <2:0>	Programmable termination for FCLKN and FCLKP buffers	Termination disabled		1								X	X	X					
term_dat <2:0>	Programmable termination for DxP and DxN buffers	Termination disabled		1				X	X	X									

The off-chip load on the LVDS buffers may represent a characteristic impedance that is not perfectly matched with the PCB traces. This may result in reflections back to the LVDS outputs and loss of signal integrity. This effect can be mitigated by enabling an internal termination between the positive and negative outputs of each LVDS buffer. Internal termination mode can be selected by setting the *en_lvds_term* bit to '1'. Once this bit is set, the internal termination values for the bit clock, frame clock, and data buffers can be independently programmed using sets of three bits. Table 7 shows how the internal termination of the LVDS buffers are programmed. The values are typical values and can vary by up to ±20% from device to device and across temperature.

Table 7: LVDS Output Internal Termination for LCLK, FCLK and Data

term_*<2:0>	LVDS Internal Termination
000	Termination disabled
001	280Ω
010	165Ω
011	100Ω
100	125Ω
101	82Ω
110	67Ω
111	56Ω

Analog Input Invert

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
invert_ch <8:1>	Swaps the polarity of the analog input pins	IPx is positive input									X	X	X	X	X	X	X	X	24

The IPx pin represents the positive analog input pin, and INx represents the negative (complementary) input. Setting the bits marked *invert_ch*<8:1> (individual control for each channel) causes the inputs to be swapped. INx would then represent the positive input, and IPx the negative input.

LVDS Test Patterns

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
en_ramp	Enables a repeating full-scale ramp pattern on the outputs	Inactive										X	0	0					25
dual_custom_pat	Enables the mode wherein the output toggles between two defined codes	Inactive										0	X	0					
single_custom_pat	Enables the mode wherein the output is a constant specified code	Inactive										0	0	X					
bits_custom1 <13:0>	Bits for the single custom pattern and for the first code of the dual custom pattern. <0> is the LSB	Inactive	X	X	X	X	X	X	X	X	X	X	X	X	X	X			26
bits_custom2 <13:0>	Bits for the second code of the dual custom pattern	Inactive	X	X	X	X	X	X	X	X	X	X	X	X	X	X			27
pat_deskew	Enables deskew pattern mode	Inactive															0	X	45
pat_sync	Enables sync pattern mode	Inactive															X	0	

To ease the LVDS synchronization setup of HMCAD1100, several test patterns can be set up on the outputs. Normal ADC data are replaced by the test pattern in these modes. Setting *en_ramp* to '1' sets up a repeating full-scale ramp pattern on all data outputs. The ramp starts at code zero and is increased 1LSB every clock cycle. It returns to zero code and starts the ramp again after reaching the full-scale code.

A constant value can be set up on the outputs by setting *single_custom_pat* to '1', and programming the desired value in *bits_custom1*<13:0>. In this mode, *bits_custom1*<13:0> replaces the ADC data at the output, and is controlled by LSB-first and MSB-first modes in the same way as normal ADC data are.

The device may also be made to alternate between two codes by programming *dual_custom_pat* to '1'. The two codes are the contents of *bits_custom1*<13:0> and *bits_custom2*<13:0>. Two preset patterns can also be selected:

1. Deskew pattern: Set using *pat_deskew*, this mode replaces the ADC output with '01010101010101' (two LSBs removed in 12 bit mode).
2. Sync pattern: Set using *pat_sync*, the normal ADC word is replaced by a fixed '11111110000000' word ('111111000000' in 12 bit mode)

Note: Only one of the above patterns should be selected at the same time.

Programmable Gain

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
gain_ch1 <3:0>	Programmable gain for channel 1	0 dB gain													X	X	X	X	2A
gain_ch2 <3:0>	Programmable gain for channel 2	0 dB gain									X	X	X	X					
gain_ch3 <3:0>	Programmable gain for channel 3	0 dB gain					X	X	X	X									
gain_ch4 <3:0>	Programmable gain for channel 4	0 dB gain	X	X	X	X													
gain_ch5 <3:0>	Programmable gain for channel 5	0 dB gain	X	X	X	X													2B
gain_ch6 <3:0>	Programmable gain for channel 6	0 dB gain					X	X	X	X									
gain_ch7 <3:0>	Programmable gain for channel 7	0 dB gain									X	X	X	X					
gain_ch8 <3:0>	Programmable gain for channel 8	0 dB gain													X	X	X	X	

HMCAD1100 includes a purely digital programmable gain option in addition to the Full-scale Control. The programmable gain of each channel can be individually set using four bits, indicated as *gain_chx*<3:0> for Channel x. The gain setting is coded in binary from 0 dB to 12 dB, as shown in Table 8.

Table 8: Gain setting for channels 1-8

gain_chx <3:0>	Channel x Gain Setting
0000	0 dB
0001	1 dB
0010	2 dB
0011	3 dB
0100	4 dB
0101	5 dB
0110	6 dB
0111	7 dB
1000	8 dB
1001	9 dB
1010	10 dB
1011	11 dB
1100	12 dB
1101	Do not use
1110	Do not use
1111	Do not use

LVDS Clock Programmability and Data Output Modes

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
phase_ddr <1:0>	Controls the phase of LCLK output relative to data.	90 degrees.										X	X						42
btc_mode	Binary two's complement format for ADC output data.	Straight offset binary.														X			46
msb_first	Serialized ADC output data comes out with MSB first.	LSB-first output.													X				
en_sdr	Enable SDR output mode. LCLK becomes a 12X input clock.	DDR output mode.												X					
fall_sdr	Controls whether the LCLK rising or falling edge comes in the middle of the data window when operating in SDR mode.	Rising edge of LCLK comes in the middle of the data window.			X									1					

The output interface of HMCAD1100 is normally a DDR interface, with the LCLK rising and falling edge transitions in the middle of alternate data windows. The phase for LCLK can be programmed relative to the output frame clock and data bits using *phase_ddr*<1:0>. The LCLK phase modes are shown in figure 8. The default timing is identical to setting *phase_ddr*<1:0>='10'.

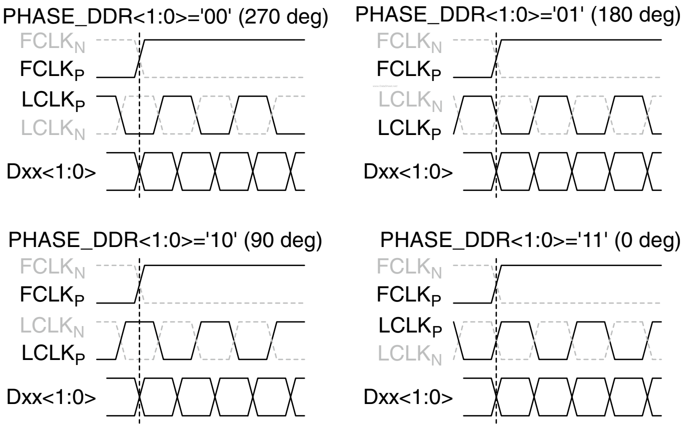

Figure 8. Phase programmability modes for LCLK

The device can also be made to operate in SDR mode by setting the *en_sdr* bit to '1'. The bit clock (LCLK) is output at 12x times the input clock in this mode, two times the rate in DDR mode. Depending on the state of *fall_sdr*, LCLK may be output in either of the two manners shown in Figure 10. As can be seen in Figure 10, only the LCLK rising (or falling) edge is used to capture the output data in SDR mode. The SDR mode is not recommended beyond 40 MSPS because the LCLK frequency becomes very high.

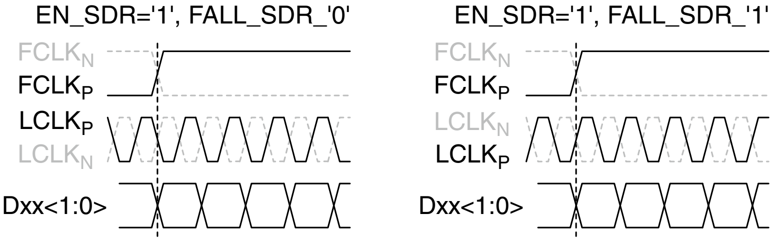

Figure 9. SDR interface modes

The default data output format is offset binary. Two's complement mode can be selected by setting the *btc_mode* bit to '1' which inverts the MSB.

The first bit of the frame (following the rising edge of FCLKP) is the LSB of the ADC output for default settings. Programming the *msb_first* mode results in reverse bit order, and the MSB is output as the first bit following the FCLKP rising edge.

Number of Serial Output Bits and LVDS output timing

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
lvds_num_bits	Sets the number of LVDS output bits	12 bit															X		53
lvds_advance	Advance LVDS data bits and frame clock by one clock cycle	Inactive											0	X					
lvds_delay	Delay LVDS data bits and frame clock by one clock cycle	Inactive											X	0					

The ADC channels have 13 bits of resolution. There are two options for the serial LVDS outputs, 12 bits or 14 bits, selected by setting *lvds_num_bits* to '0' or '1', respectively. In 12 bits mode, the LSB bit from the ADCs are removed in the output stream. In 14 bit mode, a '0' is added in the LSB position. Power down mode must be activated after or during a change in the number of output bits.

To ease timing in the receiver when using multiple ADC chips, HMCAD1100 has the option to adjust the timing of the output data and the frame clock. The propagation delay with respect to the ADC input clock can be moved one LVDS clock cycle forward or backward, by using lvds_delay and lvds_advance, respectively. See figure 10 for details. Note that LCLK is not affected by *lvds_delay* or *lvds_advance* settings.

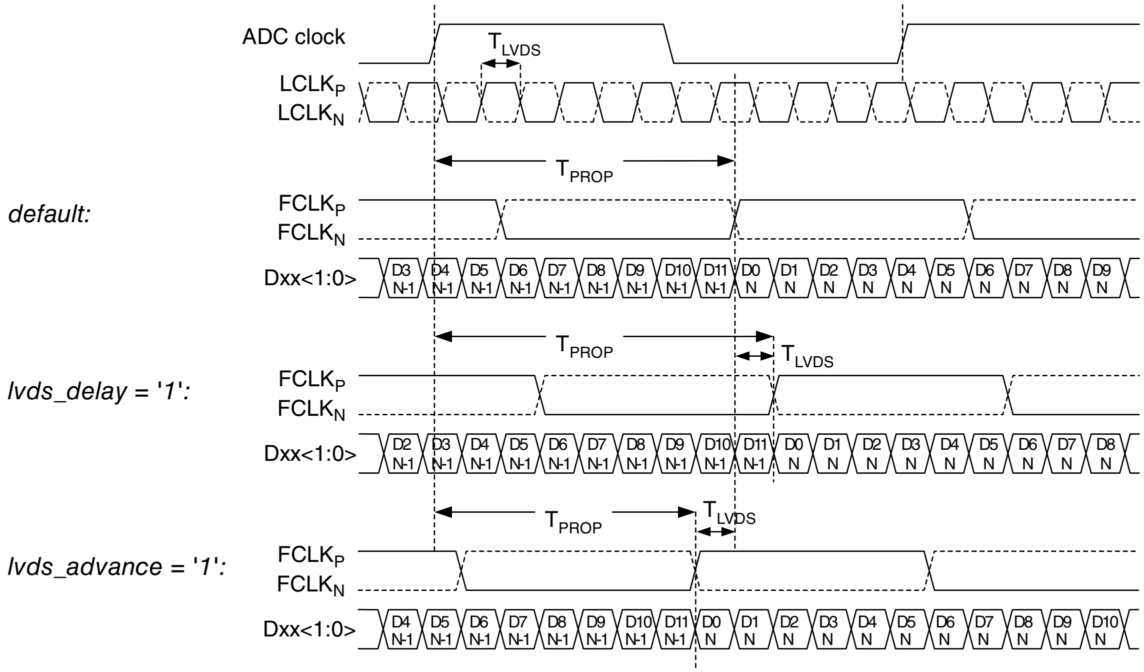

Figure 10. LVDS output timing adjustment

Full-Scale Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
fs_cntrl <5:0>	Fine adjust ADC full scale range	0% change											X	X	X	X	X	X	55

The full-scale voltage range of HMCAD1100 can be adjusted using an internal 6-bit DAC controlled by the fs_cntrl register. Changing the value in the register by one step, adjusts the full-scale range by approximately 0.3%. This leads to a maximum range of ±10% adjustment. Table 9 shows how the register settings correspond to the full-scale range. Note that the values for full-scale range adjustment are approximate. The DAC is, however, guaranteed to be monotonous.

The full-scale control and the programmable gain features differ in two major ways:

1. The full-scale control feature controls the full-scale voltage range in an analog fashion, whereas the programmable gain is a digital feature.
2. The programmable gain feature has much coarser gain steps and larger range than the full-scale control.

Table 10: Register values with corresponding change in full-scale range

Table 9: Register Values with Corresponding Change in Full-Scale Range

fs_cntrl<5:0>	Full-scale range adjustment
111111	9.70%
111110	9.40%
100001	0.30%
100000	0%
011111	–0.3%
000001	–9.7%
000000	–10%

To optimize start up time, a register is provided where the input clock frequency can be set. Some internal circuitry have start up times that are clock frequency independent. Default counter values are set to accommodate these start up times at the maximum clock frequency. This will lead to increased start up times at low clock frequency. Setting the value of this register to the nearest higher clock frequency will reduce the count values of the internal counters, to better fit the actual start up time, such that the start up time will be reduced. The start up times from Power Down mode and Deep Sleep mode are changed by this register setting.

Table 10: Clock frequency settings

clk_freq <1:0>		Clock frequency range	Startup delay (clock cycles)	Startup delay (µs)
0	0	50 - 80 MHz	992	12.4 - 19.8
0	1	32.5 - 50 MHz	640	12.8 - 19.7
1	0	20 - 32.5 MHz	420	12.9 - 21
1	1	15 - 20 MHz	260	13 - 17.3

Performance Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address In Hex
perfm_cntrl <2:0>	ADC performance control	Nominal														X	X	X	50
ext_vcm_bc <1:0>	VCM buffer driving strength control	Nominal											X	X					

There are two registers that impact performance and power dissipation.

The *perfm_cntrl* register adjusts the performance level of the ADC core. If full performance is required, the nominal setting must be used. The lowest code can be used in situations where power dissipation is critical and performance is less important. For most conditions the performance at the minimum setting will be similar to nominal setting. However, only 11 bit performance can be expected at worst case conditions. The power dissipation savings shown in table 11 are only approximate numbers for the ADC current alone.

Table 11: Performance Control Settings

perfm_cntrl <2:0>	Analog power dissipation
100	-40% (lower performance)
101	-30%
110	-20%

Table 11: Performance Control Settings

perfm_cntrl <2:0>	Analog power dissipation
111	-10%
000 (default)	Nominal
001	Do not use
010	Do not use
011	Do not use

The *ext_vcm_bc* register controls the driving strength in the buffer supplying the voltage on the VCM pin. If this pin is not in use, the buffer can be switched off. If current is drawn from the VCM pin, the driving strength can be increased to keep the voltage on this pin at the correct level.

Table 12: External Common Mode Voltage Buffer Driving Strength

ext_vcm_bc <1:0>	**VCM buffer driving strength [µA]** Max current sinked/sourced from VCM pin with < 50 mV voltage change.
00	Off (VCM floating)
01 (default)	±6.5
10	±70
11	±140

Theory of Operation

HMCAD1100 is an 8-channel, high-speed, CMOS ADC. The 13 bits given out by each channel are serialized to 12 or 14 bits and sent out on a single pair of pins in LVDS format. All eight channels of HMCAD1100 operate from one clock input, which can be differential or single ended. The sampling clocks for each of the eight channels are generated from the clock input using a carefully matched clock buffer tree. The 12x/14x clock required for the serializer is generated internally from FCLK using a phase-locked loop (PLL). A 6x/7x and 1x clock are also output in LVDS format, along with the data to enable easy data capture. HMCAD1100 uses internally generated references. The differential reference value is 1V. This results in a differential input of –1V to correspond to the zero code of the ADC, and a differential input of +1V to correspond to the full-scale code (code 8191).

The ADC employs a pipelined converter architecture. Each stage feeds its output data into the digital error correction logic, ensuring excellent differential linearity and no missing codes at 13-bit level.

HMCAD1100 operates from two sets of supplies and grounds. The analog supply and ground set is identified as AVDD and AVSS, while the digital set is identified by DVDD and DVSS.

Recommended Usage

Analog Input

The analog input to HMCAD1100 is a switched capacitor track-and-hold amplifier optimized for differential operation. Operation at common mode voltages at mid supply is recommended even if performance will be good for the ranges specified. The VCM pin provides a voltage suitable as common mode voltage reference. The internal buffer for the VCM voltage can be switched off, and driving capabilities can be changed programming the *ext_vcm_bc*<1:0> register.

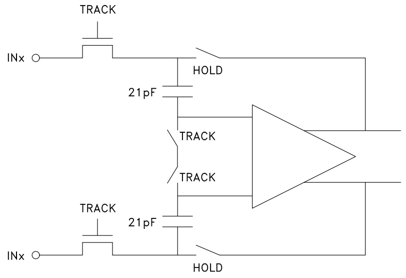

Figure 11. Input configuration

Figure 12 shows a simplified drawing of the input network. The signal source must have sufficiently low output impedance to charge the sampling capacitors within one clock cycle. A small external resistor (e.g. 22 Ohm) in series with each input is recommended as it helps reducing transient currents and dampens ringing behavior. A small differential shunt capacitor at the chip side of the resistors may be used to provide dynamic charging currents and may improve performance. The resistors form a low pass filter with the capacitor, and values must therefore be determined by requirements for the application.

DC-Coupling

Figure 13 shows a recommended configuration for DC-coupling. Note that the common mode input voltage must be controlled according to specified values. Preferably, the *CM_EXT* output should be used as reference to set the common mode voltage.

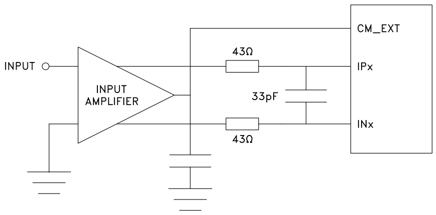

Figure 12. DC coupled input

The input amplifier could be inside a companion chip or it could be a dedicated amplifier. Several suitable single ended to differential driver amplifiers exist in the market. The system designer should make sure the specifications of the selected amplifier is adequate for the total system, and that driving capabilities comply with HMCAD1100 input specifications.

Detailed configuration and usage instructions must be found in the documentation of the selected driver, and the values given in figure 13 must be varied according to the recommendations for the driver.

AC-Coupling

A signal transformer or series capacitors can be used to make an AC-coupled input network. Figure 14 shows a recommended configuration using a transformer. Make sure that a transformer with sufficient linearity is selected, and that the bandwidth of the transformer is appropriate. The bandwidth should exceed the sampling rate of the ADC with at least a factor of 10. It is also important to minimize phase mismatch between the differential ADC inputs for good HD2 performance. This type of transformer coupled input is the preferred configuration for high frequency signals as most differential amplifiers do not have adequate performance at high frequencies. Magnetic coupling between the transformers and PCB traces may impact channel crosstalk, and must hence be taken into account during PCB layout.

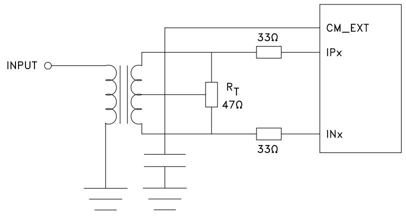

Figure 13. Transformer coupled input

If the input signal is traveling a long physical distance from the signal source to the transformer (for example a long cable), kick-backs from the ADC will also travel along this distance. If these kick-backs are not terminated properly at the source side, they are reflected and will add to the input signal at the ADC input. This could reduce the ADC performance. To avoid this effect, the source must effectively terminate the ADC kick-backs, or the traveling distance should be very short. If this problem could not be avoided, the circuit in figure 16 can be used.

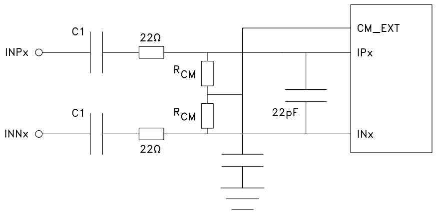

Figure 14. AC coupled input

Figure 15 shows AC-coupling using capacitors. Resistors from the *CM_EXT* output, RCM, should be used to bias the differential input signals to the correct voltage. The series capacitor, CI, form the high-pass pole with these resistors, and the values must therefore be determined based on the requirement to the high-pass cut-off frequency.

Note that Start Up Time from Sleep Mode and Power Down Mode will be affected by this filter as the time required to charge the series capacitors is dependent on the filter cut-off frequency.

If the input signal has a long traveling distance, and the kick-backs from the ADC are not effectively terminated at the signal source, the input network of figure 16 can be used. The configuration in figure 16 is designed to attenuate the kickback from the ADC and to provide an input impedance that looks as resistive as possible for frequencies below Nyquist.

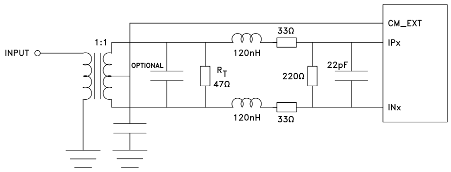

Figure 15. Alternative input network

Values of the series inductor will however depend on board design and conversion rate. In some instances a shunt capacitor in parallel with the termination resistor (e.g. 33pF) may improve ADC performance further. This capacitor attenuate the ADC kick-back even more, and minimize the kicks traveling towards the source. However, the impedance match seen into the transformer becomes worse.

Clock Input and Jitter Considerations

Typically high-speed ADCs use both clock edges to generate internal timing signals. In HMCAD1100 only the rising edge of the clock is used. Hence, input clock duty cycles between 20% and 80% are acceptable.

The input clock can be supplied in a variety of formats. The clock pins are AC-coupled internally, hence a wide common mode voltage range is accepted. Differential clock sources such as LVDS, LVPECL or differential sine wave can be connected directly to the input pins. For CMOS inputs, the CLKN pin should be connected to ground, and the CMOS clock signal should be connected to CLKP. For differential sine wave clock input the amplitude must be at least ± 0.8 Vpp. No additional configuration is needed to set up the clock source format.

The quality of the input clock is extremely important for high-speed, high-resolution ADCs. The contribution to SNR from clock jitter with a full scale signal at a given frequency is shown in equation 1.

$$SNR_{jitter} = 20 \cdot \log(2 \cdot \pi \cdot f_{IN} \cdot \epsilon_t) \qquad (1)$$

where f_{IN} is the signal frequency, and ε_τ is the total rms jitter measured in seconds. The rms jitter is the total of all jitter sources including the clock generation circuitry, clock distribution and internal ADC circuitry.

For applications where jitter may limit the obtainable performance, it is of utmost importance to limit the clock jitter. This can be obtained by using precise and stable clock references (e.g. crystal oscillators with good jitter specifications) and make sure the clock distribution is well controlled. It might be advantageous to use analog power and ground planes to ensure low noise on the supplies to all circuitry in the clock distribution. It is of utmost importance to avoid crosstalk between the ADC output bits and the clock and between the analog input signal and the clock since such crosstalk often results in harmonic distortion.

The jitter performance is improved with reduced rise and fall times of the input clock. Hence, optimum jitter performance is obtained with LVDS or LVPECL clock with fast edges. CMOS and sine wave clock inputs will result in slightly degraded jitter performance.

If the clock is generated by other circuitry, it should be re-timed with a low jitter master clock as the last operation before it is applied to the ADC clock input.

Outline Drawing

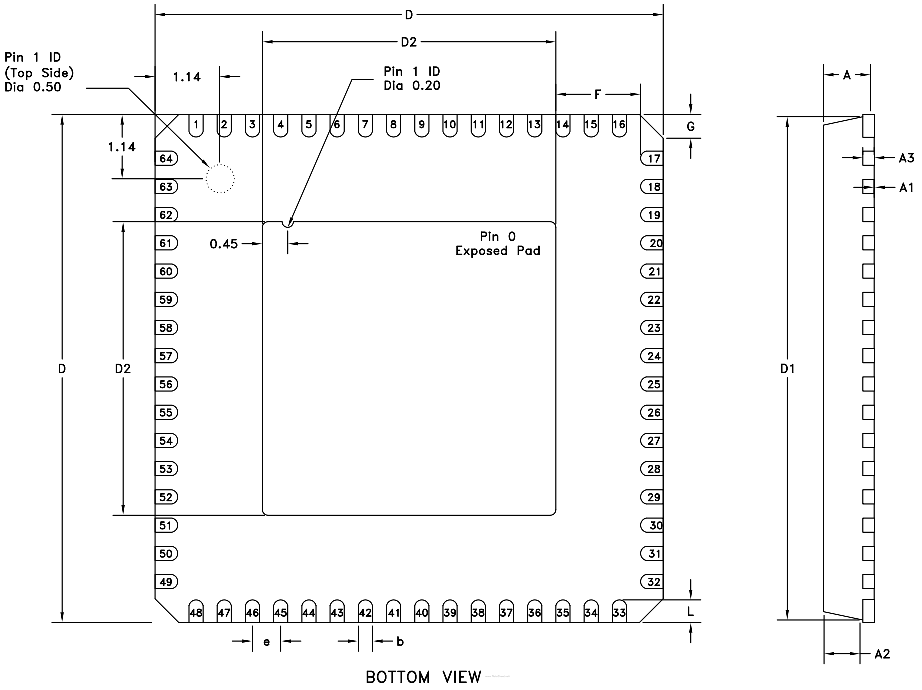

Table 13: Dimensions

Symbol	Millimeter			Inch		
	Min	Typ	Max	Min	Typ	Max
A			0.9			0.035
A1	0	0.01	0.05	0	0.0004	0.002
A2		0.65	0.7		0.026	0.028
A3	0.2 REF.			0.008 REF.		
b	0.2	0.25	0.3	0.008	0.01	0.012
D	9.00 bsc			0.354 bsc		
D1	8.75 bsc			0.344 bsc		
D2	5	5.2	5.4	0.197	0.205	0.213
L	0.3	0.4	0.5	0.012	0.016	0.02
e	0.50 bsc			0.020 bsc		
Θ1	0°		12°	0°		12°
F	1.3			0.05		
G	0.24	0.42	0.6	0.0096	0.0168	0.024

Package Information

Part Number	**Package Body Material**	**Lead Finish**	**MSL [1]**	**Package Marking [2]**
HMCAD1100	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	Level 2A	HAD1100 XXXX

[1] MSL, Peak Temp: The moisture sensitivity level rating classified according to the JEDEC industry standard and to peak solder temperature.

[2] Proprietary marking XXXX, 4-Digit lot number XXXX