



**64Mbyte(16Mx32) 72-pin FP Mode 4K Ref. SIMM Design 5V**  
**Part No. HMD16M32M8G**

**GENERAL DESCRIPTION**

The HMD16M32M8G is a 16Mbit x 32 dynamic RAM high-density memory module. The module consists of eight CMOS 16M x 4bit DRAMs in 32-pin TSOPII packages mounted on a 72-pin, double-sided, FR-4-printed circuit board. A 0.1uF decoupling capacitor is mounted on the printed circuit board for each DRAM components. The module is a Single In-line Memory Module with edge connections and is intended for mounting in to 72-pin edge connector sockets. All module components may be powered from a single 5V DC power supply and all inputs and outputs are TTL-compatible.

**FEATURES**

- w HMD16M32M8G:
- 4K Cycles/64ms Refresh Gold
- w Access times : 50, 60ns
- w High-density 64MByte design
- w Single + 5V ±0.5V power supply
- w JEDEC standard pinout
- w FP(Fast Page) mode operation
- w TTL compatible inputs and outputs
- w FR4-PCB design

**OPTIONS**

- w Timing
  - 50ns access -5
  - 60ns access -6
- w Packages
  - 72-pin SIMM M

**MARKING**

**PIN ASSIGNMENT**

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	19	A10	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	Vss	57	DQ12
4	DQ1	22	DQ5	40	/CAS0	58	DQ28
5	DQ17	23	DQ21	41	/CAS2	59	Vcc
6	DQ2	24	DQ6	42	/CAS3	60	DQ29
7	DQ18	25	DQ22	43	/CAS1	61	DQ13
8	DQ3	26	DQ7	44	/RAS0	62	DQ30
9	DQ19	27	DQ23	45	NC	63	DQ14
10	Vcc	28	A7	46	NC	64	DQ31
11	NC	29	A11	47	/W	65	DQ15
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	NC	51	DQ9	69	PD3
16	A4	34	/RAS2	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	Vss

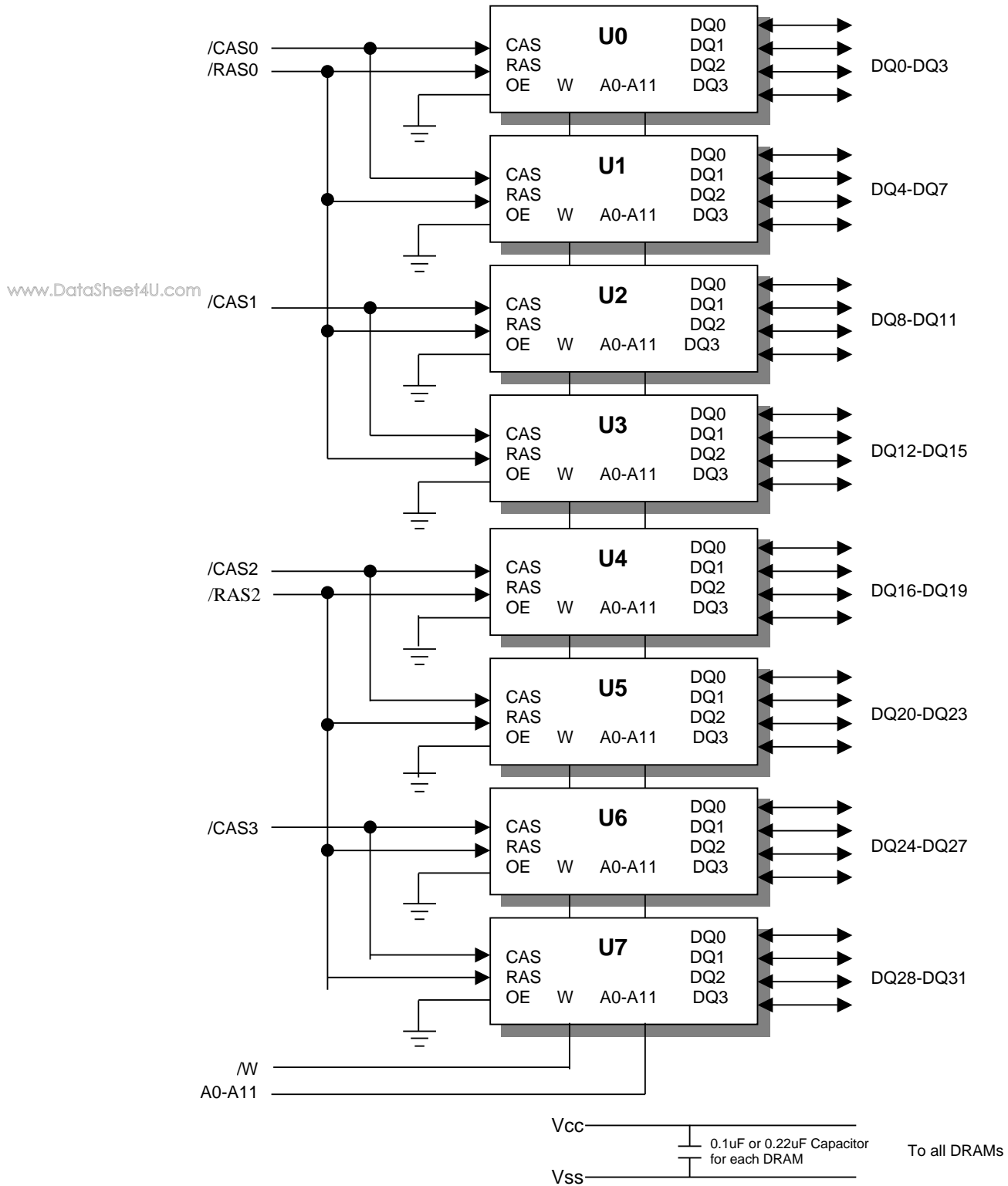
**PERFORMANCE RANGE**

SPEED	tRAC	tCAC	tRC
-5	50ns	13ns	90ns
-6	60ns	15ns	110ns

**wPART IDENTIFICATION**

PRESENCE DETECT PINS	50ns	60ns
PD1	Vss	Vss
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

FUNCTIONAL BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>IN,OUT</sub>	-1V to 7.0V
Voltage on V <sub>CC</sub> Supply Relative to V <sub>SS</sub>	V <sub>CC</sub>	-1V to 7.0V
Power Dissipation	P <sub>D</sub>	6W
Storage Temperature	T <sub>STG</sub>	-55°C to 150°C
Short Circuit Output Current	I <sub>OS</sub>	50mA

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(Voltage reference to V<sub>SS</sub>, T<sub>A</sub>=0 to 70 °C)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.4	-	V <sub>CC</sub> +1	V
Input Low Voltage	V <sub>IL</sub>	-1.0	-	0.8	V

**DC AND OPERATING CHARACTERISTICS**

SYMBOL	SPEED	MIN	MAX	UNITS
I <sub>CC1</sub>	-5	-	880	MA
	-6	-	800	MA
I <sub>CC2</sub>		-	16	MA
I <sub>CC3</sub>	-5	-	880	MA
	-6	-	800	MA
I <sub>CC4</sub>	-5	-	720	MA
	-6	-	560	MA
I <sub>CC5</sub>		-	8	MA
I <sub>CC6</sub>	-5	-	880	MA
	-6	-	800	MA
I <sub>I(L)</sub>		-60	5	μA
I <sub>O(L)</sub>		-5	5	μA
V <sub>OH</sub>		2.4	-	V
V <sub>OL</sub>		-	0.4	V

$I_{CC1}$  : Operating Current \* (/RAS , /CAS , Address cycling @ $t_{RC}=\text{min.}$ )

$I_{CC2}$  : Standby Current ( /RAS=/CAS= $V_{IH}$ )

$I_{CC3}$  : /RAS Only Refresh Current \* ( /CAS= $V_{IH}$ , /RAS, Address cycling @ $t_{RC}=\text{min.}$ )

$I_{CC4}$  : Fast Page Mode Current \* (/RAS= $V_{IL}$ , /CAS, Address cycling @ $t_{PC}=\text{min.}$ )

$I_{CC5}$  : Standby Current (/RAS=/CAS= $V_{CC}-0.2V$ )

$I_{CC6}$  : /CAS-Before-/RAS Refresh Current \* (/RAS and /CAS cycling @ $t_{RC}=\text{min.}$ )

$I_{IL}$  : Input Leakage Current (Any input  $0V \leq V_{IN} \leq 6.5V$ , all other pins not under test =  $0V$ )

$I_{OL}$  : Output Leakage Current (Data out is disabled,  $0V \leq V_{OUT} \leq 5.5V$ )

$V_{OH}$  : Output High Voltage Level ( $I_{OH} = -5mA$ )

$V_{OL}$  : Output Low Voltage Level ( $I_{OL} = 4.2mA$ )

\* NOTE:  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  are dependent on output loading and cycle rates. Specified values are obtained with the output open.  $I_{CC}$  is specified as an average current. In  $I_{CC1}$  and  $I_{CC3}$ , address can be changed maximum once while /RAS= $V_{IL}$ . In  $I_{CC4}$ , address can be changed maximum once within one page mode cycle.

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## CAPACITANCE ( $T_A=25^\circ C$ , $V_{CC} = 5V$ , $f = 1Mz$ )

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Input Capacitance (A0-A11)	$C_{IN1}$	-	40	pF
Input Capacitance (/W)	$C_{IN2}$	-	56	pF
Input Capacitance (/RAS0)	$C_{IN3}$	-	58	pF
Input Capacitance (/CAS0-/CAS3)	$C_{IN4}$	-	54	pF
Input/Output Capacitance (DQ0-31)	$C_{DQ1}$	-	57	pF

## AC CHARACTERISTICS ( $0^\circ C \leq T_A \leq 70^\circ C$ , $V_{CC} = 5V \pm 10\%$ , See notes 1,2.)

PARAMETER	SYMBOL	-5		-6		UNIT
		MIN	MAX	MIN	MAX	
Random read or write cycle time	$t_{RC}$	90		110		ns
Access time from /RAS	$t_{RAC}$		50		60	ns
Access time from /CAS	$t_{CAC}$		13		15	ns
Access time from column address	$t_{AA}$		25		30	ns
/CAS to output in Low-Z	$t_{CLZ}$	0		0		ns
Output buffer turn-off delay	$t_{OFF}$	0	13	0	15	ns
Transition time (rise and fall)	$t_T$	3	50	3	50	ns
/RAS precharge time	$t_{RP}$	30		40		ns
/RAS pulse width	$t_{RAS}$	50	10K	60	10K	ns
/RAS hold time	$t_{RSH}$	13		15		ns
/CAS hold time	$t_{CSH}$	50		60		ns
/CAS pulse width	$t_{CAS}$	13	10K	15	10K	ns
/RAS to /CAS delay time	$t_{RCD}$	20	37	20	45	ns
/RAS to column address delay time	$t_{RAD}$	15	25	15	30	ns

/CAS to /RAS precharge time	$t_{CRP}$	5		5		ns
Row address set-up time	$t_{ASR}$	0		0		ns
Row address hold time	$t_{RAH}$	10		10		ns
Column address set-up time	$t_{ASC}$	0		0		ns
Column address hold time	$t_{CAH}$	10		10		ns
Column address hold referenced to /RAS	$t_{AR}$	50		55		ns
Column Address to /RAS lead time	$t_{RAL}$	25		30		ns
Read command set-up time	$t_{RCS}$	0		0		ns
Read command hold referenced to /CAS	$t_{RCH}$	0		0		ns
Read command hold referenced to /RAS	$t_{RRH}$	0		0		ns
Write command hold time	$t_{WCH}$	10		10		ns
Write command hold referenced to /RAS	$t_{WCR}$	50		55		ns
Write command pulse width	$t_{WP}$	10		10		ns
Write command to /RAS lead time	$t_{RWL}$	13		15		ns
Write command to /CAS lead time	$t_{CWL}$	13		15		ns
Data-in set-up time	$t_{DS}$	0		0		ns
Data-in hold time	$t_{DH}$	10		10		ns
Data-in hold referenced to /RAS	$t_{DHR}$	50		55		ns
Refresh period	$t_{REF}$		16		16	ns
Write command set-up time	$t_{WCS}$	0		0		ns
/CAS setup time (C-B-R refresh)	$t_{CSR}$	10		10		ns
/CAS hold time (C-B-R refresh)	$t_{CHR}$	15		15		ns
/RAS precharge to /CAS hold time	$t_{RPC}$	5		5		ns
Access time from /CAS precharge	$t_{CPA}$		35		40	ns
Fast page mode cycle time	$t_{PC}$	40		45		ns
/CAS precharge time (Fast page)	$t_{CP}$	10		10		ns
/RAS pulse width (Fast page )	$t_{RASP}$	60	100K	70	100K	ns
/W to /RAS precharge time (C-B-R refresh)	$t_{WRP}$	10		10		ns
/W to /RAS hold time (C-B-R refresh)	$t_{WRH}$	10		10		ns
/CAS precharge(C-B-R counter test)	$t_{CPT}$	20		30		ns

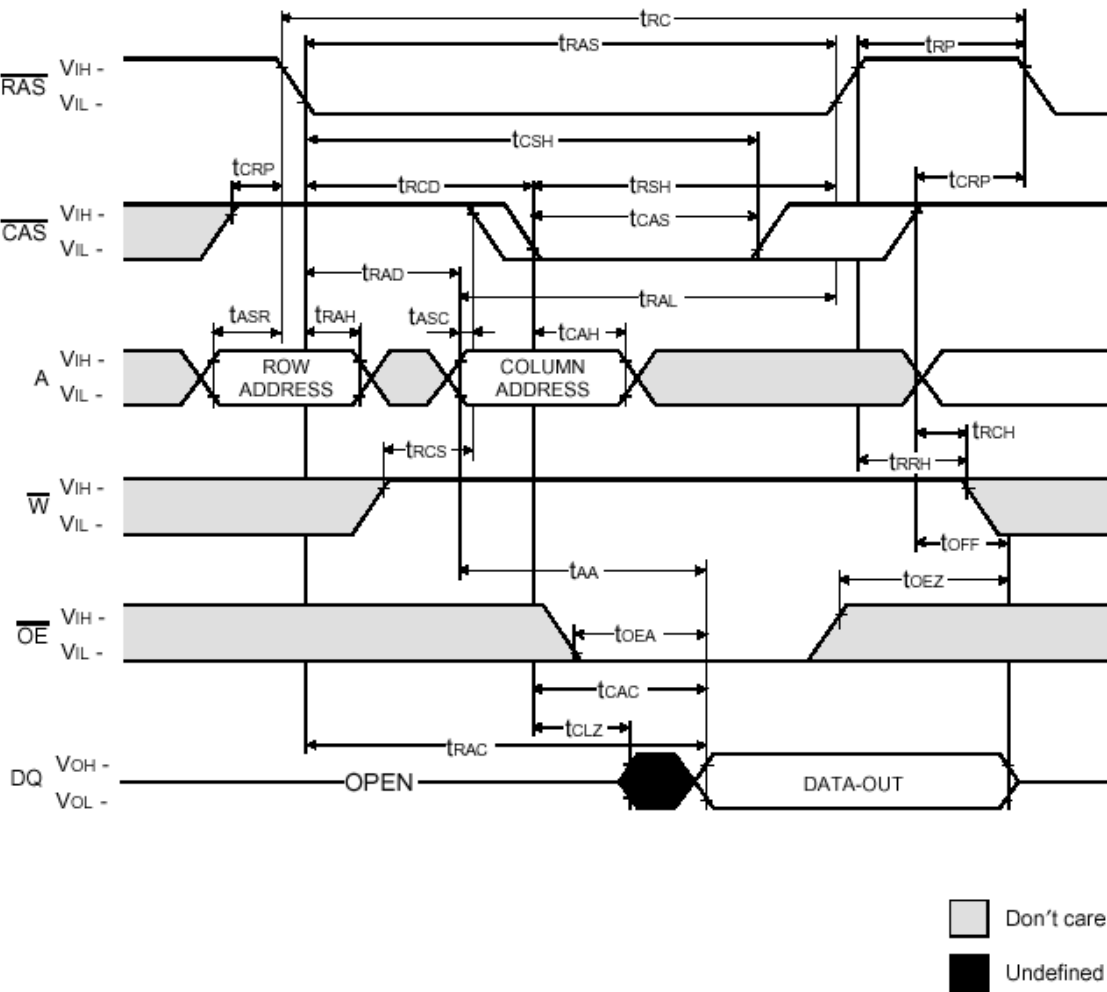
**NOTES**

1. An initial pause of 200 $\mu$ s is required after power-up followed by any 8 /RAS-only or /CAS-before-/RAS refresh cycles before proper device operation is achieved.
2.  $V_{IH(min)}$  and  $V_{IL(max)}$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH(min)}$  and  $V_{IL(max)}$  and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1TTL loads and 100pF
4. Operation within the  $t_{RCD(max)}$  limit insures that  $t_{RAC(max)}$  can be met.  $t_{RCD(max)}$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD(max)}$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
5. Assumes that  $t_{RCD} \geq t_{RCD(max)}$

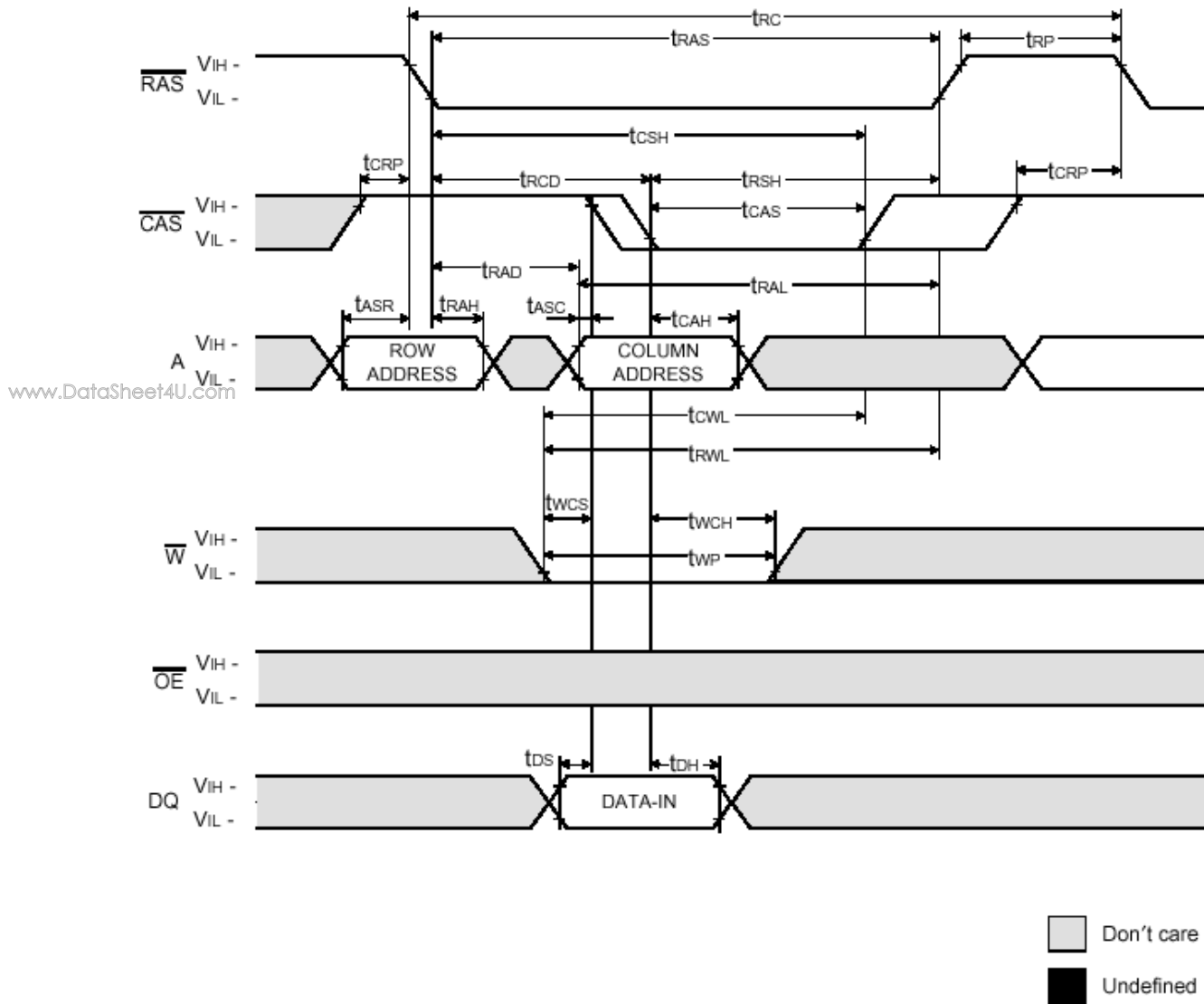
6.  $t_{AR}$ ,  $t_{WCR}$ ,  $t_{DHR}$  are referenced to  $t_{RAD(max)}$
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
8.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are non restrictive operating parameter. They are included in the data sheet as electrical characteristic only. If  $t_{WCS} \geq t_{WCS(min)}$  the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
10. These parameters are referenced to the /CAS leading edge in early write cycles and to the /W leading edge in read-write cycles.
11. Operation within the  $t_{RAD(max)}$  limit insures that  $t_{RAC(max)}$  can be met.  $t_{RAD(max)}$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD(max)}$  limit, then access time is controlled by  $t_{AA}$ .

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**Timing Diagrams**

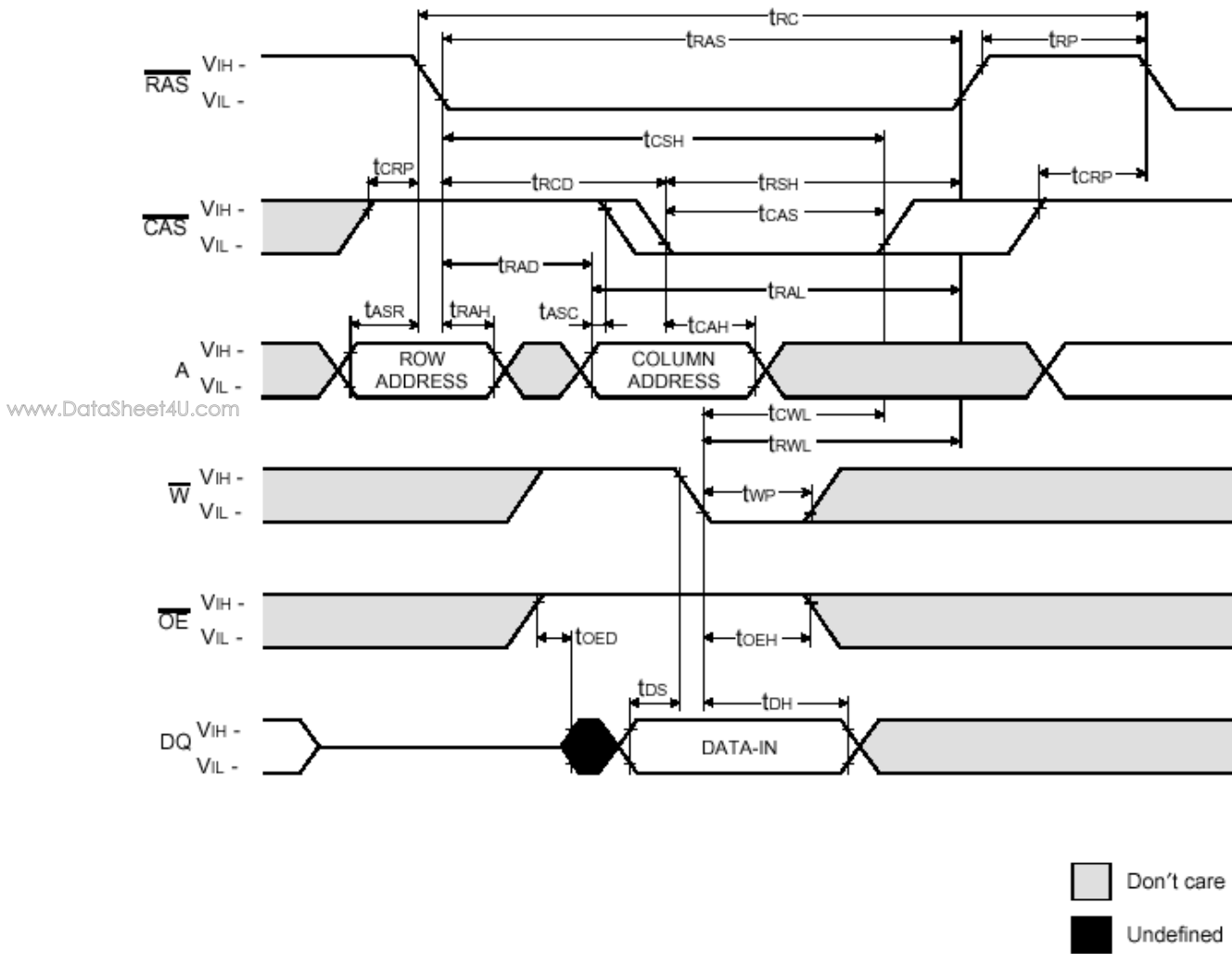
**TIMING WAVEFORM OF READ CYCLE**



TIMING WAVEFORM OF WRITE CYCLE (EARLY WRITE)

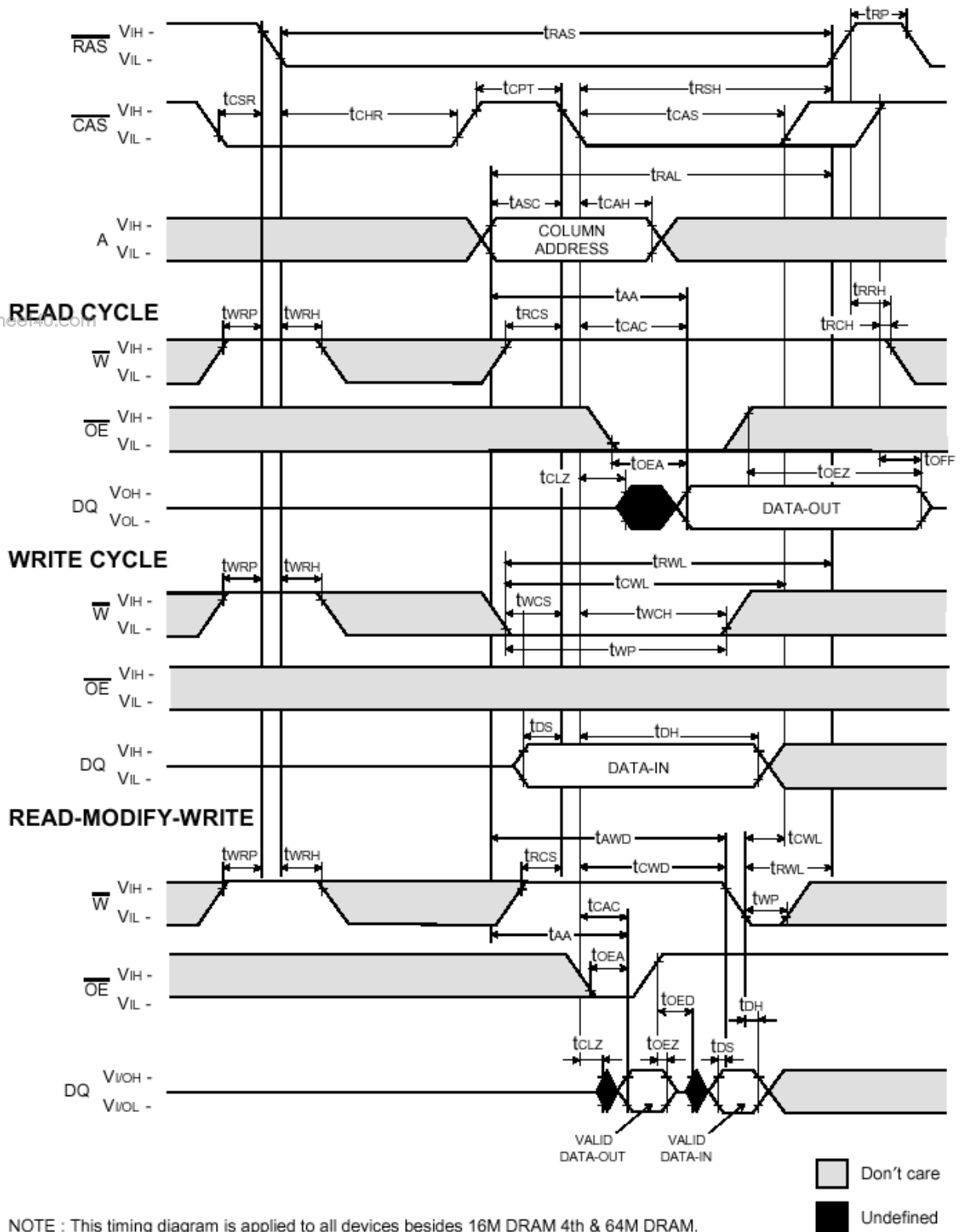


WRITE CYCLE (/OE CONTROLLED WRITE) Note: Dout=open





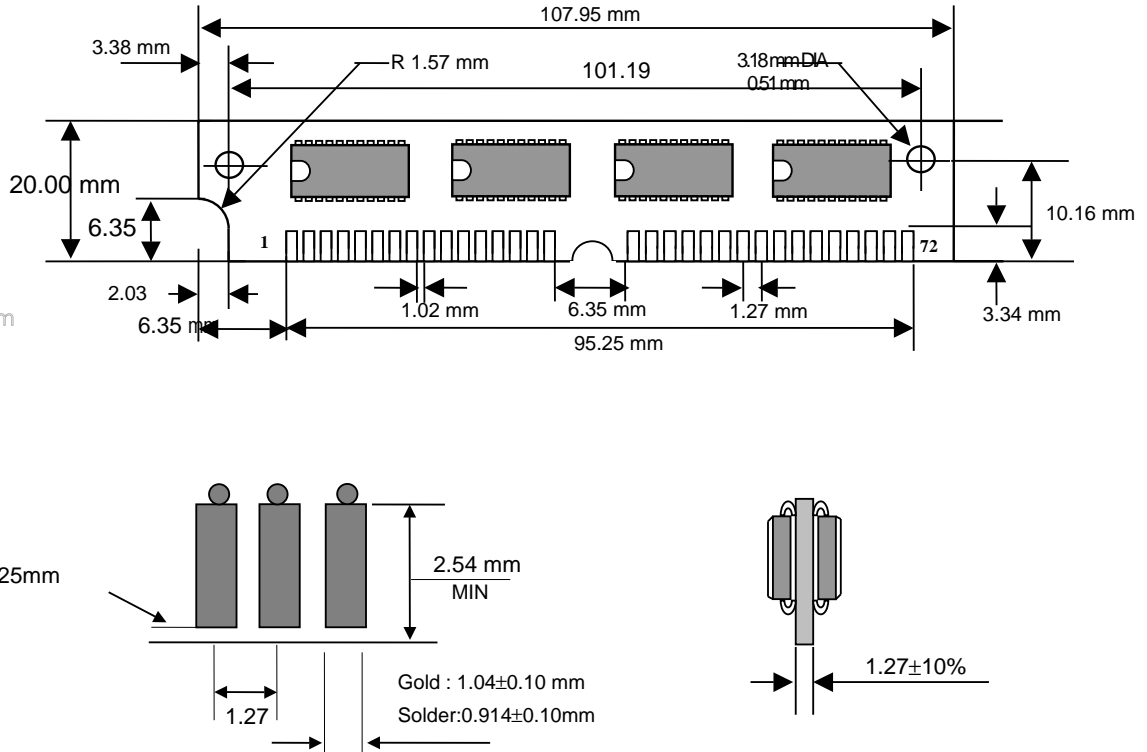
/CAS-BEFORE-/RAS REFRESH CYCLE TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 16M DRAM 4th & 64M DRAM.

PACKAGING INFORMATION

SIMM Design



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ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	MODE	SPEED
HMD16M32M8G-5	64Byte	x 32	72 Pin-SIMM	8EA	5V	FPM	50ns
HMD16M32M8G-6	64Byte	x 32	72 Pin-SIMM	8EA	5V	FPM	60ns