



**4Mbyte(1Mx32) Fast Page Mode, 1K Refresh, 72Pin SIMM, 5V
Design Part No. HMD1M32M2GL**

DESCRIPTION

The HMD1M32M2GL is an 1M x 32 bits Dynamic RAM MODULE which is assembled 2 pieces of 1M x 16bit DRAMs in 42 pin SOJ package on single sides the printed circuit board with decoupling capacitors. The HMD1M32M2GL is optimized for application to the systems, which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others, which are, requested compact size.

The HMD1M32M2GL provides common data and outputs.

Features

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w 72 pins Single In-Line Package

w Fast Page Mode Capability

w Single +5V± 0.5V power supply

w Fast Access Time & Cycle Time

| | tRAC | tCAC | tRC | tPC |
|--------------|------|------|-----|-----|
| HMD1M32M2G-5 | 50 | 15 | 90 | 35 |
| HMD1M32M2G-6 | 60 | 15 | 110 | 40 |

w Low Power

w /RAS Only Refresh, /CAS before /RAS Refresh,

Hidden Refresh Capability

w All inputs and outputs TTL Compatible

w 1,024 Refresh Cycles/16ms

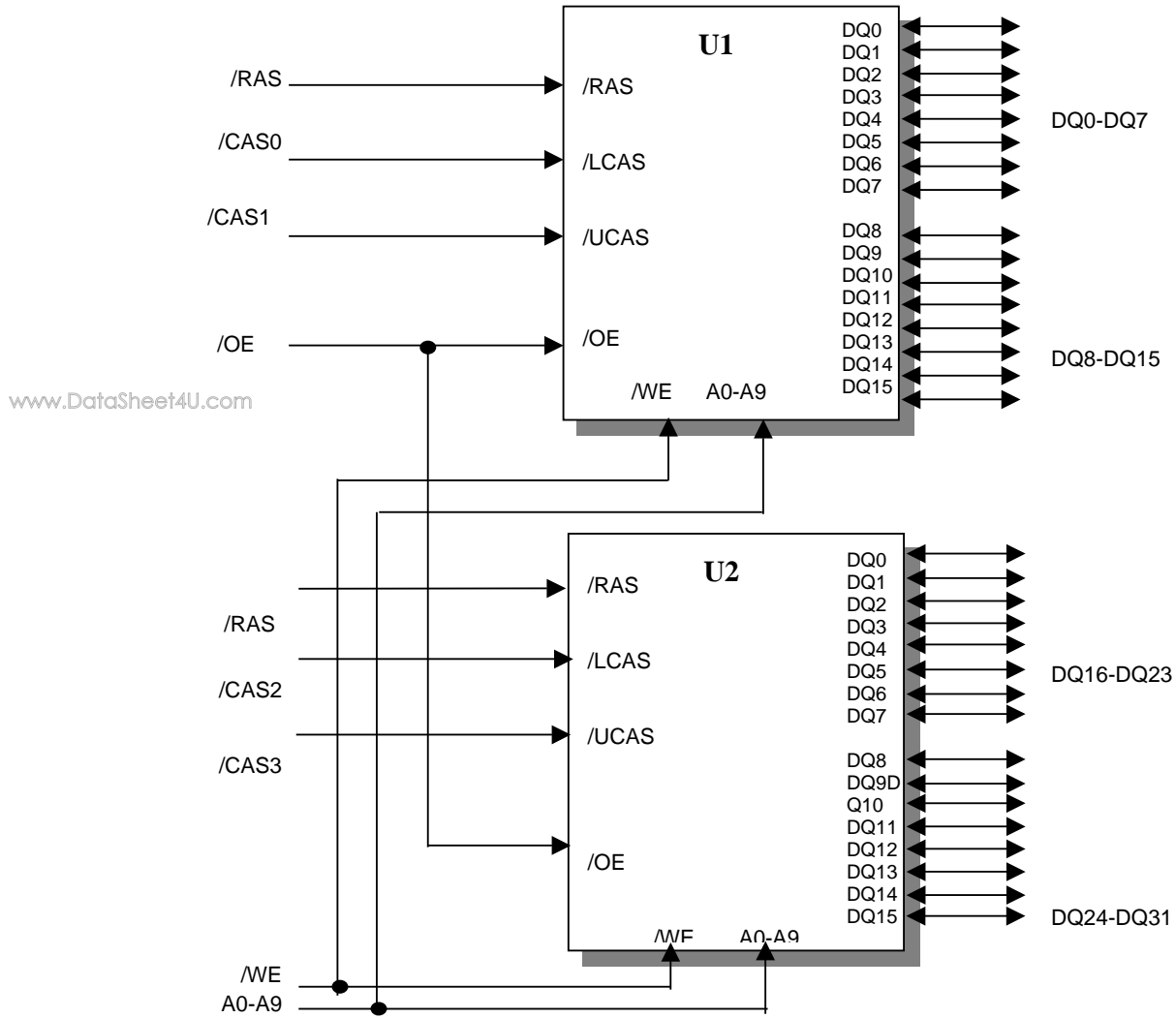
PIN DESCRIPTION

| PIN | FUNCTION | PIN | FUNCTION |
|------------|-----------------------|-----|-------------------|
| A0 – A9 | Address Inputs | /WE | Read/Write Enable |
| DQ0 – DQ31 | Data Input/Output | Vcc | Power (+5V) |
| /RAS | Row Address Strobe | Vss | Ground |
| /CAS | Column Address Strobe | NC | No Connection |
| /OE | Data Output Enable | | |

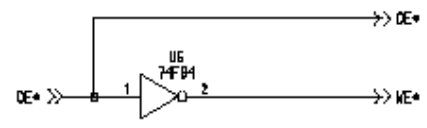
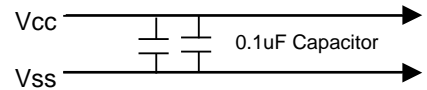
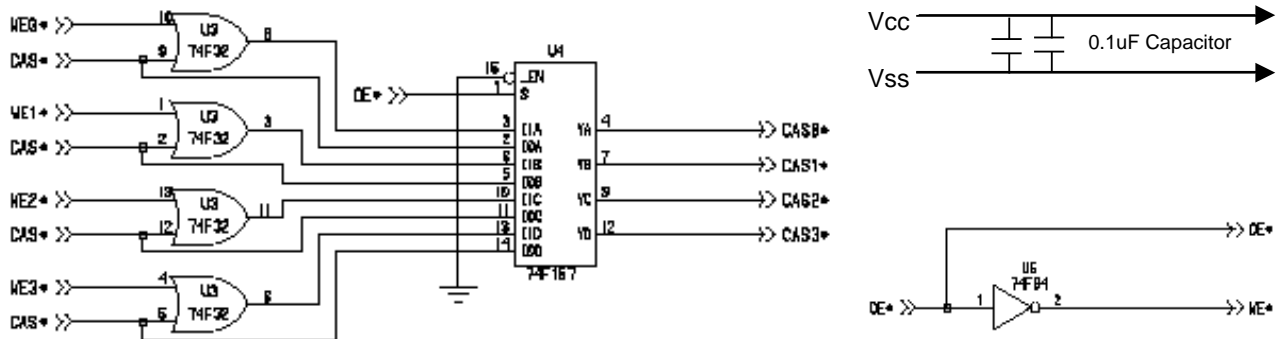
PIN ASSIGNMENT

| PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL |
|-----|--------|-----|---------|-----|--------|
| 1 | Vss | 25 | DQ22 | 49 | DQ8 |
| 2 | DQ0 | 26 | DQ7 | 50 | DQ24 |
| 3 | DQ16 | 27 | DQ23 | 51 | DQ9 |
| 4 | DQ1 | 28 | A8 | 52 | DQ25 |
| 5 | DQ17 | 29 | NC(A10) | 53 | DQ10 |
| 6 | DQ2 | 30 | Vcc | 54 | DQ26 |
| 7 | DQ18 | 31 | /WE2 | 55 | DQ11 |
| 8 | DQ3 | 32 | NC | 56 | DQ27 |
| 9 | DQ19 | 33 | Vcc | 57 | DQ12 |
| 10 | Vcc | 34 | /RAS | 58 | DQ28 |
| 11 | /WEO | 35 | Vcc | 59 | /WE3 |
| 12 | A0 | 36 | NC | 60 | DQ29 |
| 13 | A1 | 37 | NC | 61 | DQ13 |
| 14 | A2 | 38 | /OE | 62 | DQ30 |
| 15 | A3 | 39 | Vss | 63 | DQ14 |
| 16 | A4 | 40 | /CAS | 64 | DQ31 |
| 17 | A5 | 41 | Vcc | 65 | DQ15 |
| 18 | A6 | 42 | NC | 66 | Vcc |
| 19 | A7 | 43 | NC | 67 | NC |
| 20 | DQ4 | 44 | NC | 68 | NC |
| 21 | DQ20 | 45 | A9 | 69 | Vss |
| 22 | DQ5 | 46 | NC(A11) | 70 | NC |
| 23 | DQ21 | 47 | /WE1 | 71 | Vss |
| 24 | DQ6 | 48 | Vcc | 72 | Vss |

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

| SYMBOL | PARAMETER | RATING | UNIT |
|----------|------------------------------------|------------|------|
| TA | Ambient Temperature under Bias | 0 ~ 70 | C |
| TSTG | Storage Temperature (Plastic) | -55 ~ 150 | C |
| VIN/VOUT | Voltage on any Pin Relative to Vss | -1.0 ~ 7.0 | V |
| VCC | Power Supply Voltage | -1.0 ~ 7.0 | V |
| IOUT | Short Circuit Output Current | 100 | mA |
| PD | Power Dissipation | 2 | W |

*NOTE: 1. Stress greater than above absolute Maximum Ratings? May cause permanent damage to the device.

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RECOMMENDED DC OPERATING CONDITIONS ($T_A = 0 \sim 70C$)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNIT |
|--------------------|-----------------|------|------|-------|------|
| Supply Voltage | Vcc | 4.5 | 5.0 | 5.5 | V |
| Ground | Vss | 0 | 0 | 0 | V |
| Input High Voltage | V _{IH} | 2.4 | - | Vcc+1 | V |
| Input Low Voltage | V _{IL} | -1.0 | - | 0.8 | V |

*NOTE: All voltages referenced to Vcc

DC AND OPERATING CHARACTERISTICS

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|-------------------|---|-----|-----|------|
| VOH | Output High Level Voltage (IOUT = -5mA) | 2.4 | | V |
| VOL | Output Low Level Voltage (IOUT = 4.2mA) | 0 | 0.4 | V |
| ICC1 | Operating Current (/RAS,/CAS,Address Cycling : tRC = tRC min) | -5 | 280 | mA |
| | | -6 | 260 | |
| ICC2 | Standby Current (/RAS,/CAS = V _{IH}) | - | 4 | mA |
| ICC3 | /RAS Only Refresh Current (/RAS Cycling, /CAS = V _{IH} ; tRC = tRC min) | -5 | 280 | mA |
| | | -6 | 260 | |
| ICC4 | Fast Page Mode Current (/RAS = V _{IL} , /CAS, Address Cycling : tPC = tPC min) | -5 | 180 | mA |
| | | -6 | 160 | |
| ICC5 | Standby Current (/RAS,/CAS >= Vcc - 0.2V) | | 2 | mA |
| ICC6 | /CAS before /RAS Refresh Current (tRC = tRC min) | -5 | 280 | mA |
| | | -6 | 260 | |
| ICCS | Self Refresh Current (/RAS=/UCAS=/LCAS=V _{IL} , /WE=/OE=A0~A9= Vcc - 0.2V or 0.2V, DQ0~DQ31= Vcc - 0.2V, 0.2V or Open) | - | 400 | uA |
| I _{I(L)} | Input Leakage Current (Any Input (0V <= V _{IN} <= V _{IN} + 0.5V, All Other Pins Not Under Test = 0V) | -10 | 10 | uA |
| I _{O(L)} | Output Leakage Current(DOOUT is Disabled, 0V <= V _{OUT} <= Vcc) | -10 | 10 | uA |

Note: 1. I_{CC} depends on output load condition when the device is selected.

I_{CC} (max) is specified at the output open condition.

2. Address can be changed once or less while /RAS = V_{IL}.

3. Address can be changed once or less while /CAS = V_{IH}.

CAPACITANCE (T_A=25°C, V_{CC} = 5V±10%, f = 1Mhz)

| DESCRIPTION | SYMBOL | MIN | MAX | UNITS | NOTE |
|---|------------------|-----|-----|-------|------|
| Input Capacitance (A0-A9) | C _{I1} | - | 5 | pF | 1 |
| Input Capacitance (/WE,/RAS, /CAS0- /CAS3,/OE) | C _{I2} | - | 7 | pF | 1,2 |
| Input/Output Capacitance (DQ0-31) | C _{DQ1} | - | 7 | pF | 1,2 |

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. /CAS = V_{IH} to disable DOUT.

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC} = 5V±10%, V_{IH}/V_{IL} = 2.4/0.8V, V_{OH}/V_{OL} = 2.4/0.4V, See notes 1,2)

| SYMBOL | PARAMETER | -5 | | -6 | | UNIT | NOTE |
|------------------|-----------------------------------|-----|-----|-----|-----|------|--------|
| | | MIN | MAX | MIN | MAX | | |
| t _{RC} | Random Read or Write Cycle Time | 90 | | 110 | | ns | |
| t _{RWC} | Read-modify-writer cycle time | 133 | | 155 | | ns | |
| t _{RAC} | Access Time from /RAS | | 50 | | 60 | ns | 3,4,10 |
| t _{CAC} | Access Time from /CAS | | 15 | | 15 | ns | 3,4,5 |
| T _{aa} | Access Time from Column Address | | 25 | | 30 | ns | 3,10 |
| t _{OFF} | Output Buffer Turn-off Time | 0 | 13 | 0 | 15 | ns | 6 |
| t _T | Transition Time (Rise and Fall) | 3 | 50 | 3 | 50 | ns | 2 |
| TRP | /RAS Precharge Time | 30 | | 40 | | ns | |
| t _{RAS} | /RAS Pulse Width | 50 | 10K | 60 | 10K | ns | |
| t _{RSH} | /RAS Hold Time | 13 | | 15 | | ns | |
| t _{CSH} | /CAS Hold Time | 50 | | 60 | | ns | |
| t _{CAS} | /CAS Pulse Width | 13 | 10K | 15 | 10K | ns | |
| t _{RCD} | /RAS to /CAS Delay Time | 20 | 37 | 20 | 45 | ns | 4 |
| t _{RAD} | /RAS to Column Address Delay Time | 15 | 25 | 15 | 30 | ns | 10 |
| t _{CRP} | /CAS to /RAS Precharge Time | 5 | | 5 | | ns | |
| t _{ASR} | Row Address Setup Time | 0 | | 0 | | ns | |
| t _{RAH} | Row Address Hold Time | 10 | | 10 | | ns | |
| t _{ASC} | Column Address Setup Time | 0 | | 0 | | ns | 11 |
| t _{CAH} | Column Address Hold Time | 10 | | 10 | | ns | 11 |
| t _{RAL} | Column Address to /RAS Lead Time | 25 | | 30 | | ns | |
| t _{RCS} | Read Command Setup Time | 0 | | 0 | | ns | |
| t _{RCH} | Read Command Hold Time to /CAS | 0 | | 0 | | ns | 8 |

| | | | | | | | |
|------------------------|---|-----|------|-----|------|----|------|
| tRRH | Read Command Hold Time to /RAS | 0 | | 0 | | ns | 8 |
| tWCH | Write Command Hold Time | 10 | | 10 | | ns | |
| tWP | Write Command Pulse Width | 10 | | 10 | | ns | |
| tRWL | Write Command to /RAS Lead Time | 13 | | 15 | | ns | |
| tCWL | Write Command to /CAS Lead Time | 13 | | 15 | | ns | |
| tDS | Data-in Setup Time | 0 | | 0 | | ns | 9 |
| tDH | Data-in Hold Time | 10 | | 10 | | ns | 9 |
| t_{REF} | Refresh Period (1024 Cycle) | | 16 | | 16 | ms | |
| twcs | Write Command Setup Time | 0 | | 0 | | ms | 7 |
| tCWD | /CAS to /WE delay time | 36 | | 40 | | ms | 7,13 |
| tRWD | /RAS to /WE delay time | 73 | | 85 | | ns | 7 |
| tAWD | Column Address to /WE delay time | 48 | | 55 | | ns | 7 |
| tCPWD | /CAS precharge to /WE delay time | 53 | | 60 | | ns | 7 |
| tCSR | /CAS Setup Time (/CAS-before-/RAS Refresh Cycle) | 5 | | 5 | | ns | 15 |
| tCHR | /CAS Hold Time (/CAS-before-/RAS Refresh Cycle) | 10 | | 10 | | ns | 16 |
| tRPC | /RAS Precharge to /CAS Hold Time | 5 | | 5 | | ns | |
| tCPA | Access Time from /CAS Precharge | | 30 | | 35 | ns | 3 |
| tPC | Fast Page Mode Cycle Time | 35 | | 40 | | ns | |
| tCP | Fast Page Mode /RAS Precharge Time | 10 | | 10 | | ns | 12 |
| tRASP | Fast Page Mode /CAS Pulse Time | 50 | 200K | 60 | 200K | ns | |
| tRHCP | /RAS Hold Time time from /CAS Precharge | 30 | | 35 | | ns | |
| tOEA | /OE Access Time | | 13 | | 15 | ns | 3 |
| tOED | /OE to data delay | 13 | | 15 | | ns | |
| tOEZ | Output buffer turn off delay time from /OE | 0 | 13 | 0 | 15 | ns | |
| tOEH | /OE command hold time | 13 | | 15 | | ns | |
| tRASS | /RAS Pulse Width(CBR self refresh) | 100 | | 100 | | us | |
| tPRS | /RAS Precharge Time(CBR self refresh) | 90 | | 110 | | ns | |
| tCHS | /CAS Hold Time(CBR self refresh) | -50 | | -50 | | ns | |

- Note:**
1. An initial pause of 200us is required after power-up followed by any 8 /RAS-only refresh or /CAS-before-/RAS refresh cycles before proper device operation is achieved.
 2. Input voltage levels are V_{IH} / V_{IL} . $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} are assumed to be 5ns for all inputs.
 3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
 4. Operation with the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met, $t_{RCD}(\max)$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
 5. Assumes that $t_{RCD} \leq t_{RCD}(\max)$.
 6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} / V_{OL} .
 7. T_{WCS} , T_{RWD} , T_{CWD} , T_{CPWD} are non restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{wcs} \geq t_{wcs}(\min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout

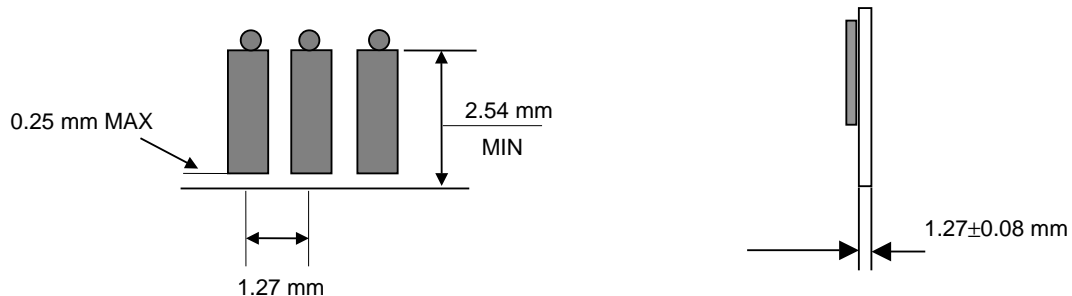
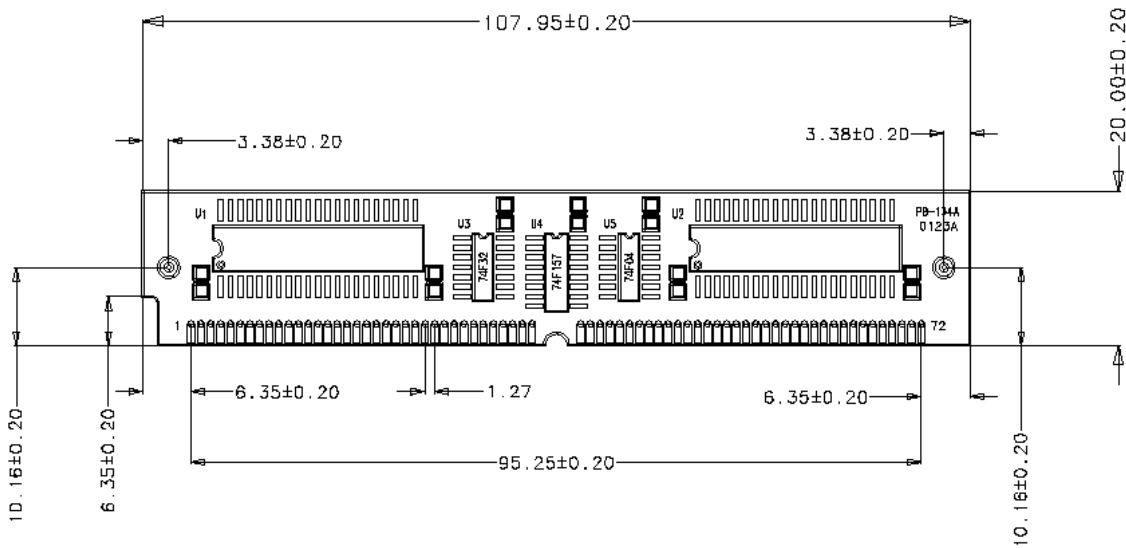
the entire cycle. If $t_{CWD} \geq t_{CWD}(\min)$, $t_{RWD} \geq t_{RWD}(\min)$, $T_{CPWD} \geq T_{CPWD}(\min)$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
9. These parameters are referenced to /CAS falling edge in early write cycles and to /WE falling edge in /OE controlled write cycle and read-modify-write cycles.
10. Operation with the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met, $t_{RAD}(\max)$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled exclusively by t_{AA} .
11. t_{ASC} , t_{CAH} are are referenced to the earlier /CAS falling edge.
12. t_{CP} is specified from the later /CAS rising edge in the previous cycle to the earlier /CAS falling edge in the next cycle.
13. t_{CWD} is referenced to the later /CAS falling edge at word read-modify-write cycle.
14. t_{CWL} is specified from /WE falling edge to the earlier /CAS rising edge .
15. t_{CSR} is referenced to the earlier /CAS falling edge before /RAS transition low.
16. t_{CHR} is referenced to the later /CAS rising edge after /RAS transition low.

PACKAGING INFORMATION

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FRONT-SIDE



ORDERING INFORMATION

| Part Number | Density | Org. | Package | Component Number | Vcc | MODE | SPEED |
|---------------|---------|------|-------------|------------------|-----|------|-------|
| HMD1M32M2GL-5 | 4MByte | X32 | 72 Pin-SIMM | 2EA | 5V | FP | 50ns |
| HMD1M32M2GL-6 | 4MByte | x 32 | 72 Pin-SIMM | 2EA | 5V | FP | 60ns |

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