**FLASH-ROM MODULE 4MByte (1M x 32-Bit), 72pin-SIMM, 5V**
**Part No. HMF1M32M8S (Switching for write enable/disable)**

## GENERAL DESCRIPTION

The HMF1M32M8S is a high-speed flash read only memory (FROM) module containing 1,048,576 words organized in a x32bit configuration. The module consists of eight 512K x 8 FROM mounted on a 72-pin, both-sided, FR4-printed circuit board.In order to write control, the HMF1M32M8S provides Write Enable and Write Disable selection by SMT switch. Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices. Eight chip enable inputs, (/CE-UU1, /CE_UM1, /CE_LM1, /CE_LL1, /CE_UU2, /CE_UM2, /CE_LM2, /CE_LL2) are used to enable the module's 4 bytes independently. Output enable (/OE) and write enable (/WE) can set the memory input and output..

When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single +5V DC power supply and all inputs and outputs are TTL-compatible



## FEATURES

- Access time: 70, 90 and 120ns
- Switching for write enable and disable.
- High-density 4MByte design
- High-reliability, low-power design
- Single + 5V ± 0.5V power supply
- Easy memory expansion
- All inputs and outputs are TTL-compatible
- FR4-PCB design
- Low profile 72-pin SIMM
- Minimum 100,000 write/erase cycle
- Sector erases architecture
- Sector group protection
- Temporary sector group unprotection

## OPTIONS MARKING

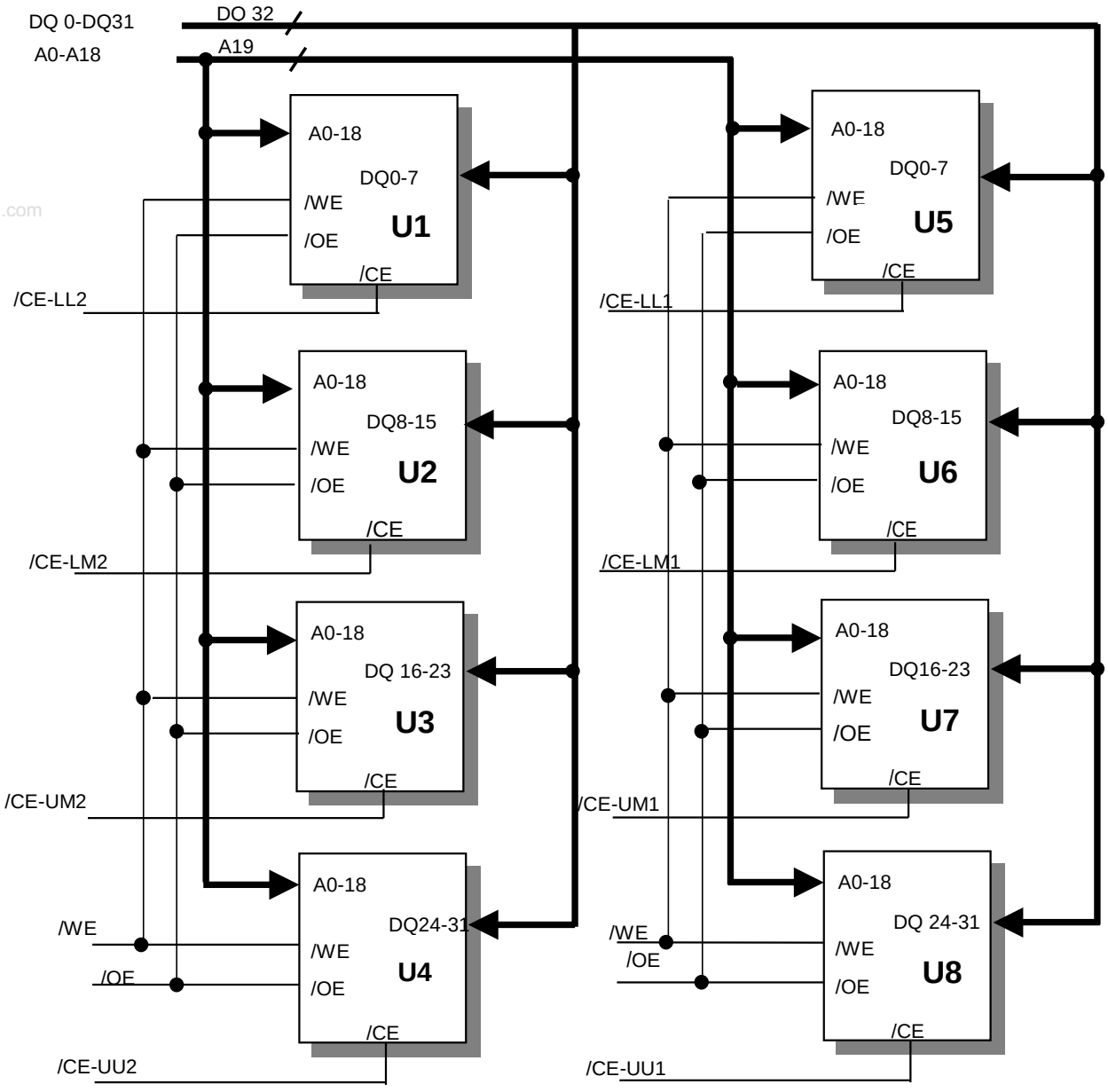
- Timing
  - 70ns access -70
  - 90ns access -90
  - 120ns access -120
- Packages
  - 72-pin SIMM M

## PIN ASSIGNMENT

| PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL |
|---|---|---|---|---|---|---|---|
| 1 | VSS | 19 | DQ4 | 37 | A18 | 55 | VCC |
| 2 | A3 | 20 | DQ3 | 38 | A16 | 56 | A15 |
| 3 | A2 | 21 | /WE | 39 | VSS | 57 | A12 |
| 4 | A1 | 22 | A17 | 40 | A6 | 58 | A7 |
| 5 | A0 | 23 | A14 | 41 | VCC | 59 | VCC |
| 6 | VCC | 24 | A13 | 42 | A5 | 60 | A8 |
| 7 | A11 | 25 | VCC | 43 | A4 | 61 | A9 |
| 8 | /OE | 26 | DQ8 | 44 | VCC | 62 | DQ24 |
| 9 | A10 | 27 | DQ9 | 45 | /CE-UM2 | 63 | DQ25 |
| 10 | VCC | 28 | DQ10 | 46 | /CE-UM1 | 64 | DQ26 |
| 11 | /CE-LL2 | 29 | /CE-LM2 | 47 | DQ23 | 65 | /CE-UU2 |
| 12 | /CE-LL1 | 30 | VCC | 48 | DQ16 | 66 | /CE-UU1 |
| 13 | DQ7 | 31 | /CE-LM1 | 49 | DQ17 | 67 | DQ31 |
| 14 | DQ0 | 32 | DQ15 | 50 | DQ18 | 68 | DQ30 |
| 15 | DQ1 | 33 | DQ14 | 51 | DQ22 | 69 | DQ29 |
| 16 | DQ2 | 34 | DQ13 | 52 | DQ21 | 70 | DQ28 |
| 17 | DQ6 | 35 | DQ12 | 53 | DQ20 | 71 | DQ27 |
| 18 | DQ5 | 36 | DQ11 | 54 | DQ19 | 72 | VSS |

**SIMM TOP VIEW**

## FUNCTIONAL BLOCK DIAGRAM



## TRUTH TABLE

| MODE | /OE | /CE | /WE | DQ | POWER |
|---|---|---|---|---|---|
| STANDBY | X | H | X | HIGH-Z | STANDBY |
| NOT SELECTED | H | L | H | HIGH-Z | ACTIVE |
| READ | L | L | H | Q | ACTIVE |
| WRITE | H | L | L | D | ACTIVE |

NOTE: X means don't care



## ABSOLUTE MAXIMUM RATINGS

| RATING | VALUE |
|---|---|
| Ambient Operating Temperature | 0 $^{o}$C to 70 $^{o}$C |
| Storage Temperature | -65 $^{o}$C to 125 $^{o}$C |
| Applied Input Voltage | -0.5V to 7.0V |
| Applied Output Voltage | -0.<br>5V to 7.0V |
| VCC to Ground Potential | -0.2V to 7.0V |
| A9 & /OE | -0.2V to 12.5V |

**wNOTICE:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
Specifications contained within the following tables are subject to change.

## RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN | TYP. | MAX |
|---|---|---|---|---|
| Vcc for ±5% device Supply Voltages | $V_{CC}$ | 4.75V | | 5.25V |
| Vcc for ± 10% device Supply Voltages | Vcc | 4.5V | | 5.5V |
| Ground | $V_{SS}$ | 0 | 0 | 0 |

## DC AND OPERATING CHARACTERISTICS ($0^{o}C \le T_A \le 70\ ^{o}C$ ; Vcc = 5V ± 0.5V )

| PARAMETER | TEST CONDITIONS | SYMBOL | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| Input Leakage Current | Vcc=Vcc max, $V_{IN}$= GND to Vcc | $I_{L1}$ | | ±1.0 | µA |
| Output Leakage Current | Vcc=Vcc max, VOUT= GND to Vcc | $I_{L0}$ | | ±10 | µA |
| Input High Voltage | | $V_{IH}$ | 0.7x $V_{CC}$ | $V_{CC}$ + 0.3 | V |

| | | | | | |
|---|---|---|---|---|---|
| Input Low Voltage | | $V_{IL}$ | -0.5 | 0.8 | V |
| Output High Voltage | $I_{OH}$ = -2.5mA, Vcc = Vcc min | $V_{OH}$ | 2.4 | | V |
| Output Low Voltage | $I_{OL}$ = 12mA, Vcc =Vcc min | $V_{OL}$ | | 0.45 | V |
| Vcc Active Current for Read | /CE=$V_{IL}$, /OE=$V_{IH}$ | $I_{CC1}$ | | 30 | mA |
| Vcc Active Current for Program | /CE=$V_{IL}$, /OE=$V_{IH}$ | $I_{CC2}$ | | 40 | mA |
| Vcc Active Current for Erase | /CE=$V_{IL}$, /OE=$V_{IH}$ | $I_{CC2}$ | | 40 | mA |
| Vcc Standby Current | /CE= $V1_H$ | $I_{cc3}$ | | 5 | mA |

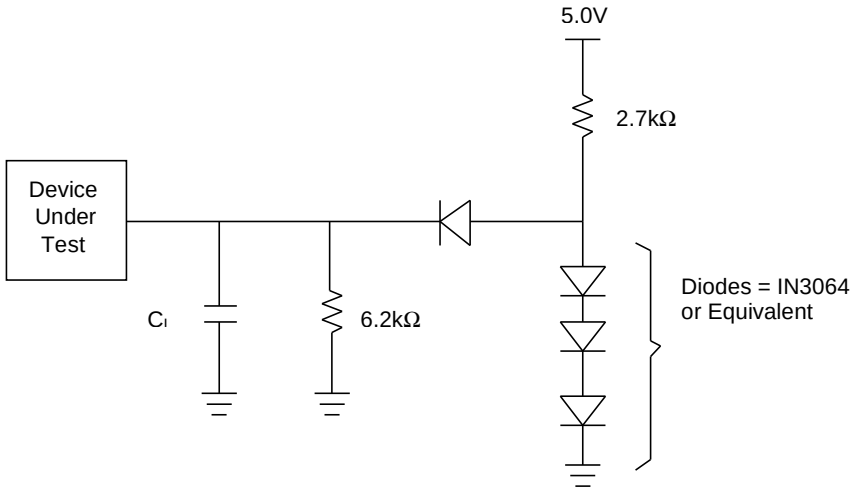
**Notes**

1.$V_{1L\ min.}$=-1.0V for pulse width is equal to or less than 50ns. $V_{1L\ min.}$ =-2.0V for pulse width is equal to or less than 20



2.$V_{1H\ max.}$ =$V_{CC}$+1.5V for pulse width is equal to or less than 20ns. If $V_{1H}$ is over the specified maximum value, read operation cannot be guaranteed.

## SWITCHING TEST CIRCUITS




**Note** : $C_L$ = 100pF including jig capacitance

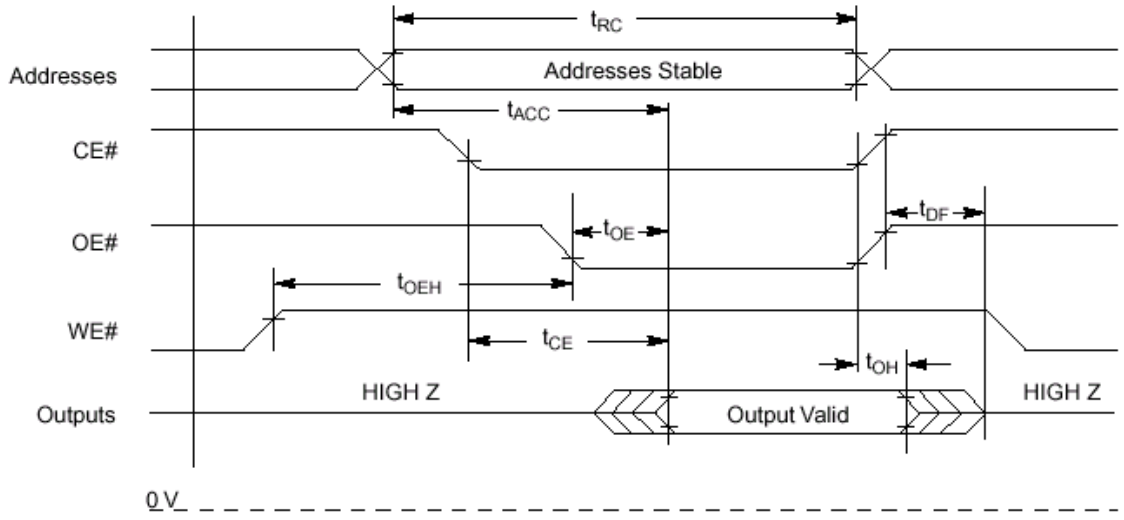
## AC CHARACTERISTICS

### u Read Only Operations Characteristics

| PARAMETER | DESCRIPTION | SPEED | | | UNIT |
|---|---|---|---|---|---|
| | | - 70 | -90 | -120 | |
| $t_{RC}$ | Read Cycle Time | 70 | 90 | 120 | ns |
| $t_{ACC}$ | Address Access time | 70 | 90 | 120 | ns |
| $t_{CE}$ | Chip Enable to Access time | 70 | 90 | 120 | ns |
| $t_{OE}$ | Output Enable time | 30 | 35 | 50 | ns |
| $t_{DF}$ | Chip Enable to Output High-Z | 20 | 20 | 30 | ns |
| $t_{OEH}$ | Output Enable Hold Time | 0 | 0 | 0 | ns |

| | | | | | |
|---|---|---|---|---|---|
| $t_{OH}$ | Output Hold Time From Addresses, /CE or /OE | 0 | 0 | 0 | ns |





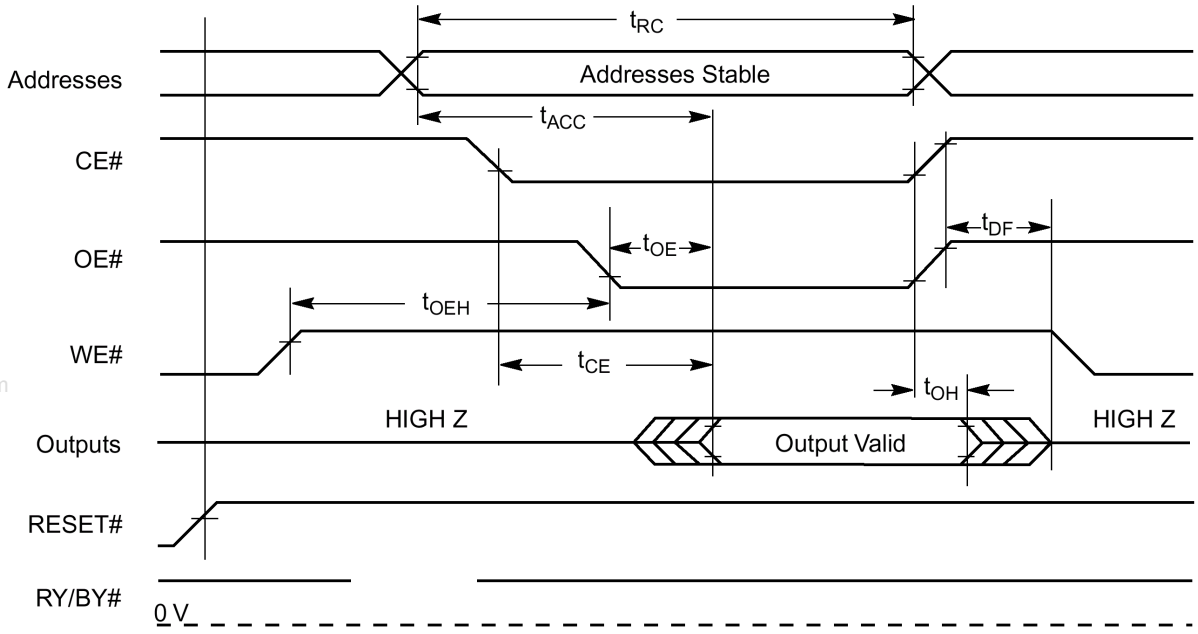

**Read Operation Timings**

## u Erase/Program Operations

| PARAMETER | DESCRIPTION | -70 | -90 | -120 | UNIT |
|---|---|---|---|---|---|
| $t_{WC}$ | Write Cycle Time (Note 1) | 70 | 90 | 120 | ns |
| $t_{AS}$ | Address Setup Time | 0 | 0 | 0 | ns |
| $t_{AH}$ | Address Hold Time | 45 | 45 | 50 | ns |
| $t_{DS}$ | Data Setup Time | 30 | 45 | 50 | ns |
| $t_{DH}$ | Data Hold Time | 0 | 0 | 0 | ns |
| $t_{OES}$ | Output Enable Setup Time | 0 | 0 | 0 | ns |
| $t_{GHWL}$ | Read Recover Time Before Write | 0 | 0 | 0 | ns |
| $t_{CS}$ | /CE Setup Time | 0 | 0 | 0 | ns |
| $t_{CH}$ | /CE Hold Time | 0 | 0 | 0 | ns |
| $t_{WP}$ | Write Pulse Width | 35 | 45 | 50 | ns |
| $t_{WPH}$ | Write Pulse Width Hi | 20 | 20 | 20 | ns |
| $t_{WHWH1}$ | Byte Programming Operation | 7 | 7 | 7 | µs |
| $t_{WHWH2}$ | Sector Erase Operation | 1 | 1 | 1 | sec |
| $t_{VCS}$ | Vcc set up time (Note 1) | 50 | 50 | 50 | µs |

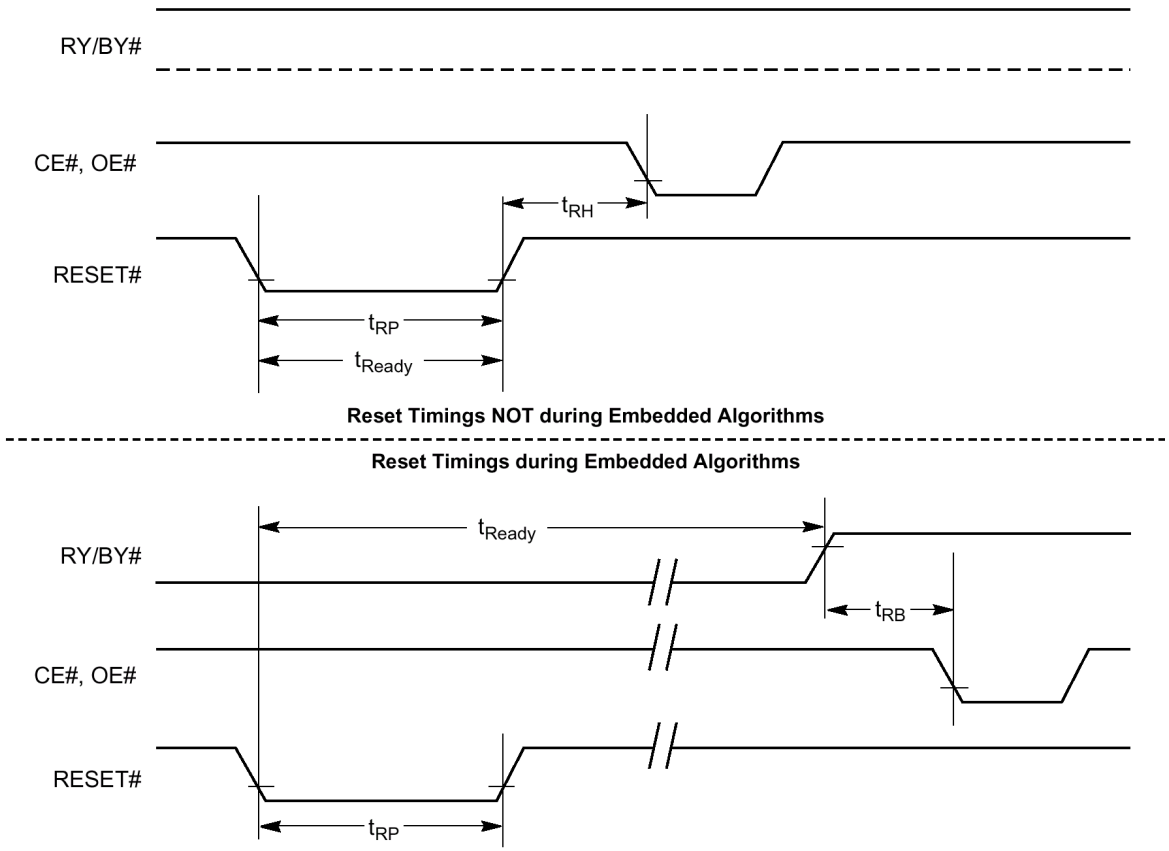
**Notes** : : 1. Not 100% tested

## u READ OPERATIONS TIMING

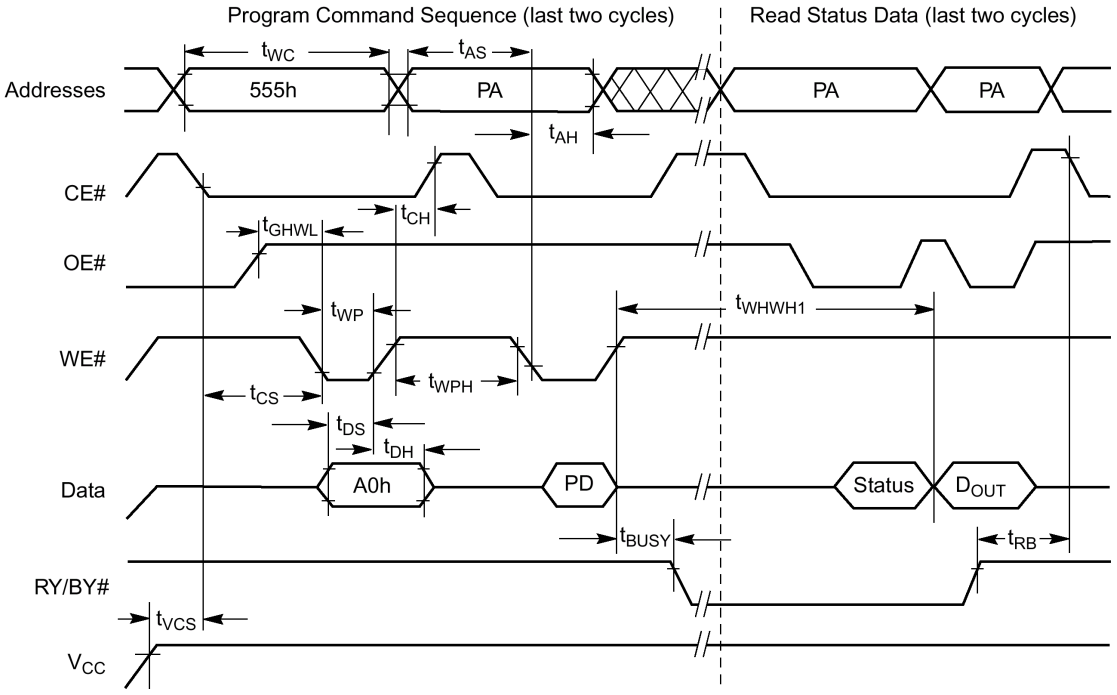





## u RESET TIMING

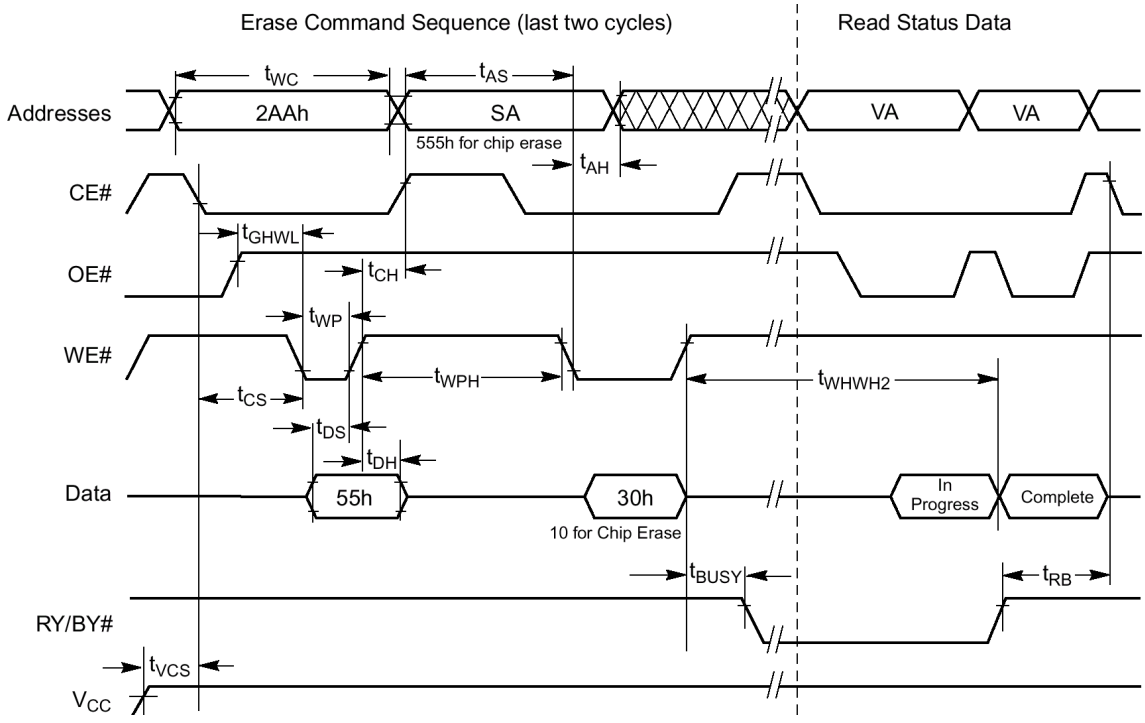


## u PROGRAM OPERATIONS TIMING

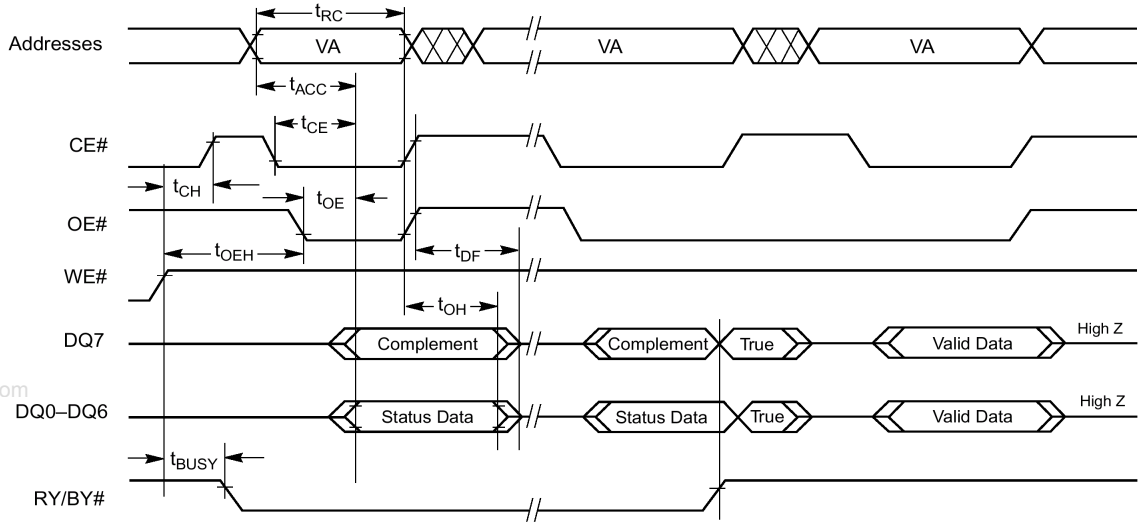





## u CHIP/SECTOR ERASE OPERATION TIMINGS

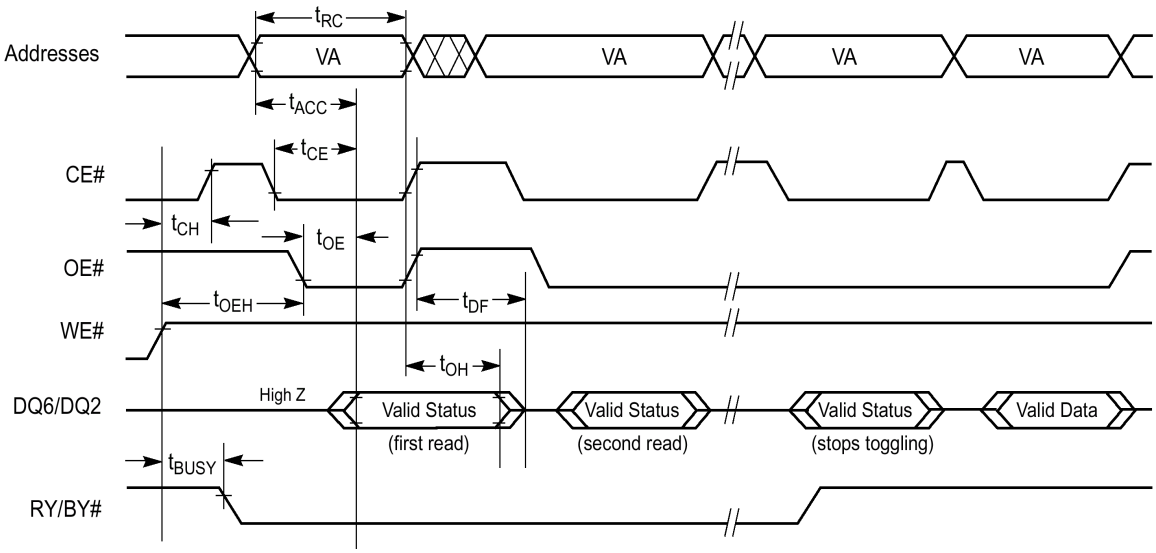


## u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)

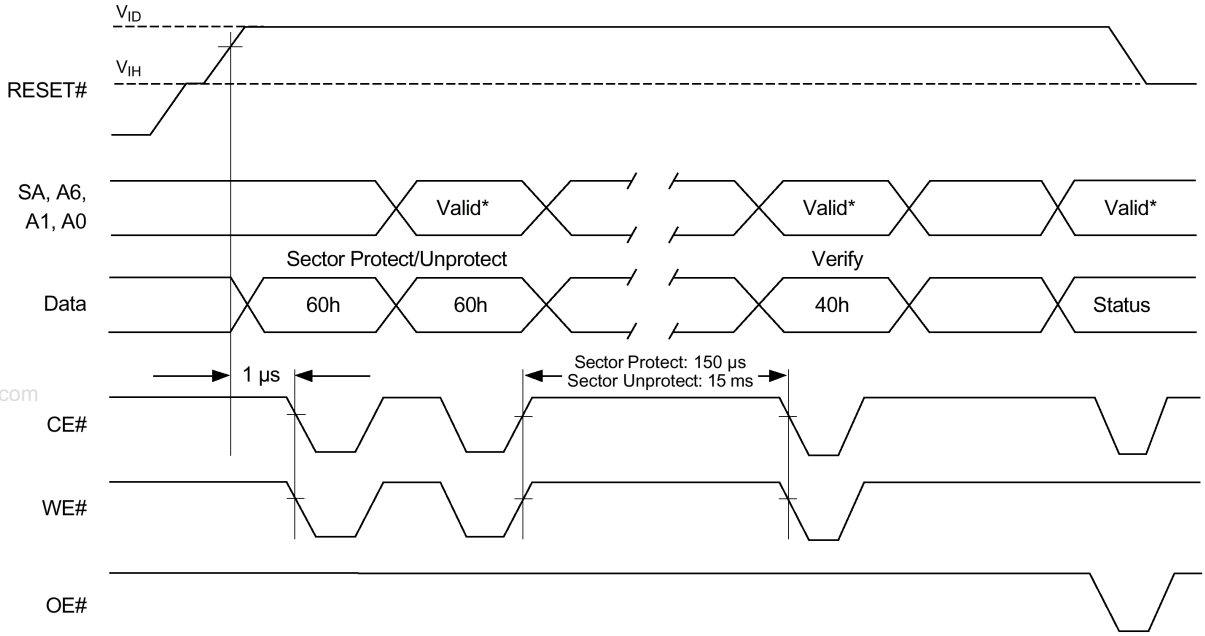





## u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)

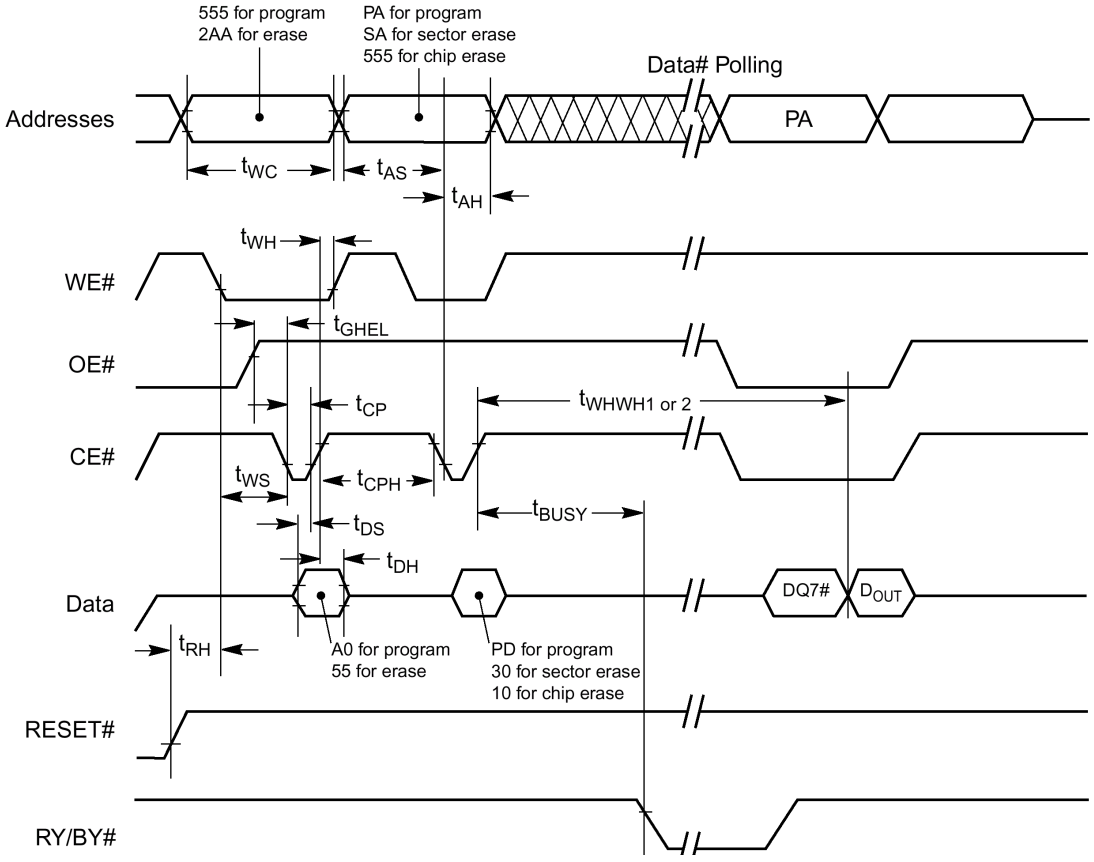


## u SECTOR PROTECT UNPROTECT TIMEING DIAGRAM

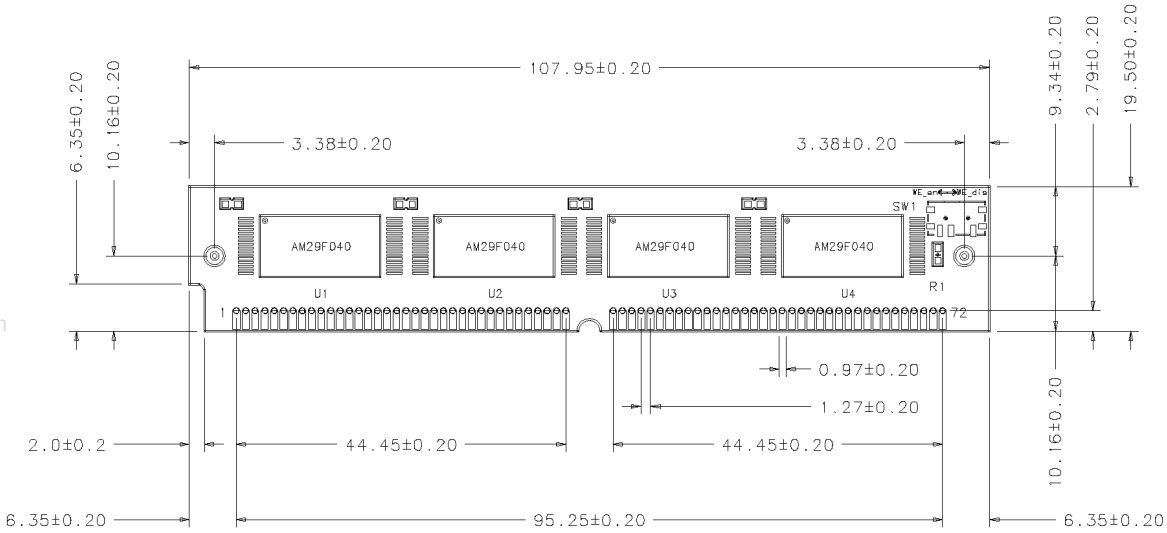




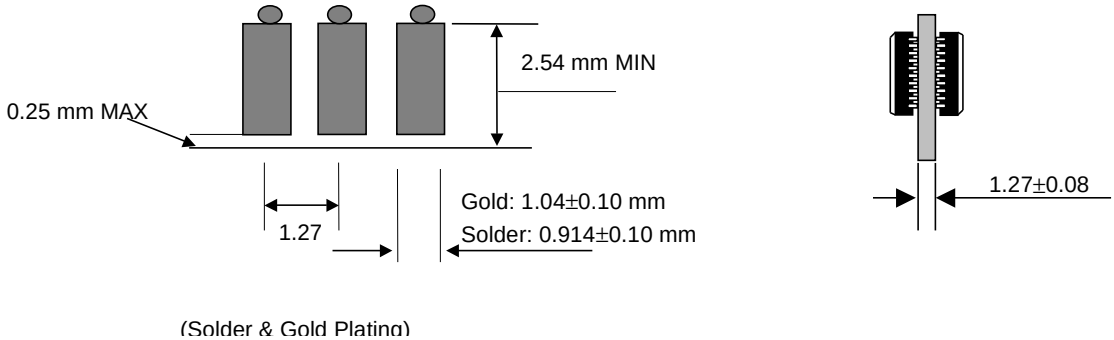

## u ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



## PACKAGE DIMMENSIONS






(Solder & Gold Plating)

## ORDERING INFORMATION

| Part Number | Density | Org. | Package | Component Number | Vcc | SPEED |
|---|---|---|---|---|---|---|
| **HMF1M32M8S-70** | 4MByte | 1MX 32bit | 72 Pin-SIMM | 8EA | 5.0V | 70ns |
| **HMF1M32M8S-90** | 4MByte | 1MX 32bit | 72 Pin-SIMM | 8EA | 5.0V | 90ns |
| **HMF1M32M8S-120** | 4MByte | 1MX 32bit | 72 Pin-SIMM | 8EA | 5.0V | 120ns |