



FLASH-ROM MODULE 8MByte (2M x 32-Bit), 72pin-SIMM, 5V
Part No. HMF2M32M8A

GENERAL DESCRIPTION

The HMF2M32M8A is a high-speed flash read only memory (FROM) module containing 2,097,152 words organized in a x32bit configuration. The module consists of eight 1M x 8 FROM mounted on a 72 -pin, double-sided, FR4-printed circuit board.

The HMF2M32M8A is entirely pin and command set compatible with JEDEC standard 4M-bit EEPROMs. Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.

Eight chip enable inputs, (/1CSLL, /2CSLL, /1CSLH, /2CSLH, /1CSHL, /2CSHL, /1CSHH, /2CSHH) are used to enable the module's 4 bytes independently. Output enable (/OE) and write enable (/WE) can set the memory input and output.

When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single +5V DC power supply and all inputs and outputs are TTL-compatible.

FEATURES

- w Access time : 75, 90 and 120ns
- w High-density 8MByte design
- w High-reliability, low-power design
- w Single + 5V \pm 0.5V power supply
- w Easy memory expansion
- w All inputs and outputs are TTL-compatible
- w FR4-PCB design
- w Low profile 72-pin SIMM
- w Minimum 1,000,000 write/erase cycle
- w Sectors erase architecture
- w Sector group protection
- w Temporary sector group unprotection
- w The used device is Am29F080B

OPTIONS

w Timing

| | |
|--------------|------|
| 75ns access | - 75 |
| 90ns access | - 90 |
| 120ns access | -120 |

w Packages

| | |
|-------------|---|
| 72-pin SIMM | M |
|-------------|---|

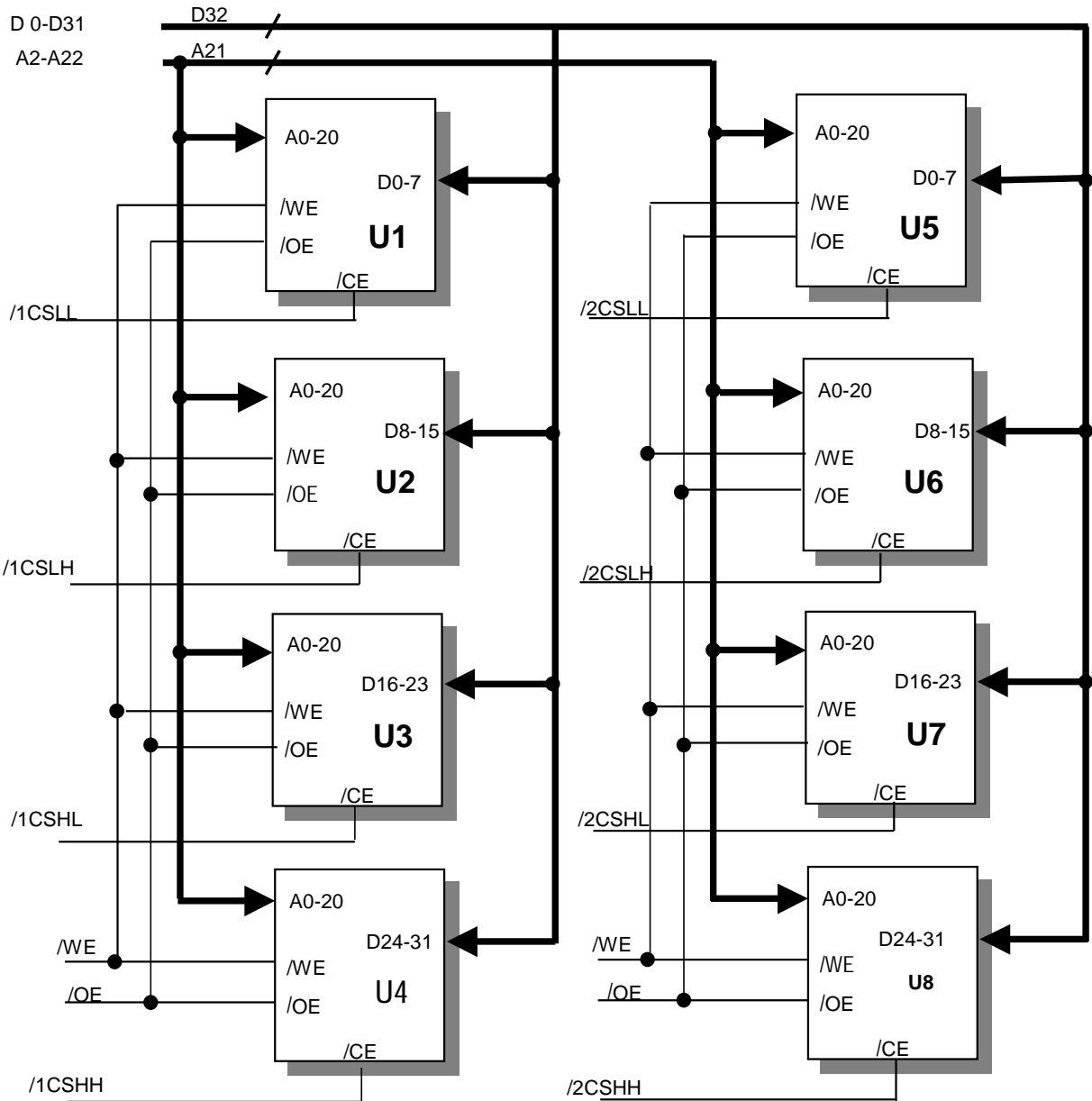
MARKING

PIN ASSIGNMENT

| PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL |
|-----|--------|-----|--------|-----|--------|
| 1 | Vss | 25 | D17 | 49 | /WE |
| 2 | NC | 26 | D18 | 50 | A20 |
| 3 | D0 | 27 | D19 | 51 | A19 |
| 4 | D1 | 28 | D20 | 52 | A18 |
| 5 | D2 | 29 | D21 | 53 | A17 |
| 6 | D3 | 30 | Vcc | 54 | A16 |
| 7 | D4 | 31 | D22 | 55 | A15 |
| 8 | D5 | 32 | D23 | 56 | A14 |
| 9 | D6 | 33 | /1CSHL | 57 | A13 |
| 10 | VCC | 34 | /2CSHL | 58 | A12 |
| 11 | D7 | 35 | D24 | 59 | Vcc |
| 12 | /1CSLL | 36 | D25 | 60 | A11 |
| 13 | /2CSLL | 37 | D26 | 61 | A10 |
| 14 | D8 | 38 | D27 | 62 | A9 |
| 15 | D9 | 39 | Vss | 63 | A8 |
| 16 | D10 | 40 | D28 | 64 | A7 |
| 17 | D11 | 41 | D29 | 65 | A6 |
| 18 | D12 | 42 | D30 | 66 | A5 |
| 19 | D13 | 43 | D31 | 67 | A4 |
| 20 | D14 | 44 | /1CSHH | 68 | A3 |
| 21 | D15 | 45 | /2CSHH | 69 | A2 |
| 22 | /1CSLH | 46 | VCC | 70 | A21 |
| 23 | /2CSLH | 47 | /RESET | 71 | A22 |
| 24 | D16 | 48 | /OE | 72 | Vss |

72-PIN SIMM
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

| MODE | /OE | /CE | /WE | DQ | POWER |
|----------------|-----|-----|-----|--------|---------|
| STANDBY | X | H | X | HIGH-Z | STANDBY |
| NOT SELECTED | H | L | H | HIGH-Z | ACTIVE |
| READ | L | L | H | Q | ACTIVE |
| WRITE or ERASE | X | L | L | D | ACTIVE |

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING |
|---|--------------|-----------------|
| Voltage with respect to ground all other pins | $V_{IN,OUT}$ | -2.0V to +7.0V |
| Voltage with respect to ground V_{CC} | V_{CC} | -2.0V to +7.0V |
| Storage Temperature | T_{STG} | -65°C to +125°C |
| Operating Temperature | T_A | -55°C to +125°C |

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED DC OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN | TYP. | MAX |
|--|----------|-------|------|-------|
| V_{CC} for $\pm 5\%$ device Supply Voltages | V_{CC} | 4.75V | | 5.25V |
| V_{CC} for $\pm 10\%$ device Supply Voltages | V_{CC} | 4.5V | | 5.5V |
| Ground | V_{SS} | 0 | 0 | 0 |

DC AND OPERATING CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{CC} = 5\text{V} \pm 0.5\text{V}$)

| PARAMETER | TEST CONDITIONS | SYMBOL | MIN | MAX | UNITS |
|---|---|-----------|----------------------|-----------|---------------|
| Input Leakage Current | $V_{CC}=V_{CC} \text{ max, } V_{IN}=\text{GND to } V_{CC}$ | I_{L1} | | ± 8.0 | μA |
| Output Leakage Current | $V_{CC}=V_{CC} \text{ max, } V_{OUT}=\text{GND to } V_{CC}$ | I_{LO} | | ± 8.0 | μA |
| Output High Voltage | $I_{OH} = -2.5\text{mA, } V_{CC} = V_{CC} \text{ min}$ | V_{OH} | $0.85 \times V_{CC}$ | | V |
| Output Low Voltage | $I_{OL} = 12\text{mA, } V_{CC} = V_{CC} \text{ min}$ | V_{OL} | | 0.45 | V |
| V_{CC} Active Current for Read(1) | $/\text{CE} = V_{IL}, /\text{OE}=V_{IH}$ | I_{CC1} | | 320 | mA |
| V_{CC} Active Current for Program or Erase(2) | $/\text{CE} = V_{IL}, /\text{OE}=V_{IH}$ | I_{CC2} | | 320 | mA |
| V_{CC} Standby Current | $/\text{CE}= V_{IH}$ | I_{CC3} | | 40 | μA |
| Low V_{CC} Lock-Out Voltage | | V_{LKO} | 3.2 | 4.2 | V |

Notes:

1. The I_{CC} current listed is typically less than 2mA/MHz, with $/\text{OE}$ at V_{IH} .

2. Icc active while embedded algorithm (program or erase) is in progress

3. Maximum Icc current specifications are tested with Vcc=Vcc max

ERASE AND PROGRAMMING PERFORMANCE

| PARAMETER | LIMITS | | | UNIT | COMMENTS |
|-----------------------|--------|------|------|------|---|
| | MIN. | TYP. | MAX. | | |
| Sector Erase Time | - | 1 | 8 | sec | Excludes 00H programming prior to erasure |
| Byte Programming Time | - | 7 | 300 | µs | Excludes system-level overhead |
| Chip Programming Time | - | 7.2 | 21.6 | sec | Excludes system-level overhead |

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CAPACITANCE

| PARAMETER SYMBOL | PARAMETER DESCRIPTION | TEST SETUP | MIN | MAX | UNIT |
|------------------|-------------------------|----------------------|-----|-----|------|
| C _{IN} | Input Capacitance | V _{IN} = 0 | 6 | 7.5 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0 | 8.5 | 12 | pF |
| C _{IN2} | Control Pin Capacitance | V _{IN} = 0 | 7.5 | 9 | pF |

Notes : Test conditions T_A = 25° C, f=1.0 MHz.

AC CHARACTERISTICS

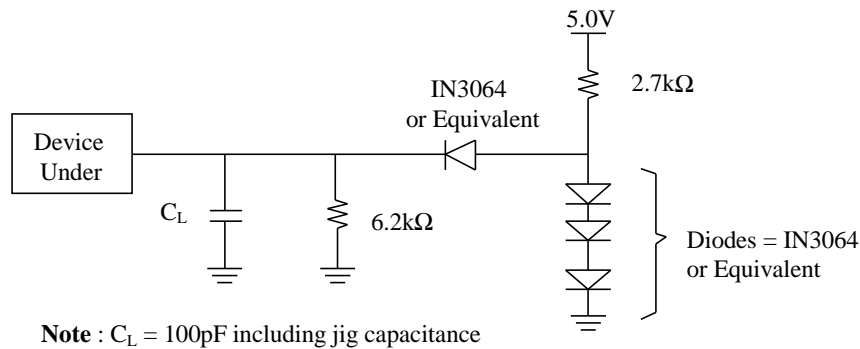
u Read Only Operations Characteristics

| PARAMETER SYMBOLS | | DESCRIPTION | TEST SETUP | | -75 | -90 | -120 | UNIT |
|-------------------|------------------|--|--|-----|-----|-----|------|------|
| JEDEC | STANDAR D | | | | | | | |
| t _{AVAV} | t _{RC} | Read Cycle Time | | Min | 70 | 90 | 120 | ns |
| t _{AVQV} | t _{ACC} | Address to Output Delay | /CE = V _{IL} /OE = V _{IL} | Max | 70 | 90 | 120 | ns |
| t _{ELQV} | t _{CE} | Chip Enable to Output Delay | /OE = V _{IL} | Max | 70 | 90 | 120 | ns |
| t _{GLQV} | t _{OE} | Chip Enable to Output Delay | | Max | 40 | 40 | 50 | ns |
| t _{EHQZ} | t _{DF} | Chip Enable to Output High-Z | | Max | 20 | 20 | 30 | ns |
| t _{GHQZ} | t _{DF} | Output Enable to Output High-Z | | Max | 20 | 20 | 30 | ns |
| t _{AXQX} | t _{QH} | Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First | | Min | 0 | 0 | 0 | ns |

TEST SPECIFICATIONS

| TEST CONDITION | 75 | ALL OTHERS | UNIT |
|--|-----------|------------|------|
| Output load | 1TTL gate | | |
| Output load capacitance, C_L (Including jig capacitance) | 30 | 100 | pF |
| Input rise and full times | 5 | 20 | ns |
| Input pulse levels | 0.0 - 3.0 | 0.45-2.4 | V |
| Input timing measurement reference levels | 1.5 | 0.8, 2.0 | V |
| Output timing measurement reference levels | 1.5 | 0.8, 2.0 | V |

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u Erase/Program Operations

| PARAMETER SYMBOLS | | DESCRIPTION | | -75 | -90 | -120 | UNIT |
|-------------------|-------------|--------------------------------|-----|-----|-----|------|---------------|
| JEDEC | STANDARD | | | | | | |
| t_{AVAV} | t_{WC} | Write Cycle Time | Min | 70 | 90 | 120 | ns |
| t_{AVWL} | t_{AS} | Address Setup Time | Min | 0 | | | ns |
| t_{WLAX} | t_{AH} | Address Hold Time | Min | 40 | 45 | 50 | ns |
| t_{DVWH} | t_{DS} | Data Setup Time | Min | 40 | 45 | 50 | ns |
| t_{WHDX} | t_{DH} | Data Hold Time | Min | 0 | | | ns |
| | t_{OES} | Output Enable Setup Time | Min | 0 | | | ns |
| t_{GHWL} | t_{GHWL} | Read Recover Time Before Write | Min | 0 | | | ns |
| t_{ELWL} | t_{CS} | /CE Setup Time | Min | 0 | | | ns |
| t_{WHEH} | t_{CH} | /CE Hold Time | Min | 0 | | | ns |
| t_{WLWH} | t_{WP} | Write Pulse Width | Min | 40 | 45 | 50 | ns |
| t_{WHWL} | t_{WPH} | Write Pulse Width High | Min | 20 | | | ns |
| t_{WHWH1} | t_{WHWH1} | Byte Programming Operation | Typ | 7 | | | μs |
| t_{WHWH2} | t_{WHWH2} | Sector Erase Operation (Note1) | Typ | 1 | | | sec |
| | t_{VCS} | Vcc set up time | Min | 50 | | | μs |

- Notes :
1. This does not include the preprogramming time
 2. This timing is only for Sector Protect operations

U Erase/Program Operations

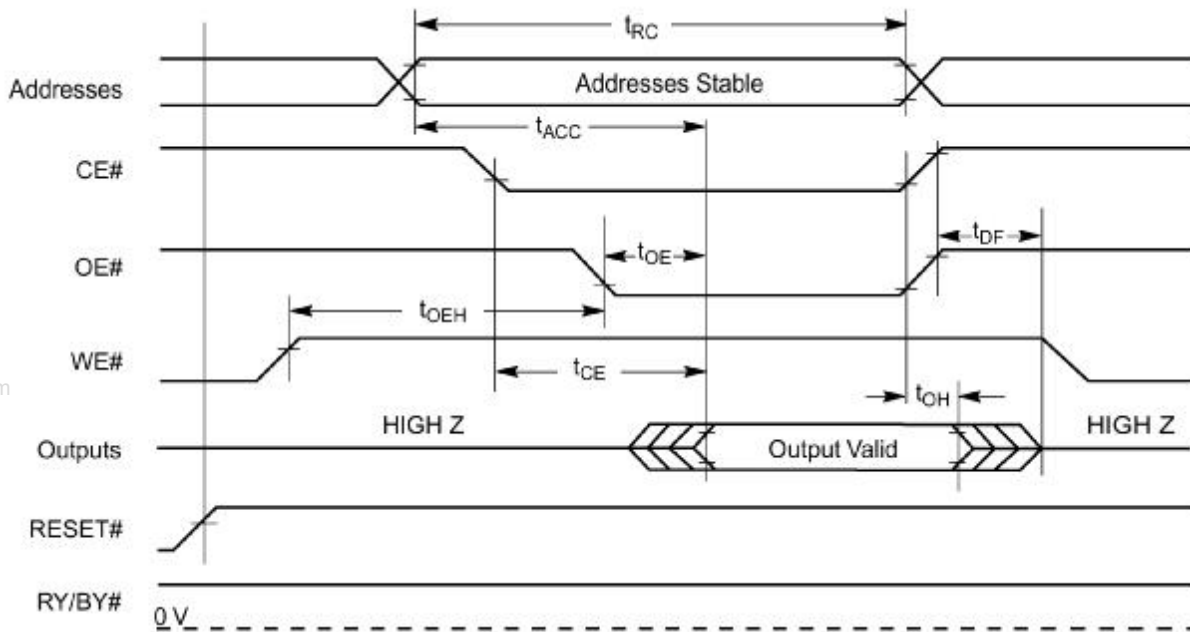
Alternate /CE Controlled Writes

| PARAMETER SYMBOLS | | DESCRIPTION | | -75 | -90 | -120 | UNIT |
|--------------------|--------------------|--------------------------------|-----|-----|-----|------|------|
| JEDEC | STANDARD | | | | | | |
| t _{AVAV} | t _{WC} | Write Cycle Time | Min | 70 | 90 | 120 | ns |
| t _{AVWL} | t _{AS} | Address Setup Time | Min | 0 | | | ns |
| t _{WLAX} | t _{AH} | Address Hold Time | Min | 40 | 45 | 50 | ns |
| t _{DVWH} | t _{DS} | Data Setup Time | Min | 40 | 45 | 50 | ns |
| t _{WHDX} | t _{DH} | Data Hold Time | Min | 0 | | | ns |
| t _{GHEL} | t _{GHEL} | Read Recover Time Before Write | Min | 0 | | | ns |
| t _{WLEL} | t _{WS} | /CE Setup Time | Min | 0 | | | ns |
| t _{EHWH} | t _{WH} | /CE Hold Time | Min | 0 | | | ns |
| t _{ELEH} | t _{CP} | Write Pulse Width | Min | 40 | 45 | 50 | ns |
| t _{EHEL} | t _{CPH} | Write Pulse Width High | Min | 20 | | | ns |
| t _{WHWH1} | t _{WHWH1} | Byte Programming Operation | Typ | 7 | | | μs |
| t _{WHWH2} | t _{WHWH2} | Sector Erase Operation (Note1) | Typ | 1 | | | sec |

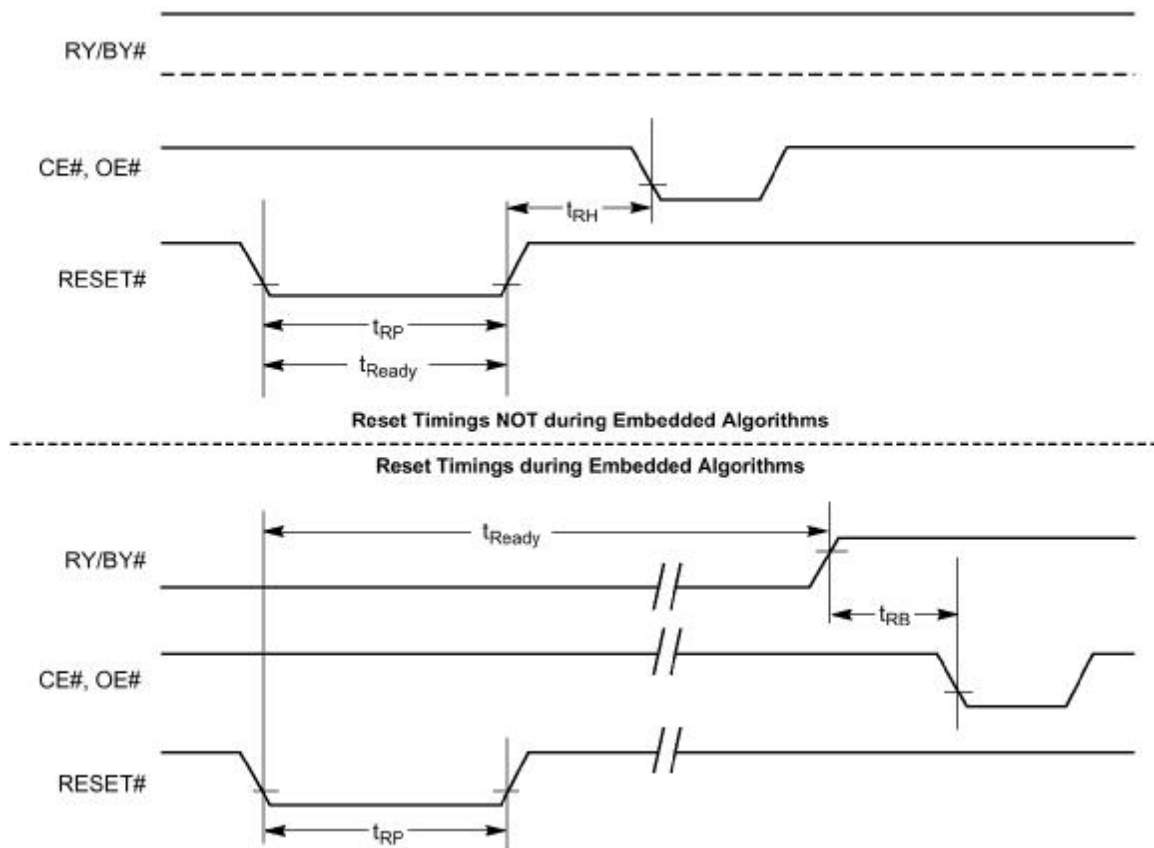
Notes :

1. This does not include the preprogramming time
2. This timing is only for Sector Protect operations

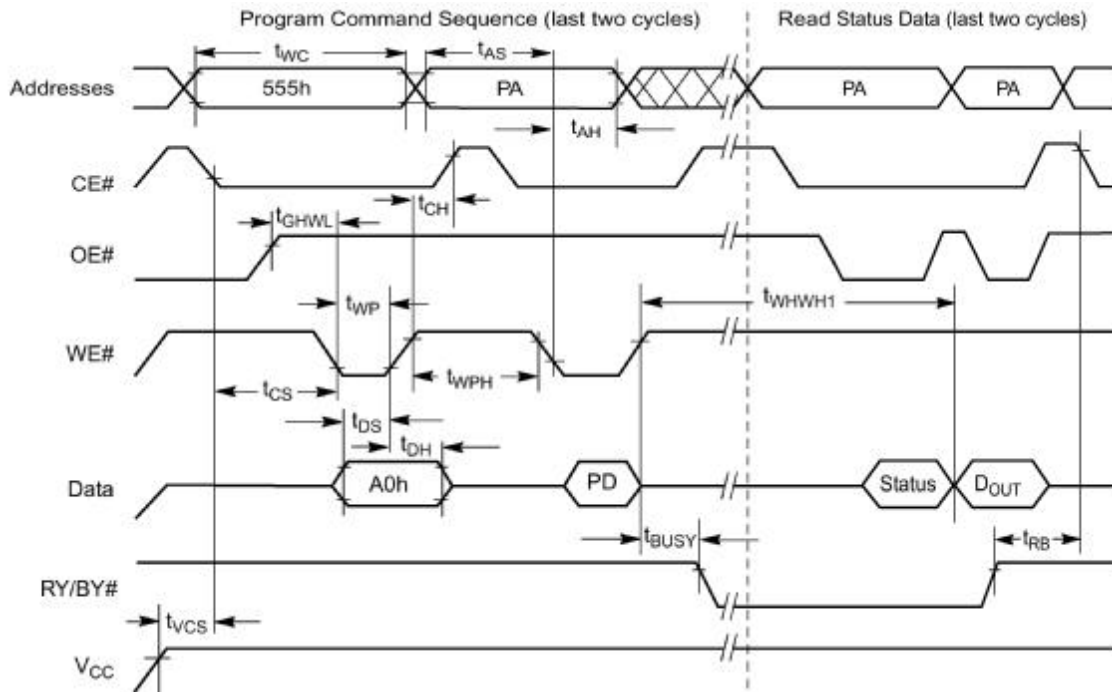
U READ OPERATIONS TIMING



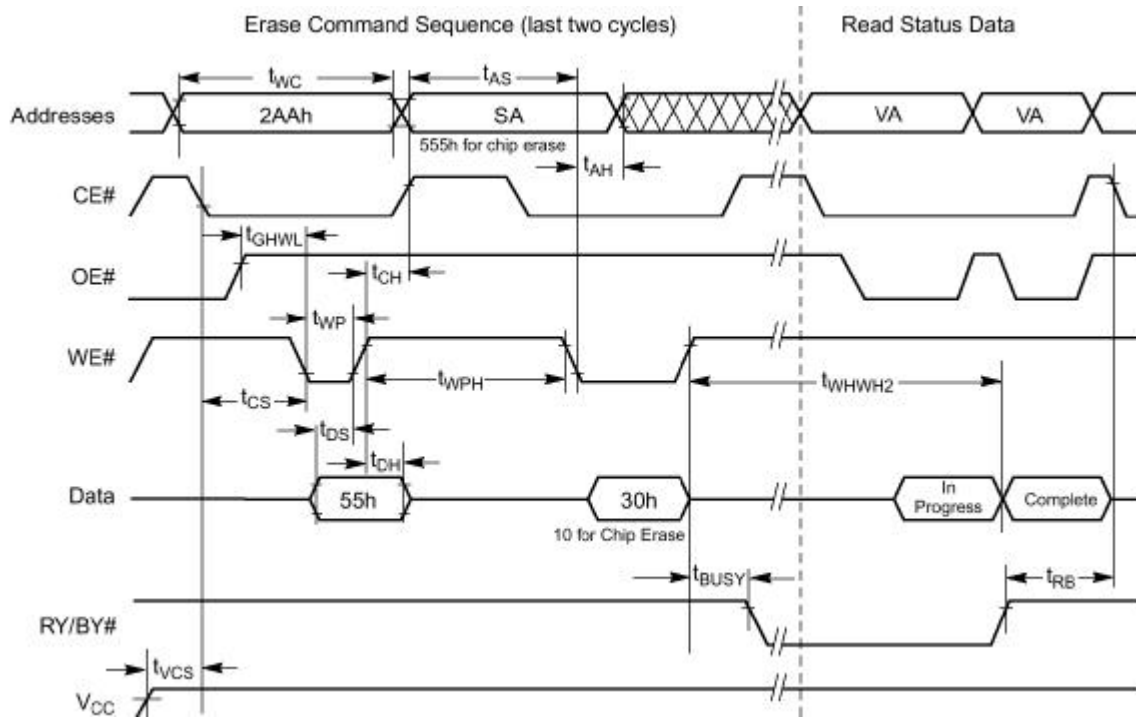
U RESET TIMING



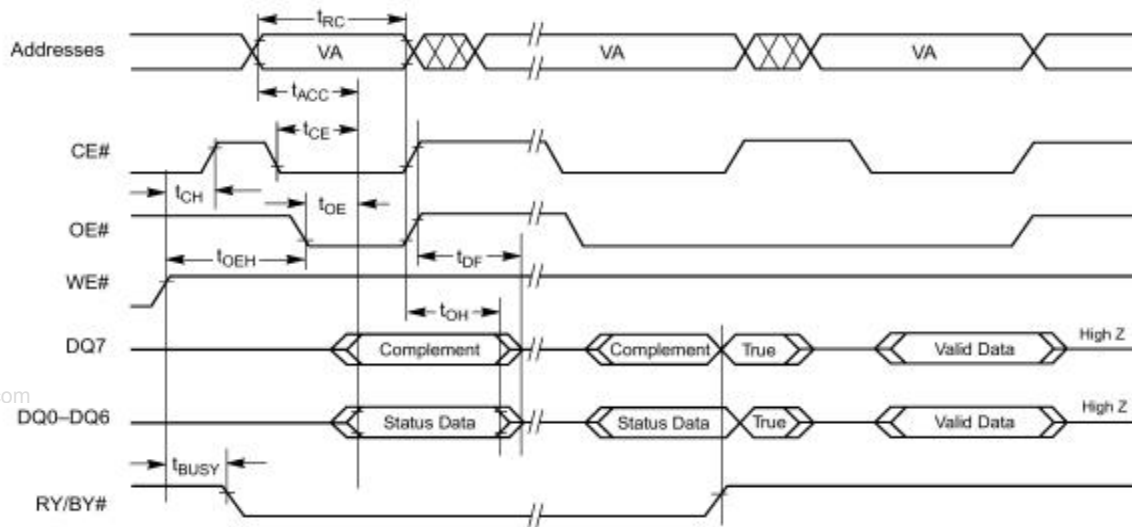
U PROGRAM OPERATIONS TIMING



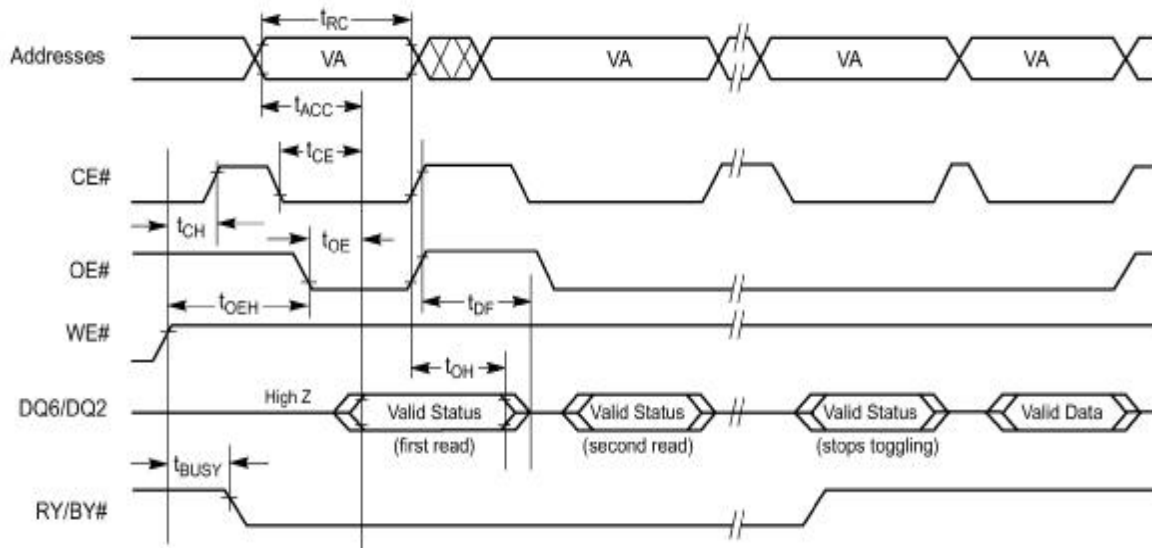
U CHIP/SECTOR ERASE OPERATION TIMINGS



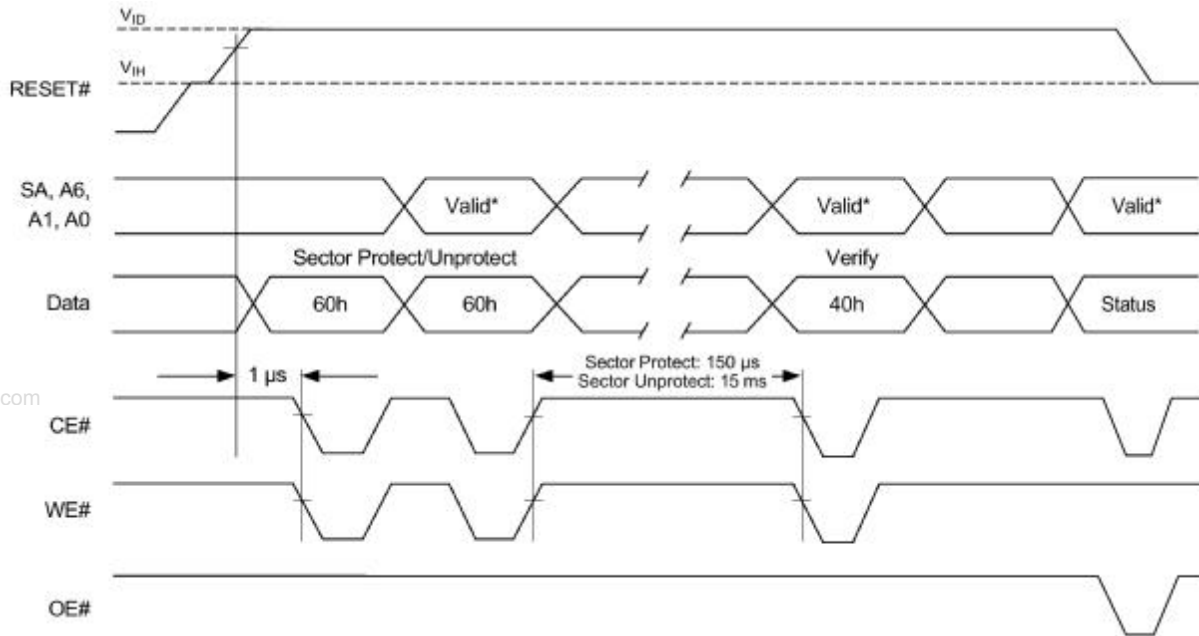
U DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



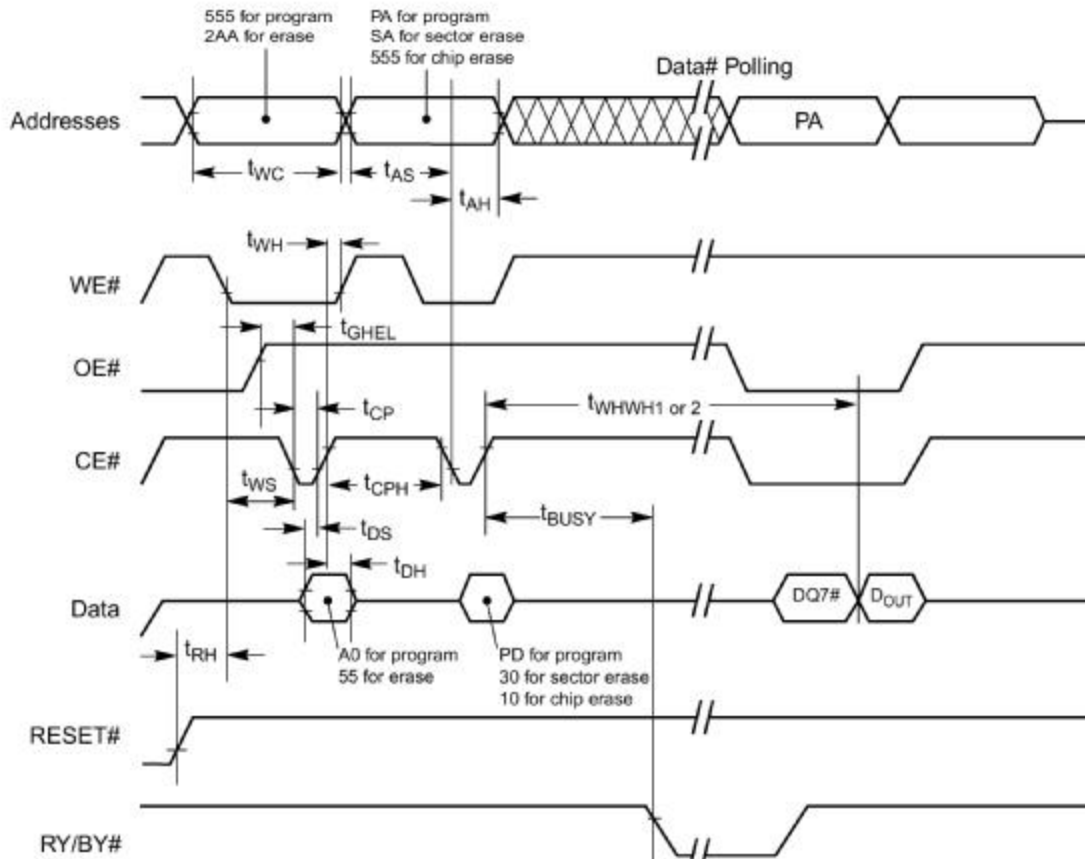
U TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



U SECTOR PROTECT UNPROTECT TIMEING DIAGRAM

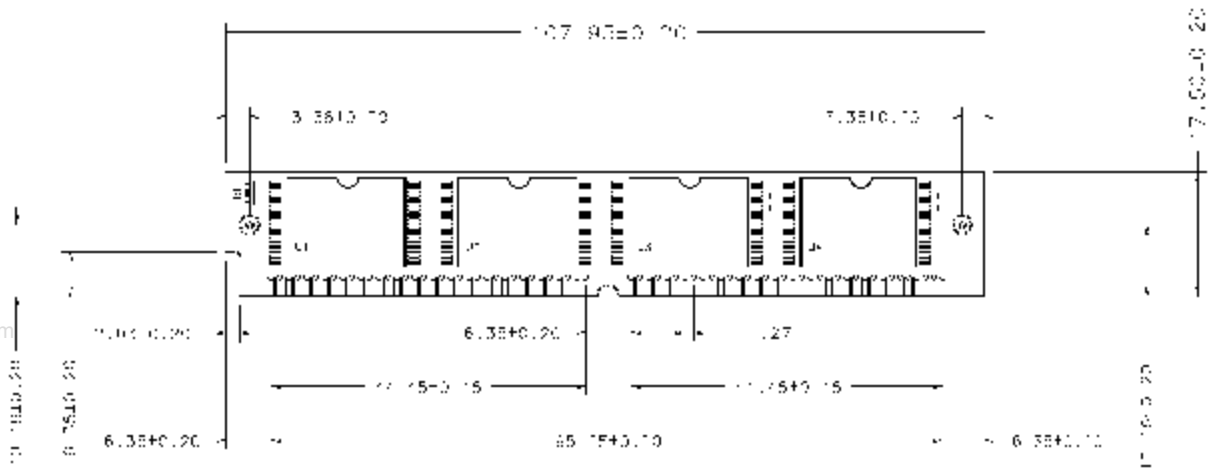


U ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS

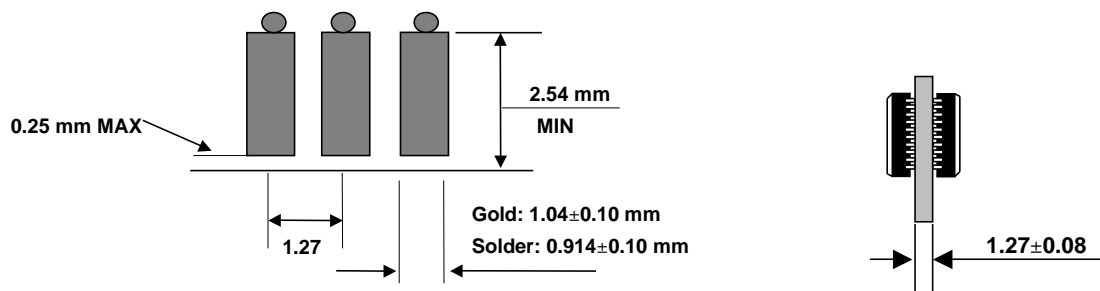
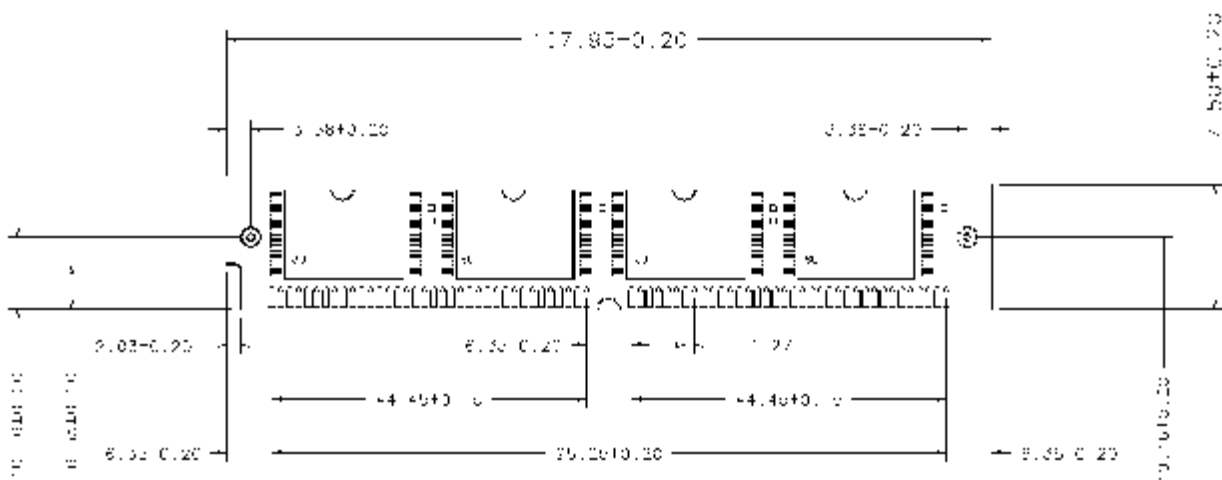


PACKAGE DIMENSIONS

(Front-Side)



(Rear-Side)



(Solder & Gold Plating)

ORDERING INFORMATION

| Part Number | Density | Org. | Package | Component Number | Vcc | SPEED |
|----------------|---------|----------|------------|------------------|------|-------|
| HMF2M32M8A-75 | 8MByte | 2M×32bit | 72Pin-SIMM | 8EA | 5.0V | 75ns |
| HMF2M32M8A-90 | 8MByte | 2M×32bit | 72Pin-SIMM | 8EA | 5.0V | 90ns |
| HMF2M32M8A-120 | 8MByte | 2M×32bit | 72Pin-SIMM | 8EA | 5.0V | 120ns |

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