



**FLASH-ROM MODULE 12MByte (3M x 32-Bit) ,72pin-SIMM, 3.3V**  
**Part No. HMF3M32M6V**

## GENERAL DESCRIPTION

The HMF3M32M6VA is a high-speed flash read only memory (FROM) module containing 6,291,456 words organized in a x32bit configuration. The module consists of six 1M x 16 FROM mounted on a 72-pin, single-sided, FR4-printed circuit board. Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other flash or EPROM devices.

Output enable (/OE) and write enable (/WE) can set the memory input and output.

When FROM module is disable condition the module is becoming power standby mode, system designer can get low -power design. All module components may be powered from a single +3.0V DC power supply.

## FEATURES

- w Access time : 70,80, 90 and 120ns
- w High-density 12MByte design
- w High-reliability, low-power design
- w Single + 3V  $\pm$  0.3V power supply
- w Easy memory expansion
- w Hardware reset pin(RESET#)
- w FR4-PCB design
- w Low profile 72-pin SIMM
- w Minimum 1,000,000 write/erase cycle
- w Flexible sector architecture
- w Embedded algorithms
- w Erase suspend / Erase resume

## OPTIONS

w Timing

70ns access	-70
80ns access	-80
90ns access	-90
120ns access	-120

w Packages

72-pin SIMM	M
-------------	---

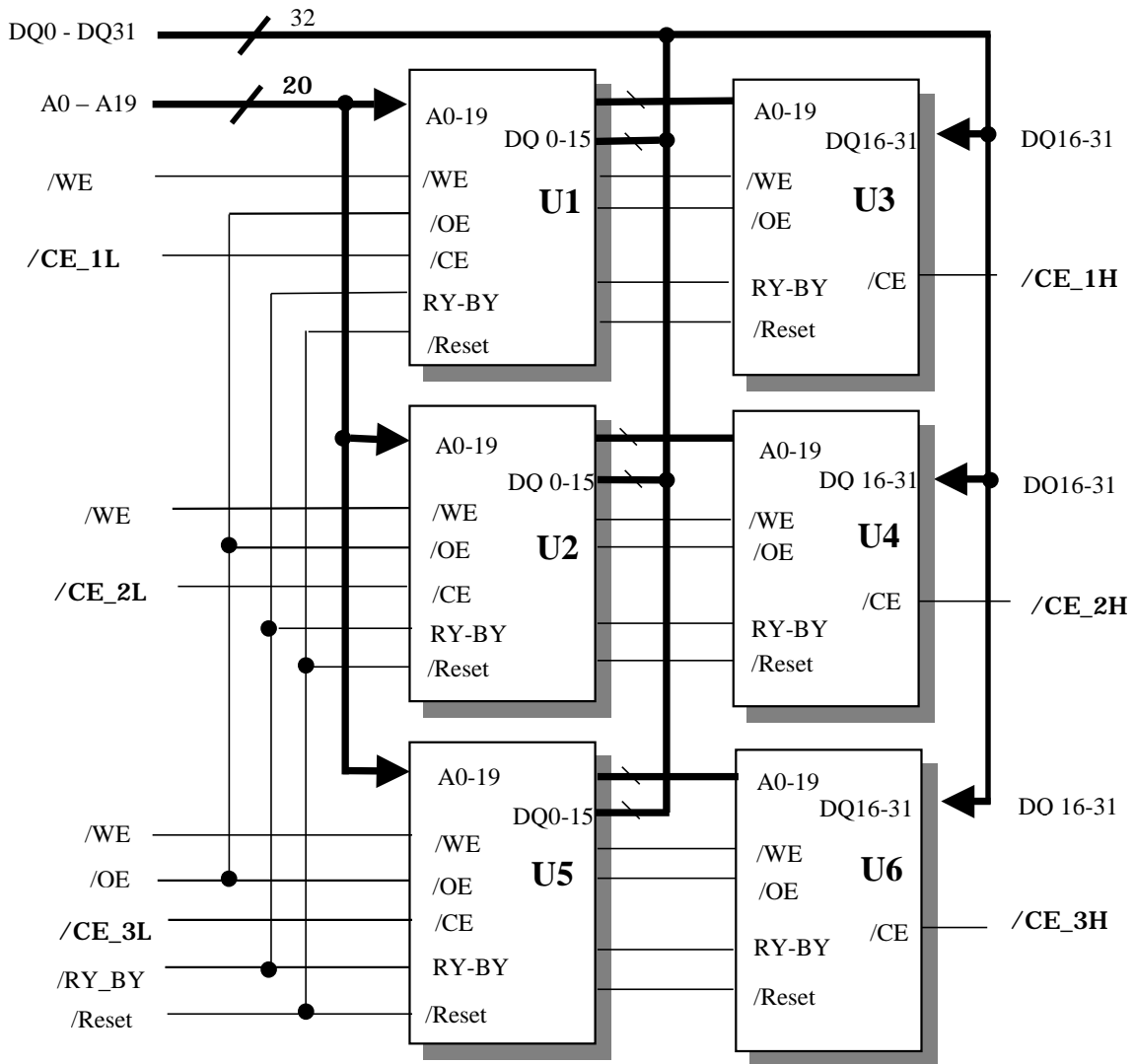
## MARKING

## PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vss	25	DQ17	49	/WE
2	/RESET	26	DQ18	50	A18
3	DQ0	27	DQ19	51	A17
4	DQ1	28	DQ20	52	A16
5	DQ2	29	DQ21	53	A15
6	DQ3	30	Vcc	54	A14
7	DQ4	31	DQ22	55	A13
8	DQ5	32	DQ23	56	A12
9	DQ6	33	/CE_1H	57	A11
10	Vcc	34	/CE_2H	58	A10
11	DQ7	35	DQ24	59	Vcc
12	/CE_1L	36	DQ25	60	A9
13	/CE_2L	37	DQ26	61	A8
14	DQ8	38	DQ27	62	A7
15	DQ9	39	Vss	63	A6
16	DQ10	40	DQ28	64	A5
17	DQ11	41	DQ29	65	A4
18	DQ12	42	DQ30	66	A3
19	DQ13	43	DQ31	67	A2
20	DQ14	44	NC	68	A1
21	DQ15	45	NC	69	A0
22	NC	46	/CE_3L	70	NC
23	/CE_3H	47	A19	71	NC
24	DQ16	48	/OE	72	Vss

## 72-PIN SIMM TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



www.DataSheet4U.com

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATING
Voltage on Any Pin Relative to Vss	V <sub>IN,OUT</sub>	-0.5V to +4.0V
Voltage on Vcc Supply Relative to Vss	V <sub>CC</sub>	-0.5V to +4.0V
Power Dissipation	P <sub>D</sub>	6W
Storage Temperature	T <sub>STG</sub>	-65°C to +150°C
Operating Temperature	T <sub>A</sub>	-55°C to +125°C

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

www.DataSheet4U.com

**RECOMMENDED DC OPERATING CONDITIONS**

PARAMETER	SYMBOL	MIN	TYP.	MAX
Supply Voltage	V <sub>CC</sub>	2.7V	3.0V	3.6V
Ground	V <sub>SS</sub>	0	0	0
Input High Voltage	V <sub>IH</sub>	2.0	-	V <sub>CC</sub> +0.3V
Input Low Voltage	V <sub>IL</sub>	-0.5	-	0.8V

**DC CHARACTERISTICS (CMOS Compatible)**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP.	MAX	UNIT
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub> , V <sub>CC</sub> =V <sub>CC</sub> max			±1.0	μA
I <sub>LIT</sub>	A9 Input Load Current	V <sub>CC</sub> = V <sub>CC</sub> max ; A9=12.5V			35	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub> , V <sub>CC</sub> = V <sub>CC</sub> max			±1.0	μA
I <sub>CC1</sub>	V <sub>CC</sub> Active Read Current (Note1)	/CE=V <sub>IK</sub> , /OE=V <sub>IH</sub>	5MHZ	9	16	mA
		Byte Mode	1MHZ	2	4	
		/CE=V <sub>IL</sub> , /OE=V <sub>IH</sub>	5MHZ	9	16	
		Word Mode	1MHZ	2	4	
I <sub>CC2</sub>	V <sub>CC</sub> Active Write Current (Note 2 and 4)	/CE=V <sub>IL</sub> , /OE=V <sub>IH</sub>		20	30	mA
I <sub>CC3</sub>	V <sub>CC</sub> Standby Current	V <sub>CC</sub> =V <sub>CC</sub> max ; /CE,/Reset=V <sub>CC</sub> ±0.3V		0.2	5	μA
I <sub>CC4</sub>	V <sub>CC</sub> Standby Current During Reset	V <sub>CC</sub> =V <sub>CC</sub> max ; /Reset=V <sub>SS</sub> ±0.3V		0.2	5	μA
I <sub>CC5</sub>	Automatic Sleep Mode(Note3)	V <sub>IH</sub> =V <sub>CC</sub> ±0.3V; V <sub>IL</sub> =V <sub>SS</sub> ±0.3V		0.2	5	μA
V <sub>IL</sub>	Input Low Voltage		-0.5		0.8	V
V <sub>IH</sub>	Input High Voltage		0.7xV <sub>CC</sub>		V <sub>CC</sub> +0.3	V

V <sub>ID</sub>	Voltage for Autoselect and Temporary Unprotect	V <sub>CC</sub> =3.3V	11.5		12.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> =4.0mA, V <sub>CC</sub> =V <sub>CC</sub> min			0.45	V
V <sub>OH1</sub>	Output High Voltage	I <sub>OH</sub> =-2.0mA, V <sub>CC</sub> =V <sub>CC</sub> min	0.85xV <sub>c</sub>			V
V <sub>OH2</sub>		I <sub>OH</sub> =-100uA, V <sub>CC</sub> = V <sub>CC</sub> min	V <sub>CC</sub> -0.4			V
V <sub>LKO</sub>	Low V <sub>CC</sub> Lock-Out Voltage		2.3		2.5	V

**Note :**

1. The I<sub>CC</sub> current listed is typically less 2mA/MHz, with /OE at V<sub>IH</sub>. Typical V<sub>CC</sub> is 3.0V.
2. I<sub>CC</sub> active while Embedded Erase or Embedded Program is progress.
3. Automatic sleep mode enables the low power mode when addresses remain stable for t<sub>ACC</sub>+30ns. Typical sleep mode current is 200nA.
4. Not 100% tested.

**LATCHUP CHARACTERISTICS**

DESCRIPTION	MIN	MAX
Input Voltage with respect to V <sub>SS</sub> on all pins except I/O Pins (Including A9,/OE, and /Reset)	-1.0V	12.5V
Input Voltage with respect to V <sub>SS</sub> on all I/O Pins	-1.0V	V <sub>CC</sub> +1.0V
V <sub>CC</sub> Current	-100mA	+100mA

Includes all pins except V<sub>CC</sub>. Test conditions: V<sub>CC</sub>=3.0V, one pin at a time.

**DATA RETENTION**

PARAMETER	TEST CONDITIONS	MIN	UNIT
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

**ERASE AND PROGRAMMING PERFORMANCE**

PARAMETER	TYP (NOTE1)	MAX (NOTE2)	UNIT	COMMENTS	
Sector Erase Time	0.7	15	s	Excludes 00h programming prior to erasure (Note4)	
Chip Erase Time	25		s		
Byte Programming Time	9	300	us	Excludes system level overhead (Note5)	
Word Programming Time	11	360	us		
Chip Programming Time (Note3)	Byte Mode	18	54		s
	Word Mode	12	36		s

**Notes :**

1. Typical program and erase times assume the following conditions: 25 °C, 3.0V Vcc, 1,000,000 cycles. Additionally programming typical assume checkerboard pattern.
2. Under worst case conditions of 90 °C, Vcc=2.7V, 1,000,000 cycles.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the two-or four-bus-cycle sequence for the program command.  
See table 9 for further information on command definitions.
6. The device has a minimum erase and program cycle endurance of 1,000,000 cycles.

www.DataSheet4U.com

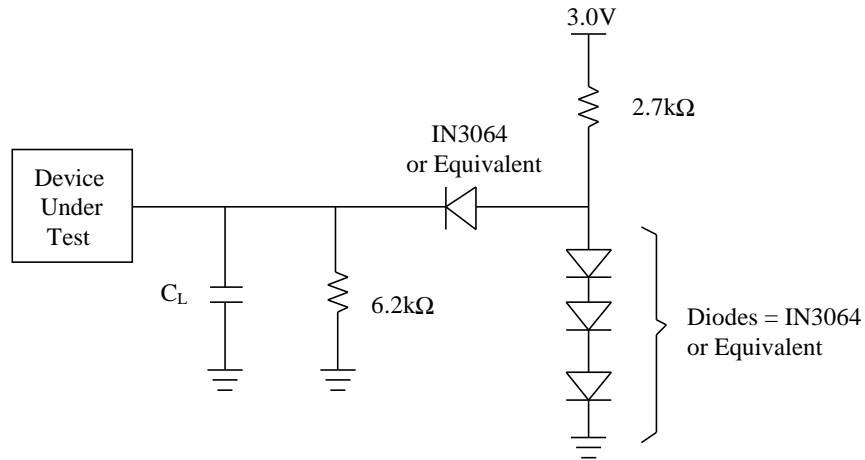
**SOP/TSOP PIN CAPACITANCE**

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	TYP.	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0	6	7.5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0	8.5	12	pF
C <sub>IN2</sub>	Control Pin Capacitance	V <sub>IN</sub> = 0	7.5	9	pF

- Notes :** 1. Sampled, not 100% tested  
2. Test conditions T<sub>A</sub> = 25° C, f=1.0 MHz.

**TEST SPECIFICATIONS**

TEST CONDITION	80R	-90/ -120	UNIT
Output load	1TTL gate		
Output load capacitance, C <sub>L</sub> (Including jig capacitance)	30	100	pF
Input rise and fall times	5		ns
Input pulse levels	0.0 - 3.0		V
Input timing measurement reference levels	1.5		V
Output timing measurement reference levels	1.5		V



Note :  $C_L = 100\text{pF}$  including jig capacitance

### AC CHARACTERISTICS

#### ⌋ Erase / Program Operations

PARAMETER SYMBOLS		DESCRIPTION		-80	-90	UNIT
JEDEC	Standard					
$t_{AVAV}$	$t_{WC}$	Write Cycle Time (Note1)	Min	80	90	ns
$t_{AVWL}$	$t_{AS}$	Address Setup Time	Min	0		ns
$t_{WLAX}$	$t_{AH}$	Address Hold Time	Min	45	45	ns
$t_{DVWH}$	$t_{DS}$	Data Setup Time	Min	35	45	ns
$t_{WHDX}$	$t_{DH}$	Data Hold Time	Min	0		ns
	$t_{OES}$	Output Enable Setup Time	Min	0		ns
$t_{GHWL}$	$t_{GHWL}$	Read Recovery Time Before Write (/OE High to /WE Low)	Min	0		ns
$t_{ELWL}$	$t_{CS}$	/CE Setup Time	Min	0		ns
$t_{WHEH}$	$t_{CH}$	/CE Hold Time	Min	0		ns
$t_{WLWH}$	$t_{WP}$	Write Pulse Width	Min	35	35	ns
$t_{WHWL}$	$t_{WPH}$	Write Pulse Width High	Min	30		ns
$t_{WHWH1}$	$t_{WHWH1}$	Programming Operation (Note2)	Byte	Typ	9	us
			Word	Typ	11	us
$t_{WHWH2}$	$t_{WHWH2}$	Sector Erase Operation (Note2)	Typ	0.7		sec
	$t_{VCS}$	Vcc Setup Time (Note1)	Min	50		us
	$t_{RB}$	Recovery Time from RY//BY	Min	0		ns
	$t_{BUSY}$	Program/ Erase Valid to RY//BY Delay	Min	90		ns

**Note:**

1. Not 100% tested.

2. See the "Erase and Programming Performance" section for more Information

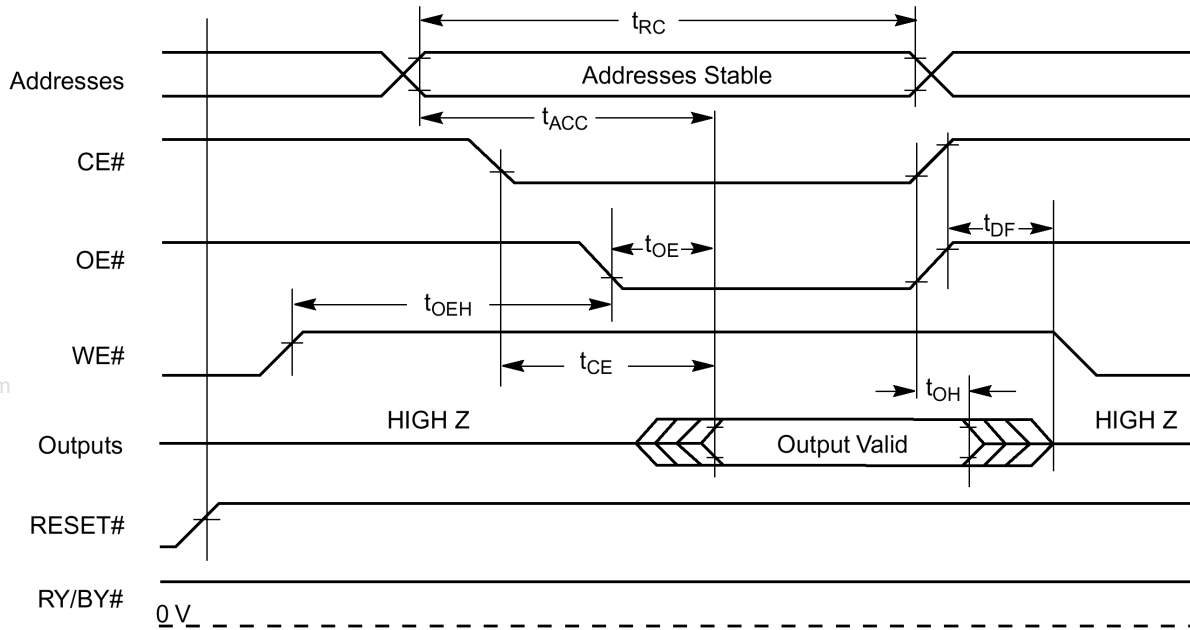
### ⌋ Alternate /CE Controlled Erase/ Program Operations

PARAMETER SYMBOLS		DESCRIPTION		-80	-90	UNIT
JEDEC	Standard					
t <sub>AVAV</sub>	t <sub>WC</sub>	Write Cycle Time (Note1)	Min	80	90	ns
t <sub>AVEL</sub>	t <sub>AS</sub>	Address Setup Time	Min	0		ns
t <sub>ELAX</sub>	t <sub>AH</sub>	Address Hold Time	Min	45	45	ns
t <sub>DVEH</sub>	t <sub>DS</sub>	Data Setup Time	Min	35	45	ns
t <sub>EHDX</sub>	t <sub>DH</sub>	Data Hold Time	Min	0		ns
	t <sub>OES</sub>	Output Enable Setup Time	Min	0		ns
t <sub>GHEL</sub>	t <sub>GHEL</sub>	Read Recovery Time Before Write (/OE High to /WE Low)	Min	0		ns
t <sub>WLEL</sub>	t <sub>WS</sub>	/WE Setup Time	Min	0		ns
t <sub>EHWH</sub>	t <sub>WH</sub>	/WE Hold Time	Min	0		ns
t <sub>ELEH</sub>	t <sub>CP</sub>	/CE Pulse Width	Min	35	35	ns
t <sub>EHEL</sub>	t <sub>CPH</sub>	/CE Pulse Width High	Min	30		ns
t <sub>WHWH1</sub>	t <sub>WHWH1</sub>	Programming	Byte	Min	9	us
		Operation (Note2)	Word	Min	11	us
t <sub>WHWH2</sub>	t <sub>WHWH2</sub>	Sector Erase Operation (Note2)	Min	0.7		

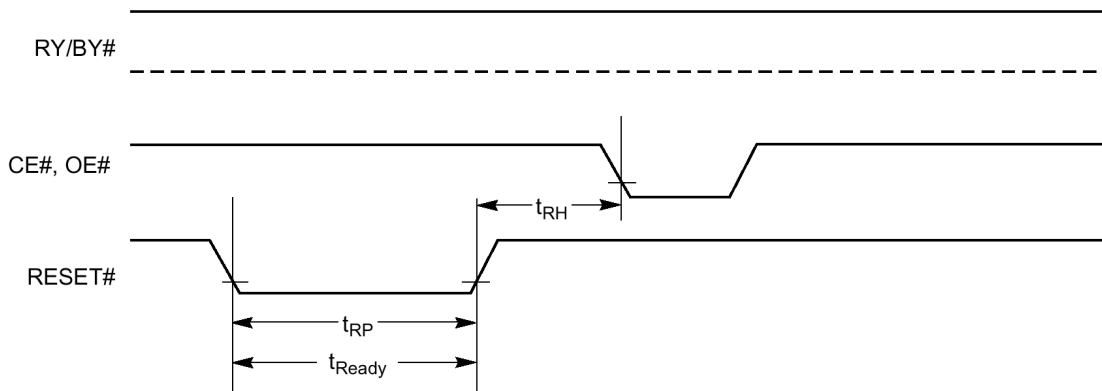
**Note:** 1. Not 100% tested.

2. See the "Erase and Programming Performance" section for more Information.

**U READ OPERATIONS TIMING**

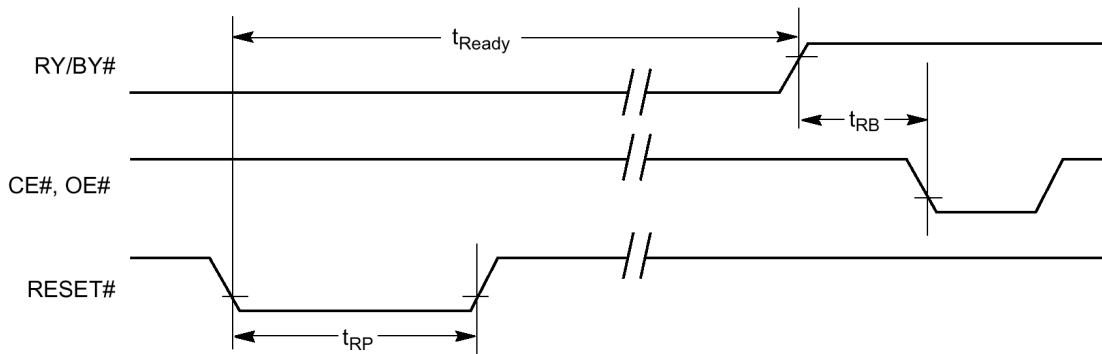


**U RESET TIMING**



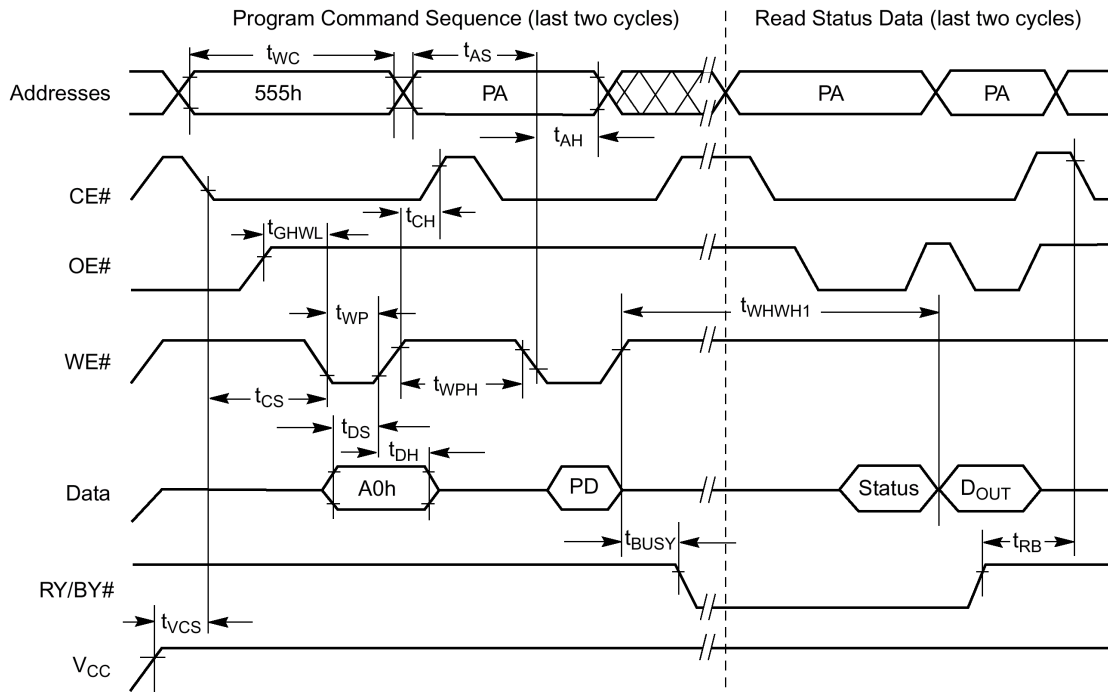
Reset Timings NOT during Embedded Algorithms

Reset Timings during Embedded Algorithms

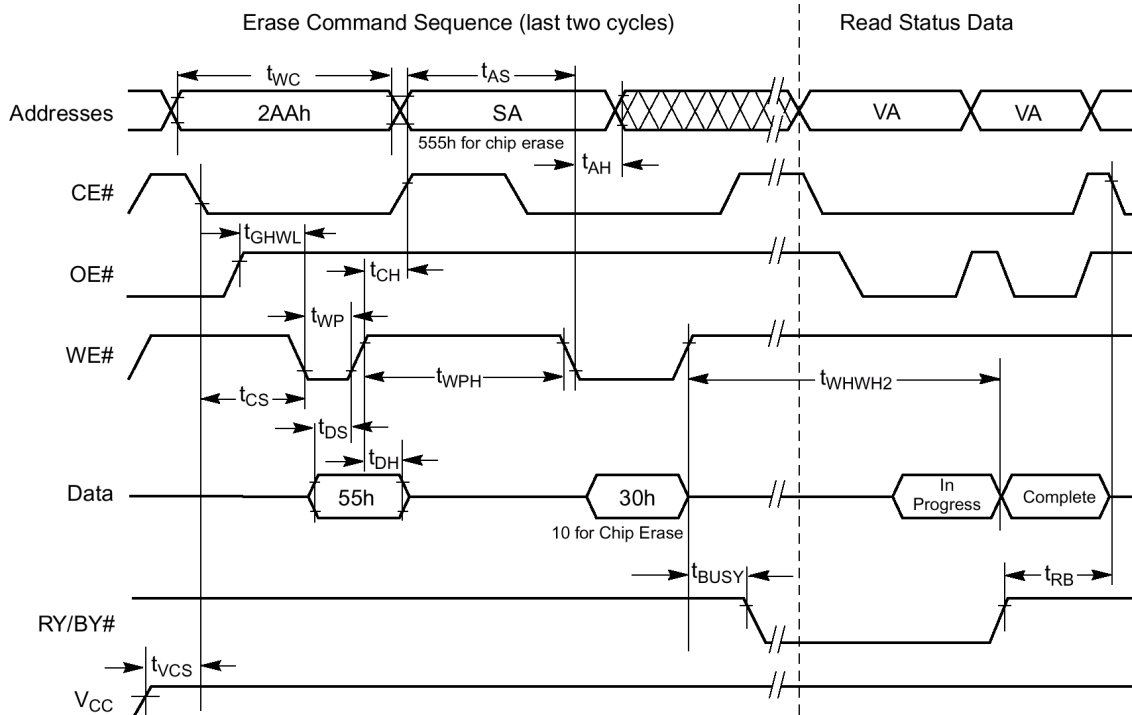




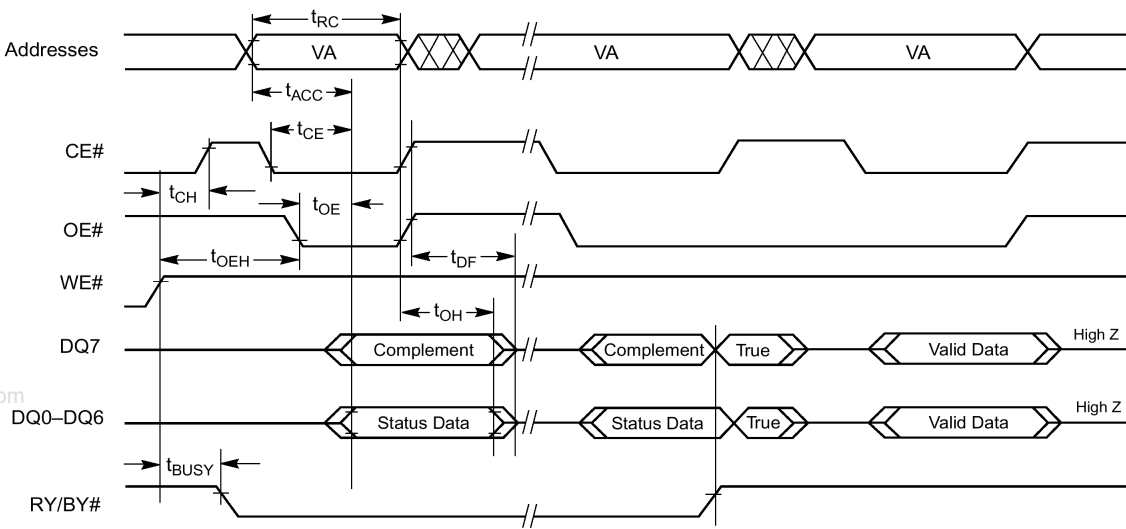
PROGRAM OPERATIONS TIMING



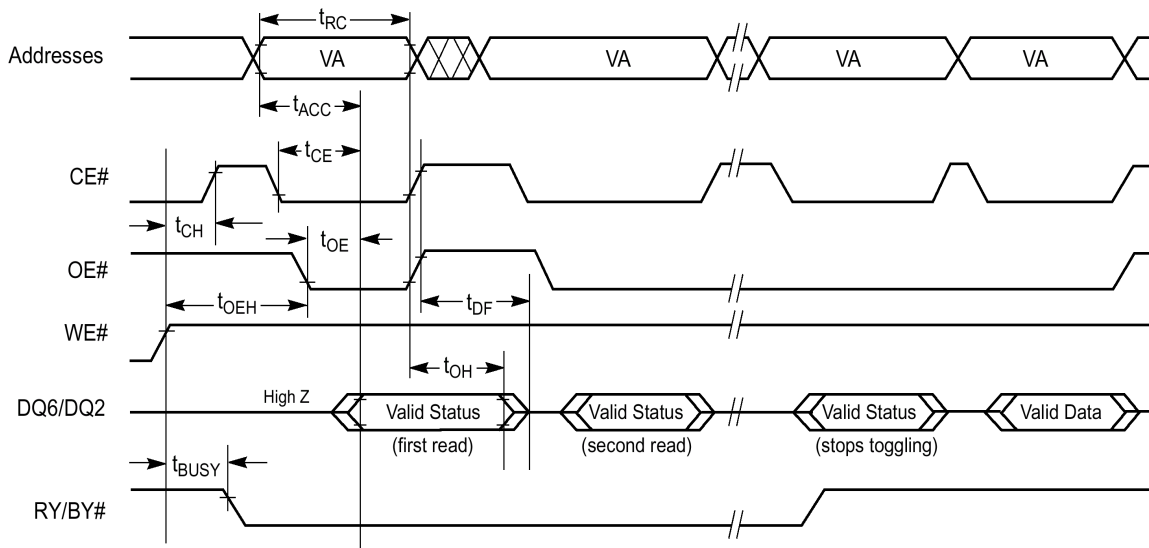
CHIP/SECTOR ERASE OPERATION TIMINGS



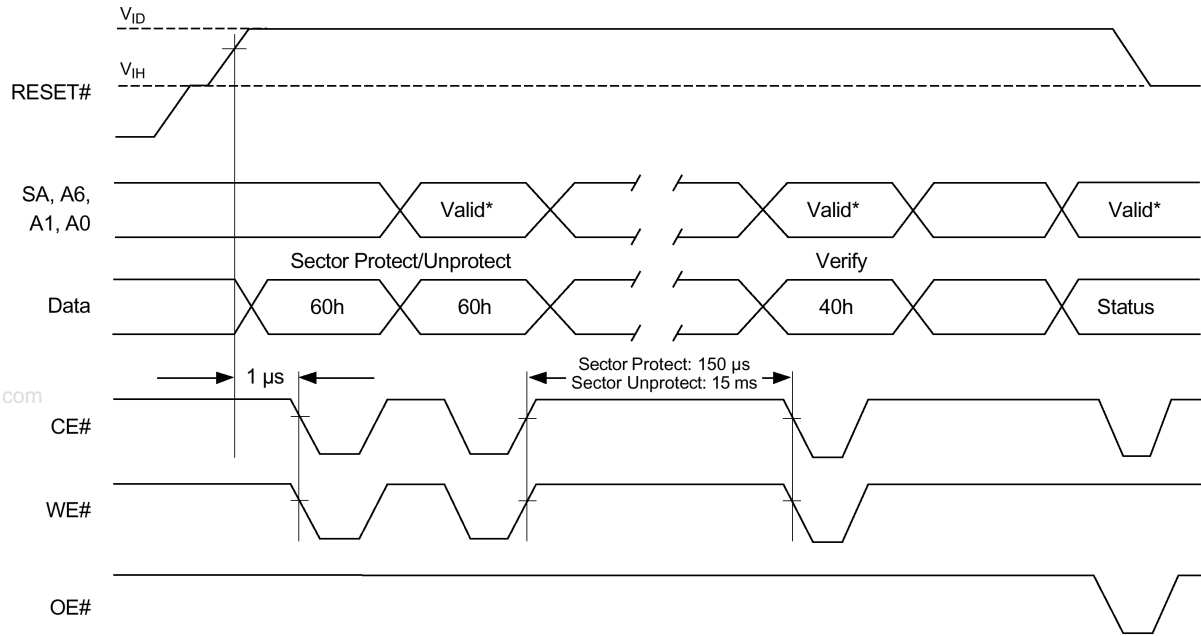
**U DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)**



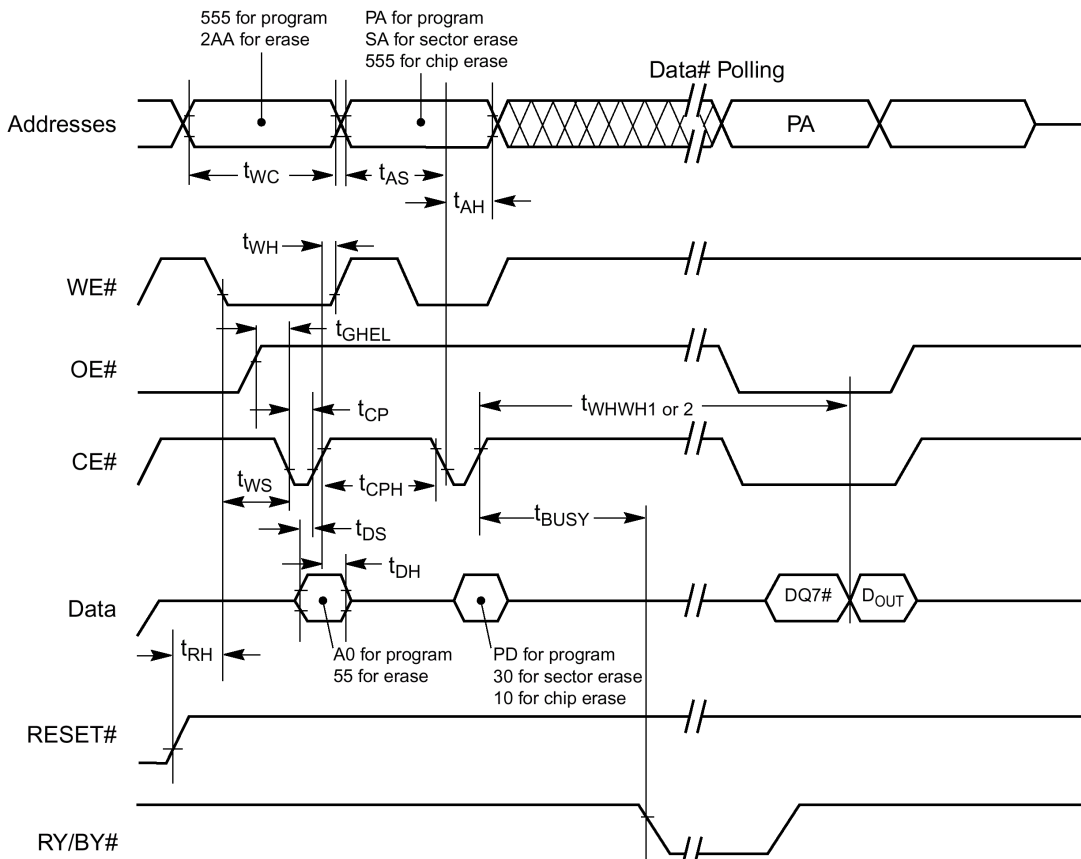
**U TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)**



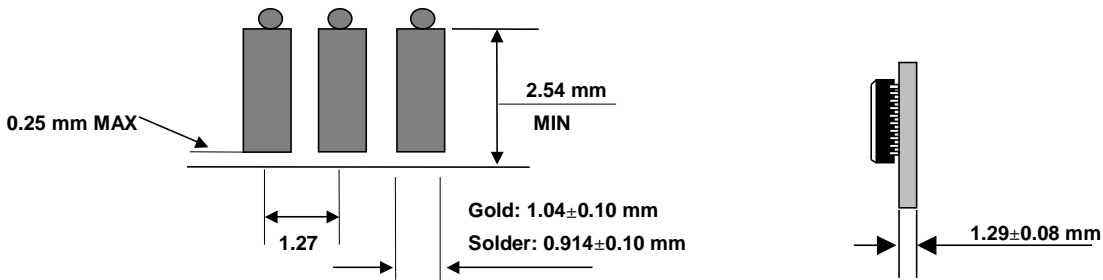
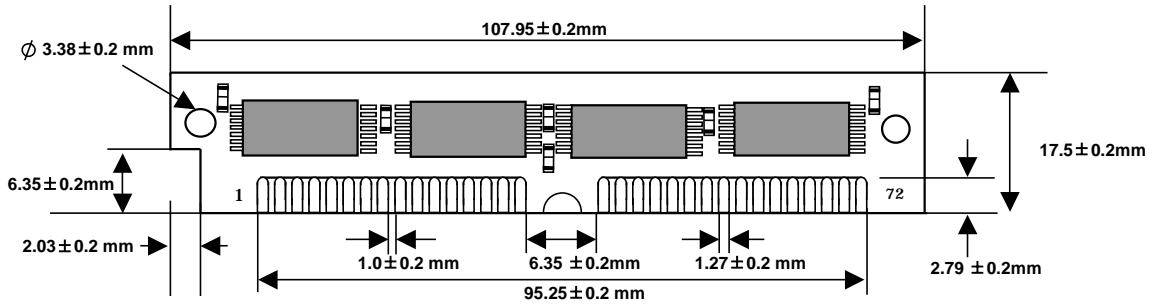
U SECTOR PROTECT UNPROTECT TIMEING DIAGRAM



U ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



PACKAGE DIMENSIONS



(Solder & Gold Plating)

ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	Speed
HMF3M32M6V-70	12MByte	3MX 32bit	72 Pin-SIMM	6EA	3.3V	70ns
HMF3M32M6V-80	12MByte	3MX 32bit	72 Pin-SIMM	6EA	3.3V	80ns
HMF3M32M6V-90	12MByte	3MX 32bit	72 Pin-SIMM	6EA	3.3V	90ns
HMF3M32M6V-120	12MByte	3MX 32bit	72 Pin-SIMM	6EA	3.3V	120ns