



**FLASH-ROM MODULE 8MByte (8M x 8-Bit)**  
**Part No. HMF8M8M4G**

## GENERAL DESCRIPTION

The HMF8M8M4G is a high-speed flash read only memory (FROM) module containing 8,388,608 words organized in a x8bit configuration. The module consists of four 2M x 8 FROM mounted on a 72-pin, single-sided, FR4-printed circuit board. Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0V flash or EPROM devices.

Four chip enable inputs, (/CE1, /CE2, /CE3, /CE4) are used to enable the module's 4 bytes independently. Output enable (/OE) and write enable (/WE) can set the memory input and output.

When FROM module is disable condition the module is becoming power standby mode, system designer can get low-power design. All module components may be powered from a single +5V DC power supply and all inputs and outputs are TTL-compatible.

## FEATURES

w Part identification

- HMF8M8M4 (Solder Plating Lead)
- HMF8M8M4G (Gold Plating Lead)

w Access time : 70, 90, 120ns

w High-density 8MByte design

w High-reliability, low-power design

w Single + 5V  $\pm$  0.5V power supply

w Easy memory expansion

w All inputs and outputs are TTL-compatible

w FR4-PCB design

w Low profile 72-pin SIMM

w Minimum 1,000,000 write/erase cycle

w Flexible sector architecture

w Embedded algorithms

w Erase suspend / Erase resume

## OPTIONS

w Timing

|              |      |
|--------------|------|
| 70ns access  | - 70 |
| 90ns access  | - 90 |
| 120ns access | -120 |

w Packages

|             |   |
|-------------|---|
| 72-pin SIMM | M |
|-------------|---|

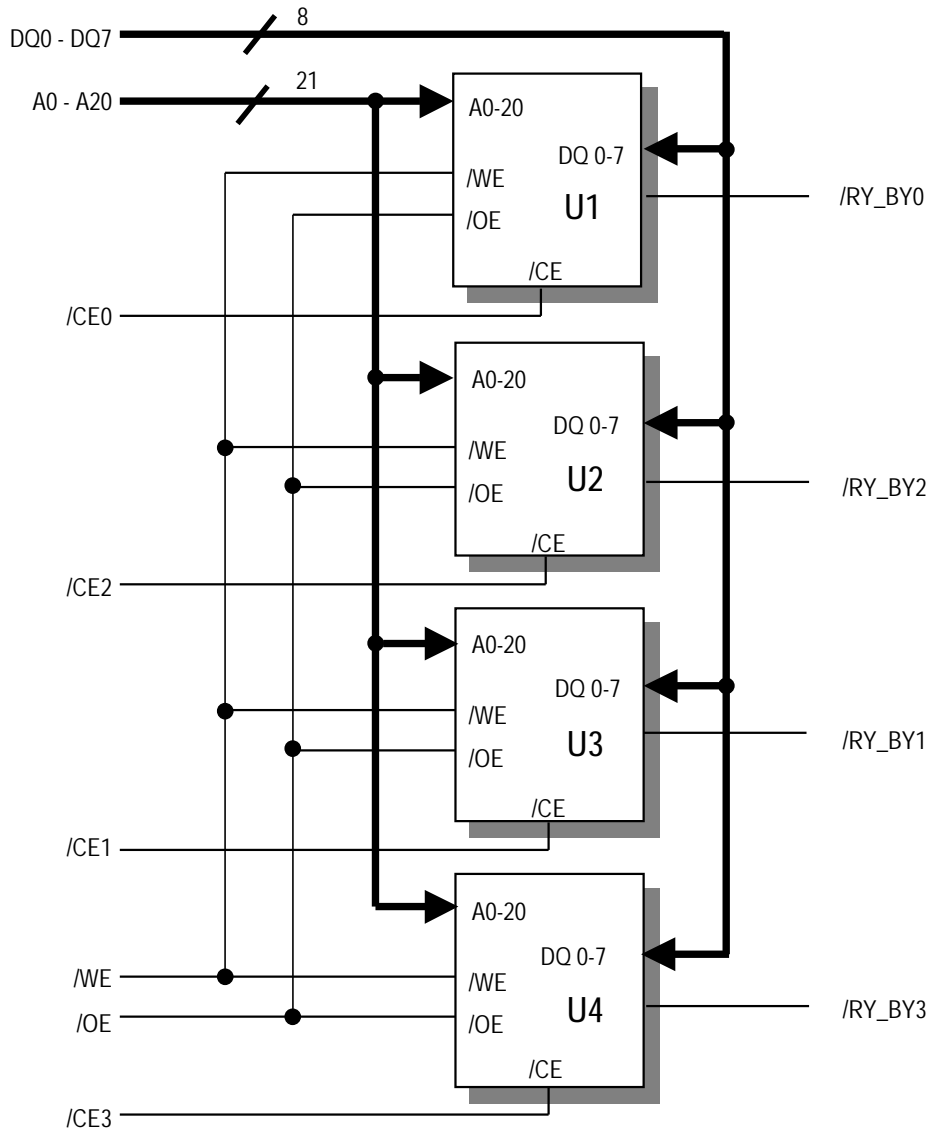
## MARKING

## PIN ASSIGNMENT

| PIN | SYMBOL | PIN | SYMBOL  | PIN | SYMBOL |
|-----|--------|-----|---------|-----|--------|
| 1   | Vss    | 25  | A15     | 49  | NC     |
| 2   | /CE0   | 26  | A16     | 50  | NC     |
| 3   | /CE1   | 27  | A17     | 51  | NC     |
| 4   | /CE2   | 28  | A18     | 52  | NC     |
| 5   | /CE3   | 29  | A19     | 53  | NC     |
| 6   | Vcc    | 30  | Vcc     | 54  | NC     |
| 7   | /WE    | 31  | A20     | 55  | NC     |
| 8   | /OE    | 32  | DQ0     | 56  | NC     |
| 9   | /RESET | 33  | DQ1     | 57  | NC     |
| 10  | A0     | 34  | DQ2     | 58  | NC     |
| 11  | A1     | 35  | DQ3     | 59  | Vcc    |
| 12  | A2     | 36  | DQ4     | 60  | NC     |
| 13  | A3     | 37  | DQ5     | 61  | NC     |
| 14  | A4     | 38  | DQ6     | 62  | NC     |
| 15  | A5     | 39  | Vss     | 63  | Vss    |
| 16  | A6     | 40  | DQ7     | 64  | NC     |
| 17  | A7     | 41  | /RY_BY0 | 65  | NC     |
| 18  | A8     | 42  | /RY_BY1 | 66  | NC     |
| 19  | A9     | 43  | /RY_BY2 | 67  | NC     |
| 20  | A10    | 44  | Vcc     | 68  | NC     |
| 21  | A11    | 45  | /RY_BY3 | 69  | NC     |
| 22  | A12    | 46  | NC      | 70  | NC     |
| 23  | A13    | 47  | NC      | 71  | NC     |
| 24  | A14    | 48  | NC      | 72  | Vss    |

## 72-PIN SIMM TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

| MODE         | /OE | /CE | /WE | DQ     | POWER   |
|--------------|-----|-----|-----|--------|---------|
| STANDBY      | X   | H   | X   | HIGH-Z | STANDBY |
| NOT SELECTED | H   | L   | H   | HIGH-Z | ACTIVE  |
| READ         | L   | L   | H   | Dout   | ACTIVE  |
| WRITE        | X   | L   | L   | Din    | ACTIVE  |

Note : X means don't care

**ABSOLUTE MAXIMUM RATINGS**

| PARAMETER                                      | SYMBOL              | RATING          |
|--|---------------------|-----------------|
| Voltage with respect to ground all other pins  | V <sub>IN,OUT</sub> | -2.0V to +7.0V  |
| Voltage with respect to ground V <sub>cc</sub> | V <sub>CC</sub>     | -2.0V to +7.0V  |
| Storage Temperature                            | T <sub>STG</sub>    | -65°C to +125°C |
| Operating Temperature                          | T <sub>A</sub>      | -55°C to +125°C |
| Power Dissipation                              | P <sub>D</sub>      | 4W              |

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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**RECOMMENDED DC OPERATING CONDITIONS**

| PARAMETER  | SYMBOL          | MIN  | TYP. | MAX  |
|--|-----------------|------|------|------|
| V <sub>cc</sub> for ± 10% device Supply Voltages | V <sub>CC</sub> | 4.5V |      | 5.5V |
| Ground   | V <sub>SS</sub> | 0    | 0    | 0    |

**DC AND OPERATING CHARACTERISTICS (0°C ≤ T<sub>A</sub> ≤ 70 °C ; V<sub>cc</sub> = 5V ± 0.5V )**

| PARAMETER  | TEST CONDITIONS   | SYMBOL           | MIN | MAX  | UNITS |
|--|---|------------------|-----|------|-------|
| Input Leakage Current                                  | V <sub>CC</sub> =V <sub>CC</sub> max, V <sub>IN</sub> = GND to V <sub>CC</sub>  | I <sub>L1</sub>  |     | ±1.0 | μA    |
| Output Leakage Current                                 | V <sub>CC</sub> =V <sub>CC</sub> max, V <sub>OUT</sub> = GND to V <sub>CC</sub> | I <sub>L0</sub>  |     | ±1.0 | μA    |
| Output High Voltage                                    | I <sub>OH</sub> = -2.5mA, V <sub>CC</sub> = V <sub>CC</sub> min                 | V <sub>OH</sub>  | 2.4 |      | V     |
| Output Low Voltage                                     | I <sub>OL</sub> = 12mA, V <sub>CC</sub> =V <sub>CC</sub> min                    | V <sub>OL</sub>  |     | 0.45 | V     |
| V <sub>CC</sub> Active Current for Read(1)             | /CE = V <sub>IL</sub> , /OE=V <sub>IH</sub>                                     | I <sub>CC1</sub> |     | 40   | mA    |
| V <sub>CC</sub> Active Current for Program or Erase(2) | /CE = V <sub>IL</sub> , /OE=V <sub>IH</sub>                                     | I <sub>CC2</sub> |     | 60   | mA    |
| V <sub>CC</sub> Standby Current                        | /CE= V <sub>IH</sub>  | I <sub>CC3</sub> |     | 1.0  | mA    |
| Low V <sub>CC</sub> Lock-Out Voltage                   |   | V <sub>LKO</sub> | 3.2 | 4.2  | V     |

**Notes:**

1. The I<sub>CC</sub> current listed is typically less than 2mA/MHz, with /OE at V<sub>IH</sub>.
2. I<sub>CC</sub> active while embedded algorithm (program or erase) is in progress
3. Maximum I<sub>CC</sub> current specifications are tested with V<sub>CC</sub>=V<sub>CC</sub> max

**ERASE AND PROGRAMMING PERFORMANCE**

| PARAMETER         | LIMITS |      |      | UNIT | COMMENTS                                  |
|-------------------|--------|------|------|------|---|
|                   | MIN.   | TYP. | MAX. |      |   |
| Sector Erase Time | -      | 1    | 8    | sec  | Excludes 00H programming prior to erasure |

|                       |   |      |      |         |                                |
|-----------------------|---|------|------|---------|--------------------------------|
| Byte Programming Time | - | 7    | 300  | $\mu$ s | Excludes system-level overhead |
| Chip Programming Time | - | 14.4 | 43.2 | sec     | Excludes system-level overhead |

## TSOP CAPACITANCE

| PARAMETER SYMBOL | PARAMETER DESCRIPTION   | TEST SETUP           | MIN | MAX | UNIT |
|------------------|-------------------------|----------------------|-----|-----|------|
| C <sub>IN</sub>  | Input Capacitance       | V <sub>IN</sub> = 0  | 6   | 7.5 | pF   |
| C <sub>OUT</sub> | Output Capacitance      | V <sub>OUT</sub> = 0 | 8.5 | 12  | pF   |
| C <sub>IN2</sub> | Control Pin Capacitance | V <sub>IN</sub> = 0  | 7.5 | 9   | pF   |

Notes : Test conditions T<sub>A</sub> = 25° C, f=1.0 MHz.

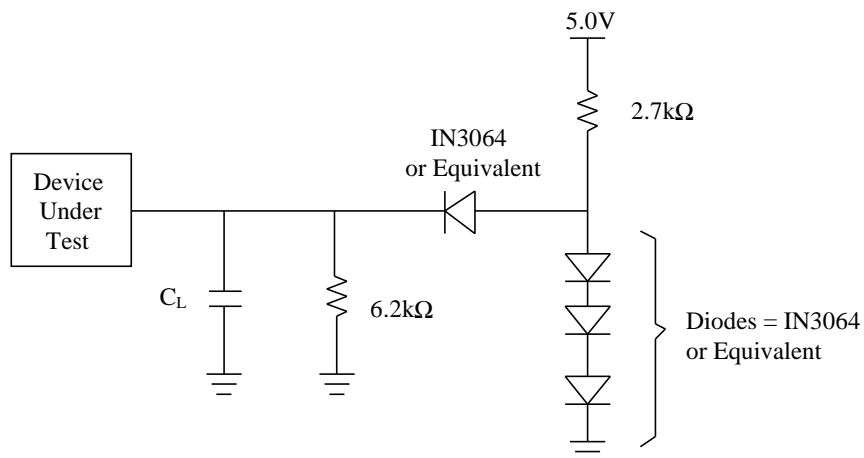
## AC CHARACTERISTICS

### Read Only Operations Characteristics

| PARAMETER SYMBOLS |                  | DESCRIPTION  | TEST SETUP                                     | -75 | -90 | UNIT |    |
|-------------------|------------------|--|--|-----|-----|------|----|
| JEDEC             | STANDARD         |  |  | Min | Max |      |    |
| t <sub>AVAV</sub> | t <sub>RC</sub>  | Read Cycle Time  | Min  | 70  | 90  | ns   |    |
| t <sub>AVQV</sub> | t <sub>ACC</sub> | Address to Output Delay  | /CE = V <sub>IL</sub><br>/OE = V <sub>IL</sub> | Max | 70  | 90   | ns |
| t <sub>ELQV</sub> | t <sub>CE</sub>  | Chip Enable to Output Delay  | /OE = V <sub>IL</sub>                          | Max | 70  | 90   | ns |
| t <sub>GLQV</sub> | t <sub>OE</sub>  | Chip Enable to Output Delay  |  | Max | 40  | 40   | ns |
| t <sub>EHQZ</sub> | t <sub>DF</sub>  | Chip Enable to Output High-Z   |  | Max | 20  | 20   | ns |
| t <sub>GHQZ</sub> | t <sub>DF</sub>  | Output Enable to Output High-Z   |  | Max | 20  | 20   | ns |
| t <sub>AXQX</sub> | t <sub>QH</sub>  | Output Hold Time From Addresses,<br>/CE or /OE, Whichever Occurs First |  | Min | 0   | 0    | ns |

## TEST SPECIFICATIONS

| TEST CONDITION   | ALL SPEED OPTIONS | UNIT |
|--|-------------------|------|
| Output load  | 1TTL gate         |      |
| Output load capacitance,<br>C <sub>L</sub> (Including jig capacitance) | 100               | pF   |
| Input rise and full times  | 20                | ns   |
| Input pulse levels   | 0.45-2.4          | V    |
| Input timing measurement reference levels                              | 0.8               | V    |
| Output timing measurement reference levels                             | 2.0               | V    |



Note :  $C_L = 100\text{pF}$  including jig capacitance

### u Erase/Program Operations

| PARAMETER SYMBOLS |             | DESCRIPTION                    |     | -75 | -90 | UNIT          |
|-------------------|-------------|--------------------------------|-----|-----|-----|---------------|
| JEDEC             | STANDARD    |                                |     |     |     |               |
| $t_{AVAV}$        | $t_{WC}$    | Write Cycle Time               | Min | 70  | 90  | ns            |
| $t_{AVWL}$        | $t_{AS}$    | Address Setup Time             | Min | 0   | 0   | ns            |
| $t_{WLAX}$        | $t_{AH}$    | Address Hold Time              | Min | 40  | 45  | ns            |
| $t_{DVWH}$        | $t_{DS}$    | Data Setup Time                | Min | 40  | 45  | ns            |
| $t_{WHDX}$        | $t_{DH}$    | Data Hold Time                 | Min | 0   | 0   | ns            |
|                   | $t_{OES}$   | Output Enable Setup Time       | Min | 0   | 0   | ns            |
| $t_{GHWL}$        | $t_{GHWL}$  | Read Recover Time Before Write | Min | 0   | 0   | ns            |
| $t_{ELWL}$        | $t_{CS}$    | /CE Setup Time                 | Min | 0   | 0   | ns            |
| $t_{WHEH}$        | $t_{CH}$    | /CE Hold Time                  | Min | 0   | 0   | ns            |
| $t_{WLWH}$        | $t_{WP}$    | Write Pulse Width              | Min | 40  | 45  | ns            |
| $t_{WHWL}$        | $t_{WPH}$   | Write Pulse Width High         | Min | 20  | 20  | ns            |
| $t_{WHWH1}$       | $t_{WHWH1}$ | Byte Programming Operation     | Typ | 7   | 7   | $\mu\text{s}$ |
| $t_{WHWH2}$       | $t_{WHWH2}$ | Sector Erase Operation (Note1) | Typ | 1   | 1   | sec           |
|                   | $t_{VCS}$   | Vcc set up time                | Min | 50  | 50  | $\mu\text{s}$ |

#### Notes :

1. This does not include the preprogramming time
2. This timing is only for Sector Protect operations

## U Erase/Program Operations

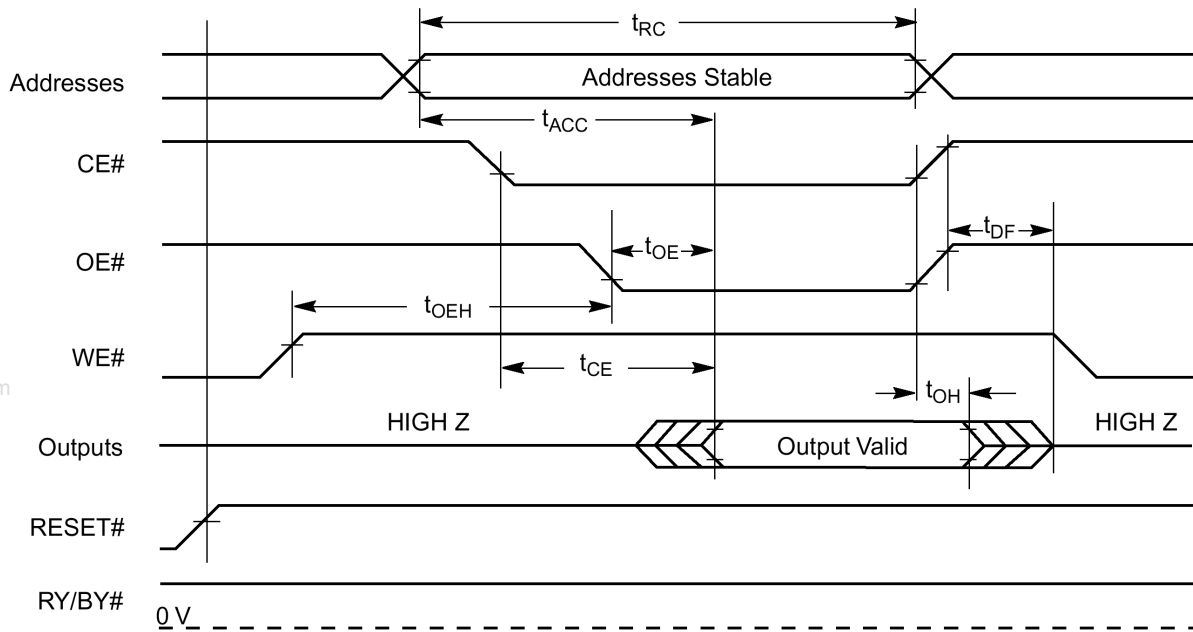
### Alternate /CE Controlled Writes

| PARAMETER SYMBOLS  |                    | DESCRIPTION                    |     | -75 | -90 | UNIT |
|--------------------|--------------------|--------------------------------|-----|-----|-----|------|
| JEDEC              | STANDARD           |                                |     |     |     |      |
| t <sub>AVAV</sub>  | t <sub>WC</sub>    | Write Cycle Time               | Min | 70  | 90  | ns   |
| t <sub>AVWL</sub>  | t <sub>AS</sub>    | Address Setup Time             | Min | 0   | 0   | ns   |
| t <sub>WLAX</sub>  | t <sub>AH</sub>    | Address Hold Time              | Min | 40  | 45  | ns   |
| t <sub>DVWH</sub>  | t <sub>DS</sub>    | Data Setup Time                | Min | 40  | 45  | ns   |
| t <sub>WHDX</sub>  | t <sub>DH</sub>    | Data Hold Time                 | Min | 0   | 0   | ns   |
|                    | t <sub>OES</sub>   | Output Enable Setup Time       | Min | 0   | 0   | ns   |
| t <sub>GHWL</sub>  | t <sub>GHWL</sub>  | Read Recover Time Before Write | Min | 0   | 0   | ns   |
| t <sub>ELWL</sub>  | t <sub>CS</sub>    | /CE Setup Time                 | Min | 0   | 0   | ns   |
| t <sub>WHEH</sub>  | t <sub>CH</sub>    | /CE Hold Time                  | Min | 0   | 0   | ns   |
| t <sub>WLWH</sub>  | t <sub>WP</sub>    | Write Pulse Width              | Min | 40  | 45  | ns   |
| t <sub>WHWL</sub>  | t <sub>WPH</sub>   | Write Pulse Width High         | Min | 20  | 20  | ns   |
| t <sub>WHWH1</sub> | t <sub>WHWH1</sub> | Byte Programming Operation     | Typ | 7   | 7   | μs   |
| t <sub>WHWH2</sub> | t <sub>WHWH2</sub> | Sector Erase Operation (Note1) | Typ | 1   | 1   | sec  |

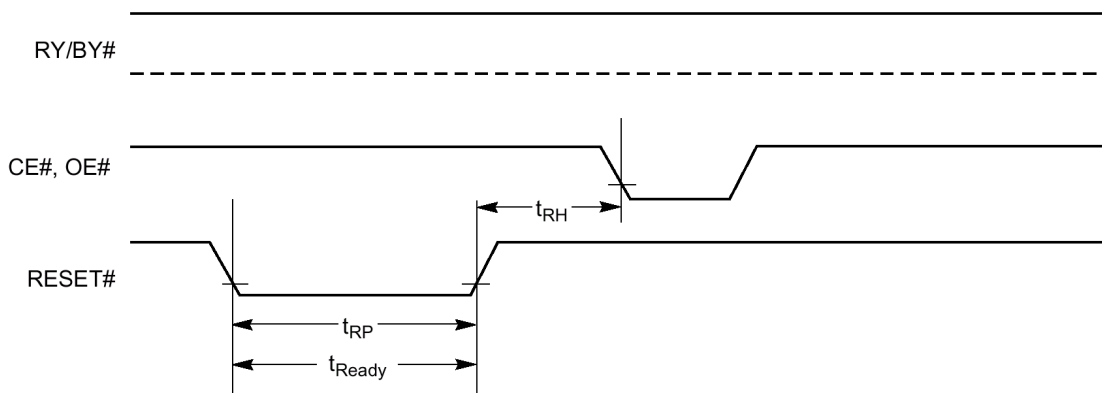
#### Notes :

1. This does not include the preprogramming time
2. This timing is only for Sector Protect operations

U READ OPERATIONS TIMING

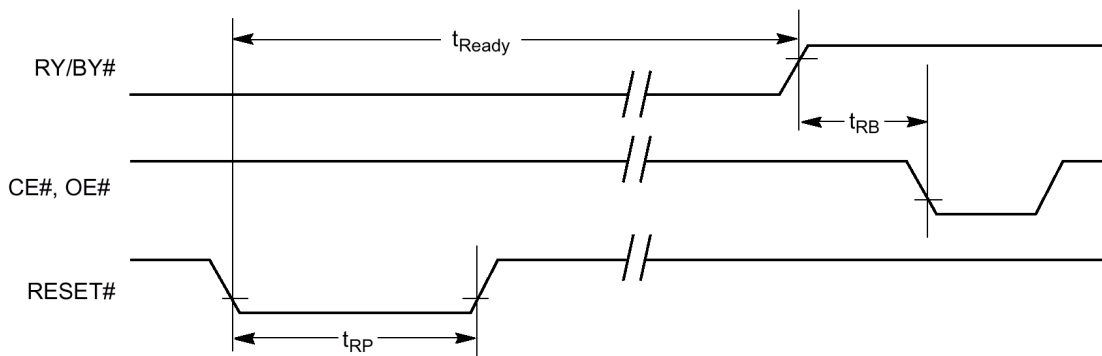


U RESET TIMING

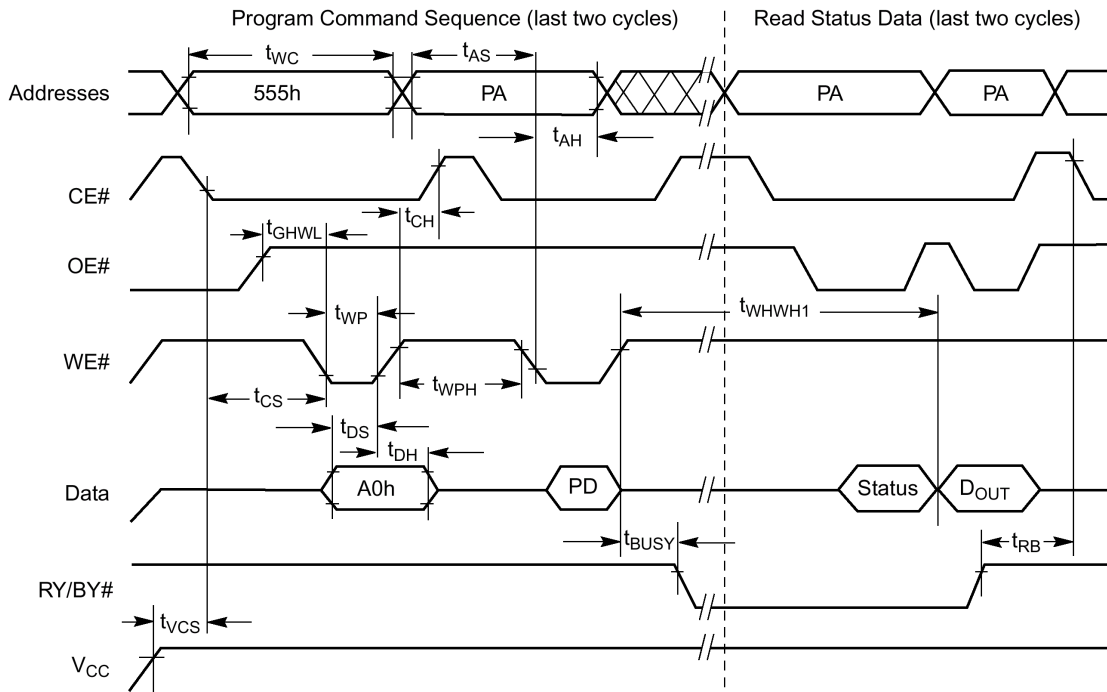


Reset Timings NOT during Embedded Algorithms

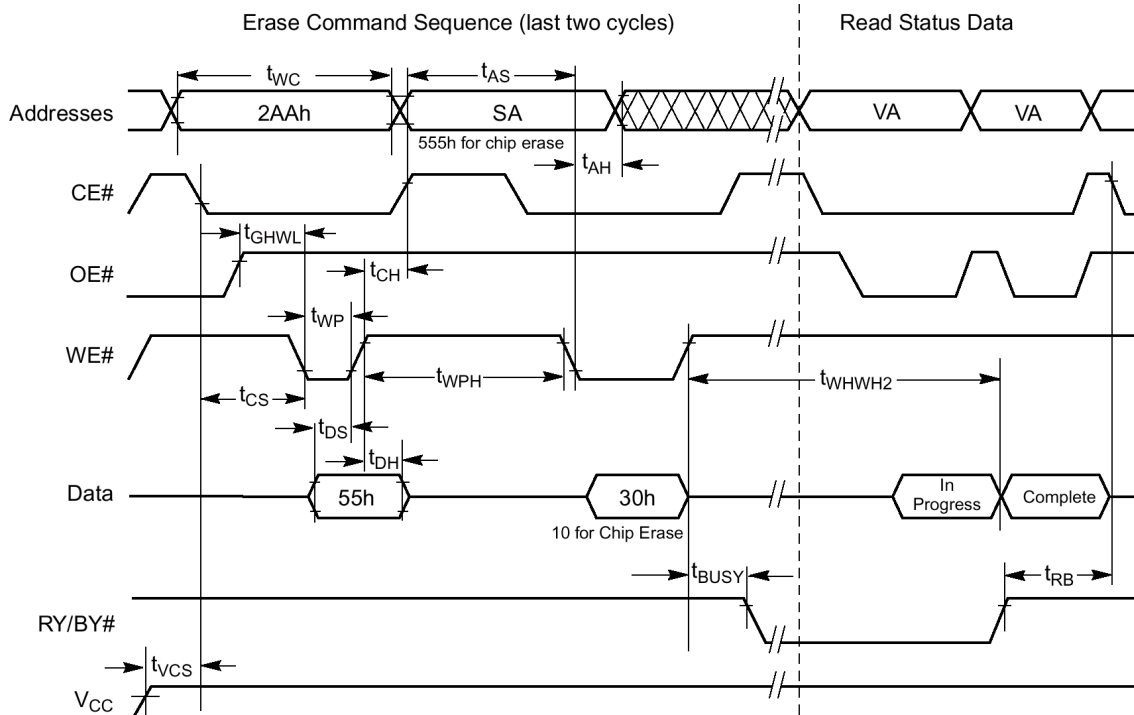
Reset Timings during Embedded Algorithms



PROGRAM OPERATIONS TIMING

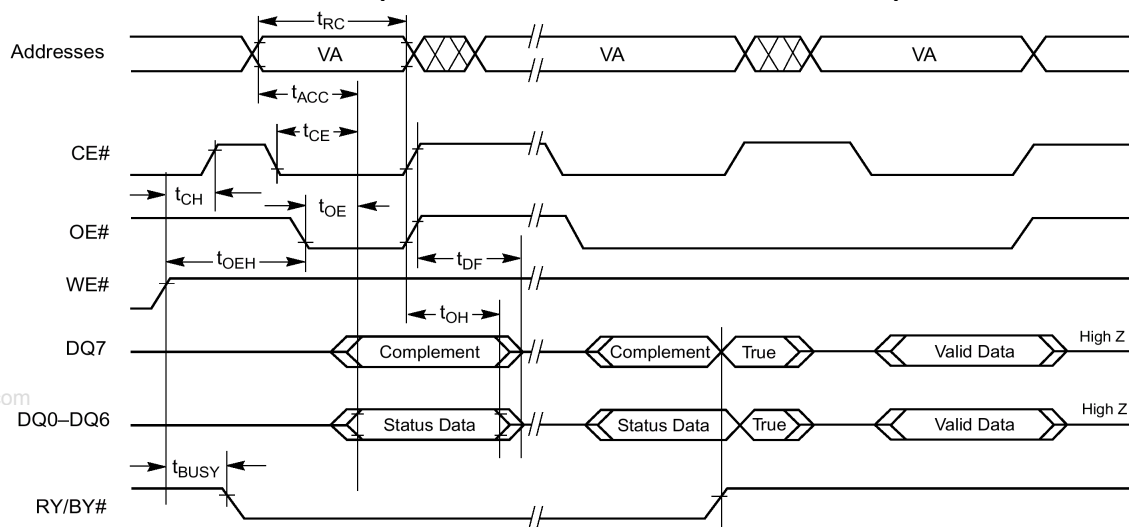


CHIP/SECTOR ERASE OPERATION TIMINGS

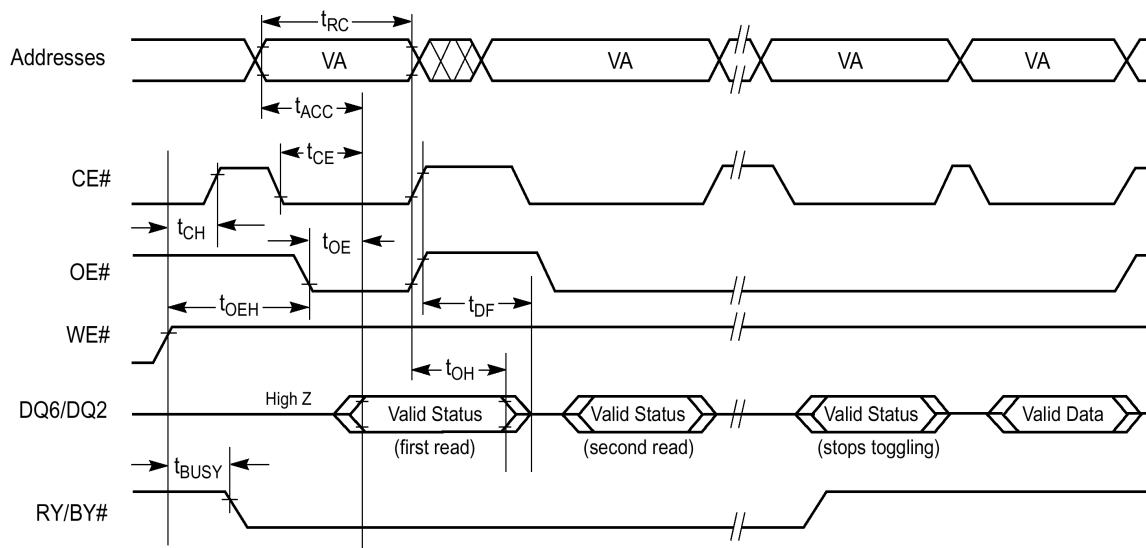




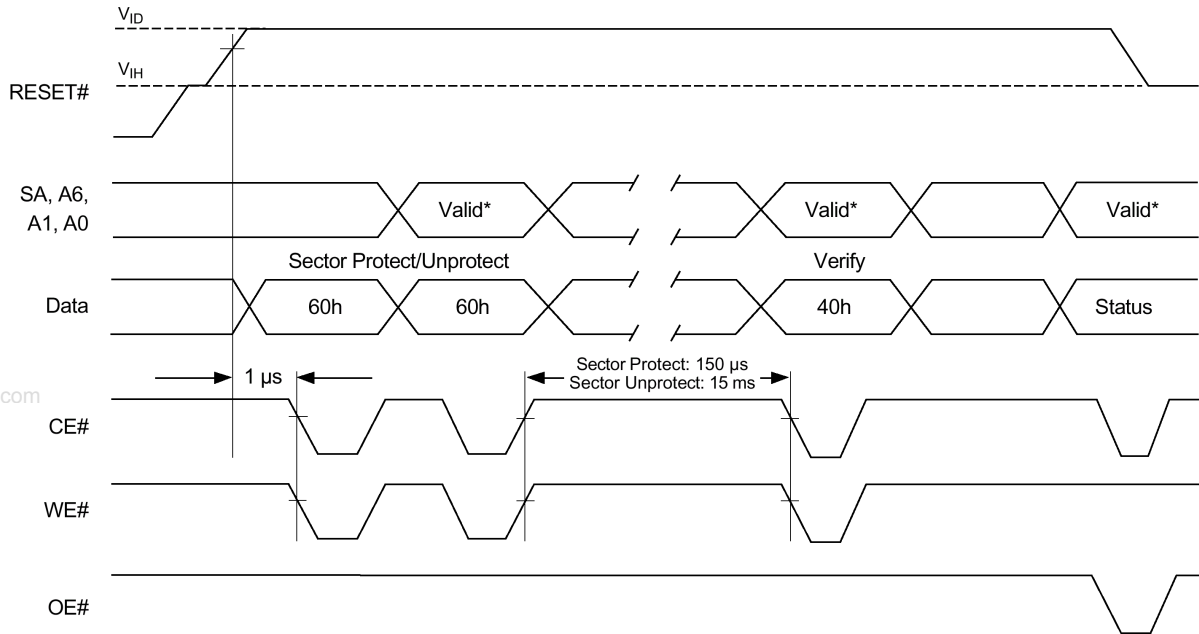
**U DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)**



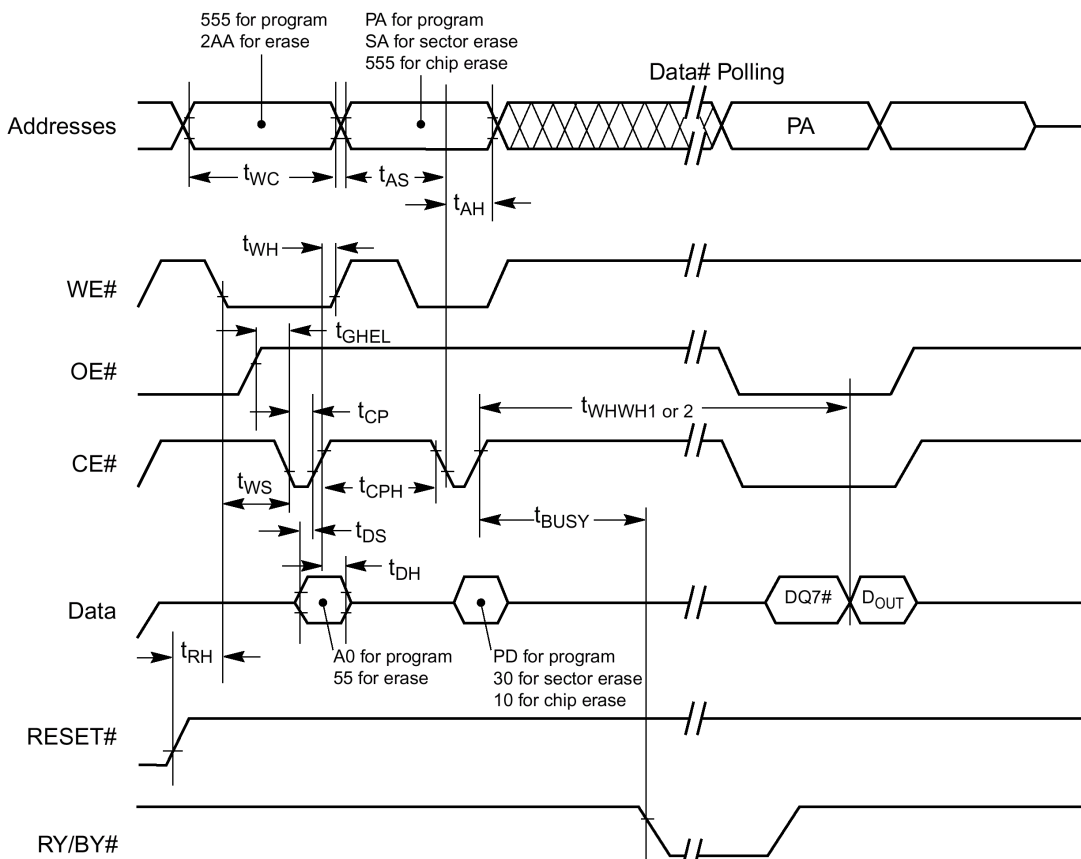
**U TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)**



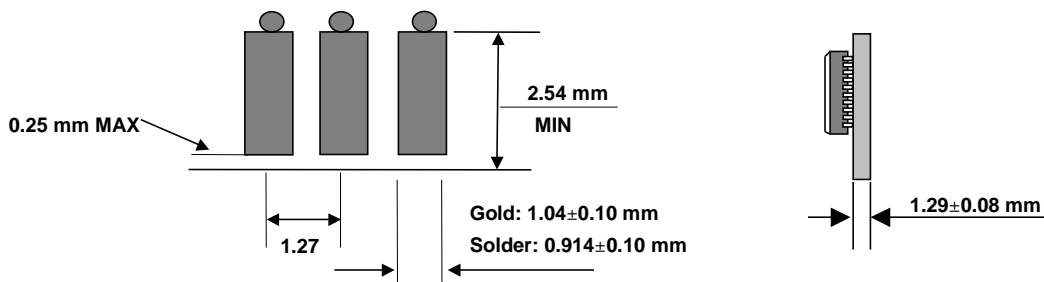
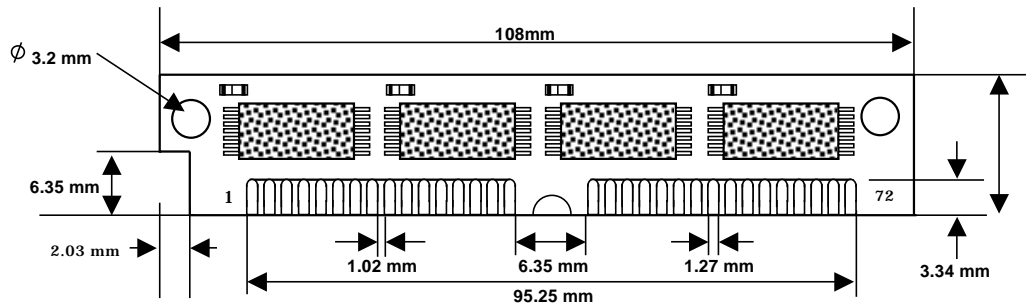
U SECTOR PROTECT UNPROTECT TIMEING DIAGRAM



U ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



PACKAGE DIMENSIONS



(Solder & Gold Plating)

ORDERING INFORMATION

| Part Number   | Density | Org.      | Package     | Component Number | Vcc | SPEED |
|---------------|---------|-----------|-------------|------------------|-----|-------|
| HMF8M8M4G-70  | 8MByte  | 8M X 8bit | 72 Pin-SIMM | 4EA              | 5V  | 70ns  |
| HMF8M8M4G-90  | 8MByte  | 8M X 8bit | 72 Pin-SIMM | 4EA              | 5V  | 90ns  |
| HMF8M8M4G-120 | 8MByte  | 8M X 8bit | 72 Pin-SIMM | 4EA              | 5V  | 120ns |