**Non-Volatile SRAM MODULE 2Mbit (128K x 16-Bit), 40pin-Dip, 5V**
**Part No. HMN12816D**

## GENERAL DESCRIPTION

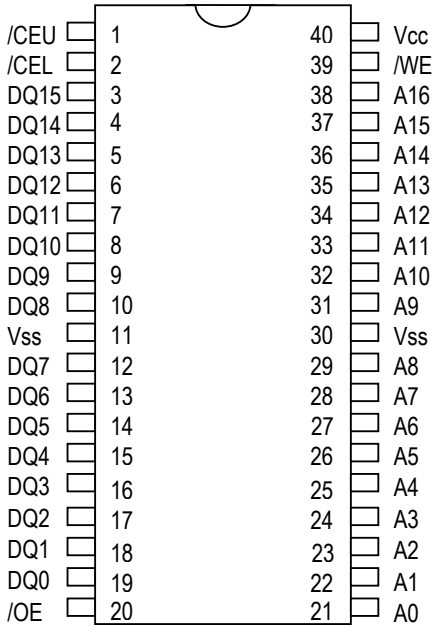
The HMN12816D 128K x 16 nonvolatile SRAM's are 2,097,152-bit fully static, nonvolatile SRAM's, organized as 131,072 words by 16 bits. Each NVSRAM has a self contained lithium energy source and control circuitry which constantly monitors Vcc for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. DIP-package HMN12816D devices can be used in place of solutions which build nonvolatile 128Kx16 memory by utilizing a variety of discrete components. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

The HMN12816D uses extremely low standby current CMOS SRAM's, coupled with small lithium coin cells to provide non-volatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

## FEATURES

- Access time : 70, 85, 120, 150ns
- High-density design : 256KByte Design
- Battery internally isolated until power is applied
- Industry-standard 40-pin 128K x 16 pinout
- Unlimited write cycles
- Data retention in the absence of $V_{CC}$
- 10-years minimum data retention in absence of power
- Automatic write-protection during power-up/power-down cycles
- Data is automatically protected during power loss
- Conventional SRAM operation; unlimited write cycles

## PIN ASSIGNMENT




40-pin Encapsulated Package

## OPTIONS MARKING

- Timing

| | |
|---|---|
| 70 ns | - 70 |
| 85 ns | - 85 |
| 120 ns | -120 |
| 150 ns | -150 |

## FUNCTIONAL DESCRIPTION

The HMN12816D devices execute a read cycle whenever /WE (Write Enable) is inactive (high) and either/both of /CEU or /CEL (Chip Enables) are active (low) and /OE (Output Enable) is active (low). The unique address specified by the 17 address inputs (A0-A16) defines which of the 131,072 words of data is accessed. The status of /CEU and /CEL determines whether all or part of the addressed word is accessed. If /CEU is active with /CEL inactive, then only the upper byte of the addressed word is accessed. If /CEU is inactive with /CEL active, then only the lower byte of the addressed word is accessed. If both the /CEU and /CEL inputs are active (low), then the entire 16-bit word is accessed. Valid data will be available to the 16 data output drivers within $t_{ACC}$ (Access Time) after the last address input signal is stable, providing that /CEU, /CEL and /OE access times are also satisfied. If /CEU, /CEL, and /OE access times are not satisfied, then data access must be measured from the later occurring signal, and the limiting parameter is either $t_{CO}$ for /CEU, /CEL, or $t_{OE}$ for /OE rather than address access.

The HMN12816D devices execute a write cycle whenever /WE and either/both of /CEU or /CEL are active (low) after address inputs are stable. The unique address specified by the 17 address inputs (A0-A16) defines which of the 131,072 words of data is accessed. The status of /CEU and /CEL determines whether all or part of the addressed word is accessed. If /CEU is active with /CEL inactive, then only the upper byte of the addressed word is accessed. If /CEU is inactive with /CEL active, then only the lower byte of the addressed word is accessed. If both the /CEU and /CEL inputs are active (low), then the entire 16-bit word is accessed. The write cycle is terminated by the earlier rising edge of /CEU and/or /CEL, or WE. All address inputs must be kept valid throughout the write cycle. /WE must return to the high state for a minimum recovery time ($t_{WR}$ ) before another cycle can be initiated. The /OE control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled (/CEU and/or /CEL, and /OE active) then /WE will disable the outputs in $t_{ODW}$ from its falling edge.

## PIN DESCRIPTION

$A_0$-$A_{16}$ : Address Inputs

/CEU : Chip enable upper byte

/CEL : Chip enable lower byte

$DQ_0$-$DQ_{15}$ : Data input / Data output

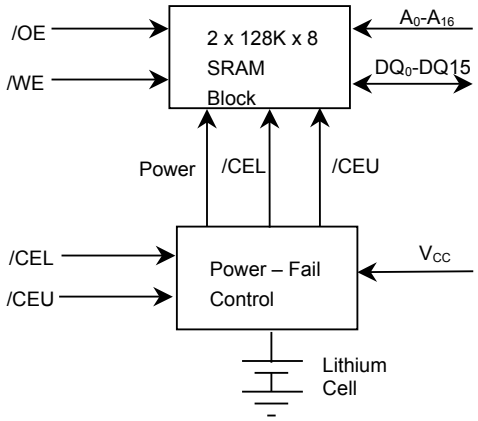
/WE : Write enable

/OE : Output enable

$V_{CC}$ : +5V power supply

$V_{ss}$ : Ground

## BLOCK DIAGRAM



## READ/WRITE FUNCTION

| /OE | /WE | /CEL | /CEU | VCC CURRENT | DQ0-DQ7 | DQ8-DQ15 | CYCLE PERFORMED |
|---|---|---|---|---|---|---|---|
| H | H | X | X | $I_{CCO}$ | High-Z | High-Z | Output Disabled |
| L | H | L | L | $I_{CCO}$ | Output | Output | Read Cycle |
| L | H | L | H | | Output | High-Z | |
| L | H | H | L | | High-Z | Output | |
| X | L | L | L | $I_{CCO}$ | Input | Input | Write Cycle |
| X | L | L | H | | Input | High-Z | |
| X | L | H | L | | High-Z | Input | |
| X | X | H | H | $I_{CCS}$ | High-Z | High-Z | Output Disabled |

## DATA RETENTION MODE

The HMN12816D provides full functional capability for $V_{CC}$ greater than 4.5 volts and write protects by 4.25volts. Data is maintained in the absence of $V_{CC}$ without any additional support circuitry. The nonvolatile static RAMs constantly monitor $V_{CC}$. Should the supply volt-age decay, the NV SRAM's automatically write protect themselves, all inputs become "don't care," and all out-puts become high impedance. As $V_{CC}$ falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when $V_{CC}$ rises above approximately 3.0 volts, the power switching circuit connects external $V_{CC}$ to RAM and disconnects the lithium energy source.

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING | CONDITIONS |
|---|---|---|---|
| DC voltage applied on $V_{CC}$ relative to $V_{SS}$ | $V_{CC}$ | -0.3V to 7.0V | |
| DC Voltage applied on any pin excluding $V_{CC}$ relative to $V_{SS}$ | $V_T$ | -0.3V to 7.0V | $V_T \leq V_{CC}$+0.3 |
| Operating temperature | $T_{OPR}$ | 0 to 70°C | |
| Storage temperature | $T_{STG}$ | -40°C to 70°C | |
| Temperature under bias | $T_{BIAS}$ | -10°C to 70°C | |
| Soldering temperature | $T_{SOLDER}$ | 260°C | For 10 second |

**NOTE:** Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

## RECOMMENDED DC OPERATING CONDITIONS ( $T_A = T_{OPR}$ )

| PARAMETER | SYMBOL | MIN | TYPICAL | MAX |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5V | 5.0V | 5.5V |
| Ground | $V_{SS}$ | 0 | 0 | 0 |
| Input high voltage | $V_{IH}$ | 2.2 | - | Vcc+0.3V |
| Input low voltage | $V_{IL}$ | -0.3 | - | 0.8V |

**NOTE:** Typical values indicate operation at $T_A$ = 25℃

## DC ELECTRICAL CHARACTERISTICS ($T_A$= 0$^{O}$C to 70 $^{O}$C )

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | -2.0 | - | +2.0 | μA |
| I/O Leakage Current CE ≥$V_{IH}$≤$V_{CC}$ | $I_{IO}$ | -1.0 | - | +1.0 | μA |
| Output Current @ 2.4V | $I_{OH}$ | -1.0 | - | - | mA |
| Output Current @0.4V | $I_{OL}$ | 2.0 | - | - | mA |
| Standby Current /CEU,/CEL=2.2V | $I_{CCS1}$ | - | 10 | 20 | mA |
| Standby Current /CEU,/CEL=Vcc-0.5V | $I_{CCS2}$ | - | 6 | 10 | mA |
| Operating Current | $I_{CCO1}$ | - | | 170 | mA |

## CAPACITANCE ($T_A$=25℃, f=1MHz, $V_{CC}$=5.0V)

| DESCRIPTION | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | 20 | 25 | pF |
| Input/Output Capacitance | $C_{I/O}$ | | 5 | 10 | pF |

## READ CYCLE ($T_A$= $T_{OPR}$, $V_{CCmin}$ ≤ $V_{CC}$≤ $V_{CCmax}$ )

| PARAMETER | SYMBOL | CONDITIONS | -70 | | -85 | | -120 | | -150 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| Read Cycle Time | $t_{RC}$ | | 70 | - | 85 | - | 120 | - | 150 | - | ns |
| Address Access Time | $t_{ACC}$ | Output load A | - | 70 | - | 85 | - | 120 | - | 150 | ns |
| Chip enable access time | $t_{ACE}$ | Output load A | - | 70 | - | 85 | - | 120 | - | 150 | ns |
| Output enable to Output valid | $t_{OE}$ | Output load A | - | 35 | - | 45 | - | 60 | - | 70 | ns |
| Chip enable to output in low Z | $t_{CLZ}$ | Output load B | 5 | - | 5 | - | 5 | - | 10 | - | ns |
| Output enable to output in low Z | $t_{OLZ}$ | Output load B | 5 | - | 0 | - | 0 | - | 5 | - | ns |
| Chip disable to output in high Z | $t_{CHZ}$ | Output load B | 0 | 25 | 0 | 35 | 0 | 45 | 0 | 60 | ns |
| Output disable to output high Z | $t_{OHZ}$ | Output load B | 0 | 25 | 0 | 25 | 0 | 35 | 0 | 50 | ns |
| Output hold from address change | $t_{OH}$ | Output load A | 10 | - | 10 | - | 10 | - | 10 | - | ns |

## WRITE CYCLE ($T_A$= $T_{OPR}$, $V_{ccmin}$ ≤ $V_{cc}$ ≤ $V_{ccmax}$ )

| PARAMETER | SYMBOL | CONDITIONS | -70 | | -85 | | -120 | | -150 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | Min | Max | |
| Write Cycle Time | $t_{WC}$ | | 70 | - | 85 | - | 120 | - | 150 | - | ns |
| Chip enable to end of write | $t_{CW}$ | Note 1 | 65 | - | 75 | - | 100 | - | 100 | - | ns |
| Address setup time | $t_{AS}$ | Note 2 | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Address valid to end of write | $t_{AW}$ | Note 1 | 65 | - | 75 | - | 100 | - | 90 | - | ns |
| Write pulse width | $t_{WP}$ | Note 1 | 55 | - | 65 | - | 85 | - | 90 | - | ns |
| Write recovery time (write cycle 1) | $t_{WR1}$ | Note 3 | 5 | - | 5 | - | 5 | - | 5 | - | ns |
| Write recovery time (write cycle 2) | $t_{WR2}$ | Note 3 | 15 | - | 15 | - | 15 | - | 15 | - | ns |
| Data valid to end of write | $t_{DW}$ | | 30 | - | 35 | - | 45 | - | 50 | - | ns |
| Data hold time (write cycle 1) | $t_{DH1}$ | Note 4 | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| Data hold time (write cycle 2) | $t_{DH2}$ | Note 4 | 10 | - | 10 | - | 10 | - | 0 | - | ns |
| Write enabled to output in high Z | $t_{WZ}$ | Note 5 | 0 | 25 | 0 | 30 | 0 | 40 | 0 | 50 | ns |
| Output active from end of write | $t_{OW}$ | Note 5 | 5 | - | 0 | - | 0 | - | 5 | - | ns |

**NOTE:** 1. A write ends at the earlier transition of /CE going high and /WE going high.

2. A write occurs during the overlap of allow /CE and a low /WE. A write begins at the later transition of /CE going low and /WE going low.

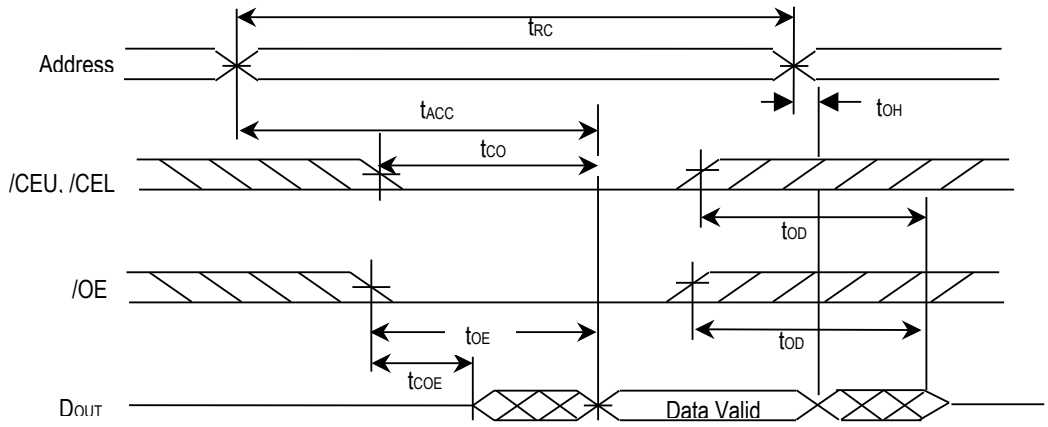
3. Either $t_{WR1}$ or $t_{WR2}$ must be met.

4. Either $t_{DH1}$ or $t_{DH2}$ must be met.

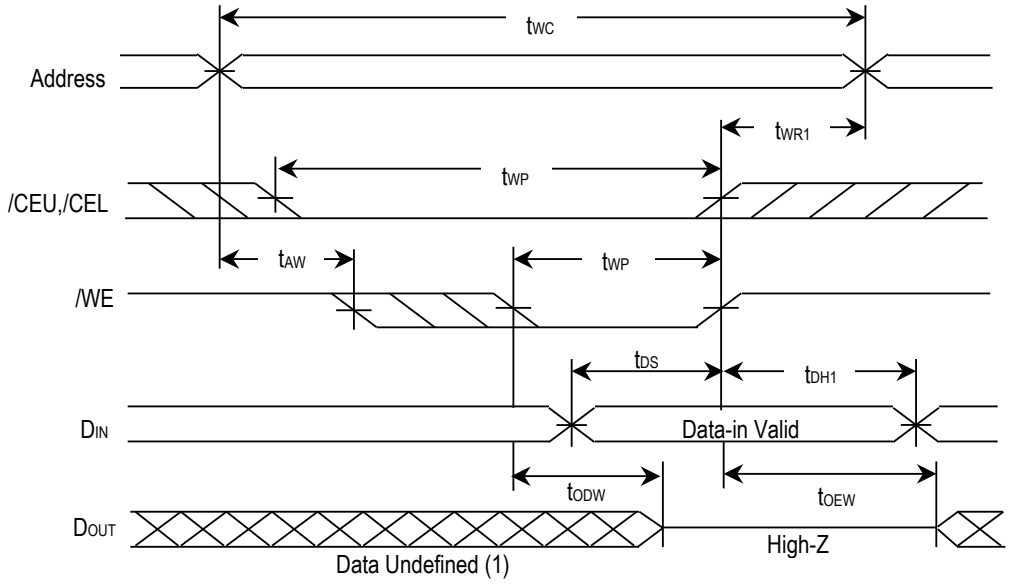
5. If /CE goes low simultaneously with /WE going low or after /WE going low, the outputs remain in high-impedance state.

## TIMING WAVEFORM

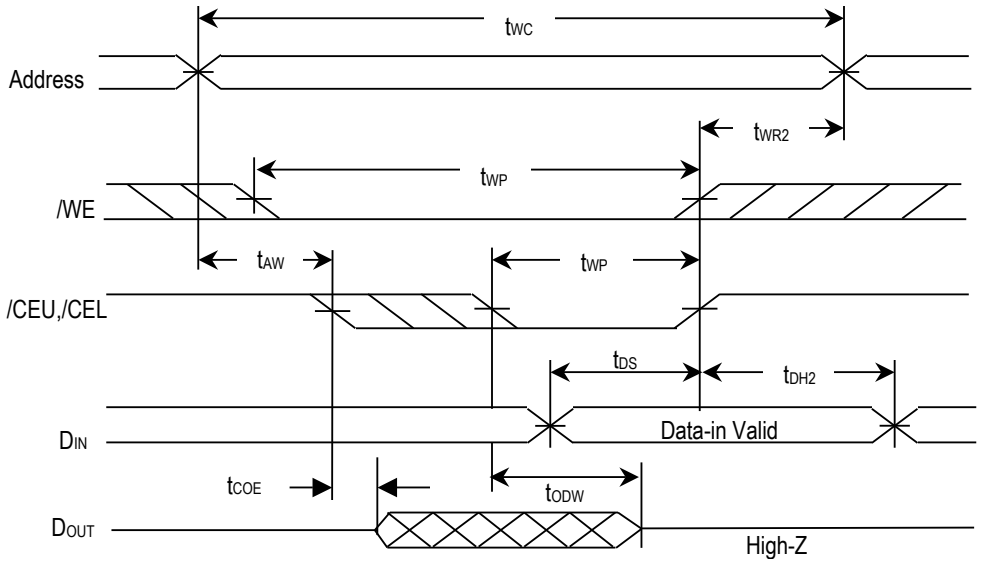
### READ CYCLE



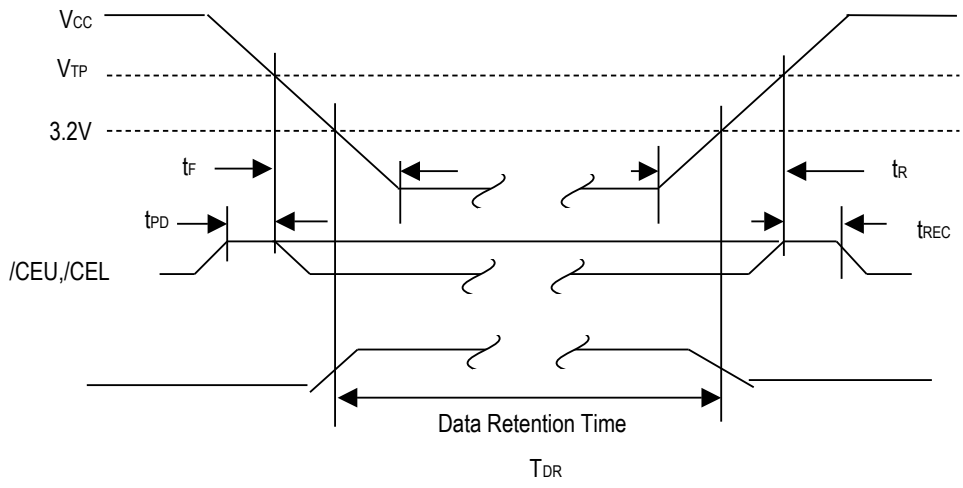

### WRITE CYCLE NO.1



## WRITE CYCLE NO.2




## POWER-DOWN/POWER-UP CONDITION



## POWER-DOWN/POWER-UP TIMING($t_A$= 0$^O$C to 70$^O$C)

| PARAMETER | SYMBOL | MIN | TYP. | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| /CEU,/CEL at $V_{IH}$ before Power-Down | $t_{PD}$ | 0 | - | - | us | 11 |
| $V_{CC}$ Slew from $V_{TP}$ to 0V | $t_F$ | 300 | - | - | us | - |
| $V_{CC}$ Slew from 0V to $V_{TP}$ | $t_R$ | 300 | - | - | us | - |
| /CEU,/CEL at $V_{IH}$ after Power-Up | $t_{REC}$ | 2 | - | 125 | us | - |

($t_A$= 25$^O$C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Expected Data Retention Time | $t_{DR}$ | 10 | - | - | years | 9 |

**WARNING:**

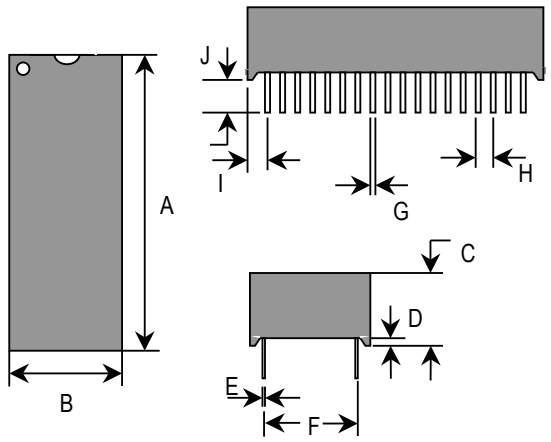
Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

**NOTES:**

1. /WE is high for a read cycle.
2. /OE = $V_{IH}$ or $V_{IL}$ . If /OE = $V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. $t_{WP}$ is specified as the logical and of /CEU or /CEL and /WE. $t_{WP}$ is measured from the latter of /CEU, /CEL or /WE going low to the earlier of /CEU, /CEL or /WE going high.
4. $t_{DS}$ is measured from the earlier of /CEU or /CEL or /WE going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the /CEU or /CEL low transition occurs simultaneously with or later than the /WE low transition in the output buffers remain in a high impedance state during this period.
7. If the /CEU or /CEL high transition occurs prior to or simultaneously with the /WE high transition, the output buffers remain in high impedance state during this period.
8. If /WE is low or the /WE low transition occurs prior to or simultaneously with the /CEU or /CEL low transition, the output buffers remain in a high impedance state during this period.
9. Each HMN12816D has a built-in switch that disconnects the lithium source until $V_{CC}$ is first applied by the user. The expected $t_{DR}$ is defined as accumulative time in the absence of $V_{CC}$ starting from the time power is first applied by the user.
10. All AC and DC electrical characteristics are valid over the full operating temperature range 0_C to 70_C.
11. In a power down condition the voltage on any pin may not exceed the voltage on Vcc .
12. $t_{WR1}$, $t_{DH1}$ are measured from /WE going high.
13. $t_{WR2}$, $t_{DH2}$ are measured from /CEU or /CEL going high.

## PACKAGE DIMENSION

| Dimension | Min | Max |
|---|---|---|
| A | 2.070 | 2.100 |
| B | 0.710 | 0.740 |
| C | 0.365 | 0.375 |
| D | 0.015 | - |
| E | 0.008 | 0.013 |
| F | 0.590 | 0.630 |
| G | 0.017 | 0.023 |
| H | 0.090 | 0.110 |
| I | 0.080 | 0.110 |
| J | 0.120 | 0.150 |




All dimensions are in inches.

## ODERING INFORMATION

**H M N 128 16 D - 70 I**

**Operating Temp. :** Blank = Commercial (0 to 70 °C )
**I** = Industrial (-40 to 85°C)

**Speed options :** 70 = 70 ns
85 = 85 ns
120 = 120 ns
150 = 150 ns

**Dip type package**

**Device :** 128K x 16 bit

**Nonvolatile SRAM**

**HANBit Memory Module**