



Non-Volatile SRAM MODULE 16Mbit (2,048K x 8-Bit), 36Pin-DIP, 5V  
**Part No. HMN2M8D**

## GENERAL DESCRIPTION

The HMN2M8D Nonvolatile SRAM is a 16,777,216-bit static RAM organized as 2,097,152 bytes by 8 bits.

The HMN2M8D has a self-contained lithium energy source provide reliable non-volatility coupled with the unlimited write cycles of standard SRAM and integral control circuitry which constantly monitors the single 5V supply for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on to sustain the memory until after  $V_{CC}$  returns valid and write protection is unconditionally enabled to prevent garbled data. In addition the SRAM is unconditionally write-protected to prevent an inadvertent write operation. At this time the integral energy source is switched on to sustain the memory until after  $V_{CC}$  returns valid.

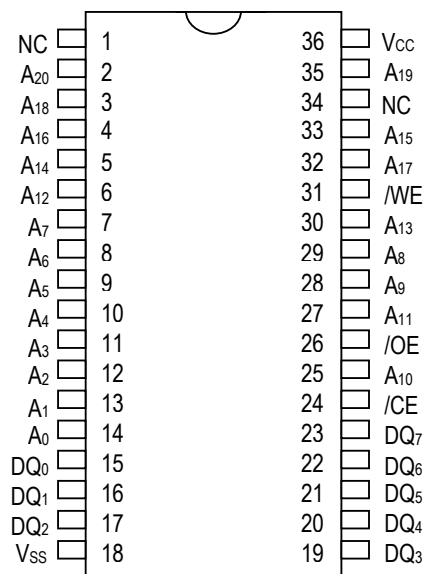
The HMN2M8D uses extremely low standby current CMOS SRAM's, coupled with small lithium coin cells to provide non-volatility without long write-cycle times and the write-cycle limitations associated with EEPROM.

## FEATURES

- ◆ Access time : 70, 85, 120, 150ns
- ◆ High-density design : 16Mbit Design
- ◆ Battery internally isolated until power is applied
- ◆ Industry-standard 36-pin 2,048K x 8 pinout
- ◆ Unlimited write cycles
- ◆ Data retention in the absence of  $V_{CC}$
- ◆ 5-years minimum data retention in absence of power
- ◆ Automatic write-protection during power-up/power-down cycles
- ◆ Data is automatically protected during power loss
- ◆ Industrial temperature operation
- ◆ Timing
 

70 ns	- 70
85 ns	- 85
120 ns	-100
150 ns	-150

## PIN ASSIGNMENT



36-pin Encapsulated Package

## FUNCTIONAL DESCRIPTION

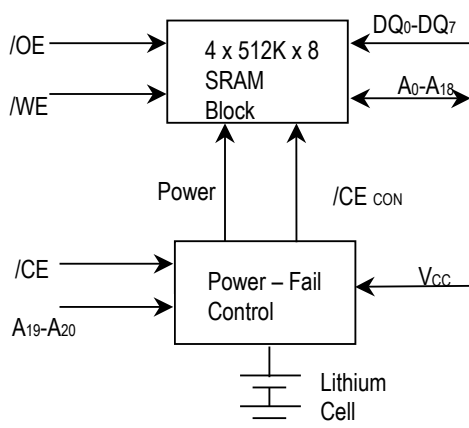
The HMN2M8D executes a read cycle whenever  $/WE$  is inactive(high) and  $/CE$  is active(low). The address specified by the address inputs( $A_0-A_{20}$ ) defines which of the 2,097,152 bytes of data is accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (access time) after the last address input signal is stable.

When power is valid, the HMN2M8D operates as a standard CMOS SRAM. During power-down and power-up cycles, the HMN2M8D acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

The HMN2M8D is in the write mode whenever the  $/WE$  and  $/CE$  signals are in the active (low) state after address inputs are stable. The later occurring falling edge of  $/CE$  or  $/WE$  will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of  $/CE$  or  $/WE$ . All address inputs must be kept valid throughout the write cycle.  $WE$  must return to the high state for a minimum recovery time ( $t_{WR}$ ) before another cycle can be initiated. The  $/OE$  control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus been enabled ( $/CE$  and  $/OE$  active) then  $/WE$  will disable the outputs in  $t_{ODW}$  from its falling edge.

The HMN2M8D provides full functional capability for  $V_{CC}$  greater than 4.5 V and write protects by 4.37 V nominal. Power-down/power-up control circuitry constantly monitors the  $V_{CC}$  supply for a power-fail-detect threshold  $V_{PFD}$ . When  $V_{CC}$  falls below the  $V_{PFD}$  threshold, the SRAM automatically write-protects the data. All inputs to the RAM become "don't care" and all outputs are high impedance. As  $V_{CC}$  falls below approximately 3 V, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts.

## BLOCK DIAGRAM



## PIN DESCRIPTION

$A_0-A_{19}$ : Address Input
$/CE$ : Chip Enable
$V_{SS}$ : Ground
$DQ_0-DQ_7$ : Data In / Data Out
$/WE$ : Write Enable
$/OE$ : Output Enable
$V_{CC}$ : Power (+5V)
NC : No Connection

**TRUTH TABLE**

MODE	/OE	/CE	/WE	I/O OPERATION	POWER
Not selected	X	H	X	High Z	Standby
Output disable	H	L	H	High Z	Active
Read	L	L	H	D <sub>OUT</sub>	Active
Write	X	L	L	D <sub>IN</sub>	Active

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATING	CONDITIONS
DC voltage applied on V <sub>CC</sub> relative to V <sub>SS</sub>	V <sub>CC</sub>	-0.5V to 7.0V	
DC Voltage applied on any pin excluding V <sub>CC</sub> relative to V <sub>SS</sub>	V <sub>T</sub>	-0.5V to 7.0V	
Operating temperature	T <sub>OPR</sub>	0 to 70°C	Commercial
		-40 to 80°C	Industrial
Storage temperature	T <sub>STG</sub>	-55°C to 125°C	
Temperature under bias	T <sub>BIAS</sub>	-40°C to 85°C	
Soldering temperature	T <sub>SOLDER</sub>	260°C	For 10 second

**NOTE:** Permanent device damage may occur if Absolute Maximum Ratings are exceeded.

Functional operation should be restricted to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

**RECOMMENDED DC OPERATING CONDITIONS (T<sub>A</sub> = T<sub>OPR</sub>)**

PARAMETER	SYMBOL	MIN	TYPICAL	MAX
Supply Voltage	V <sub>CC</sub>	4.5V	5.0V	5.5V
Ground	V <sub>SS</sub>	0	0	0
Input high voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.5V
Input low voltage	V <sub>IL</sub>	-0.5	-	0.8V

**NOTE:** Typical values indicate operation at T<sub>A</sub> = 25°C

**DC ELECTRICAL CHARACTERISTICS** ( $T_A = T_{OPR}$ ,  $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$ )

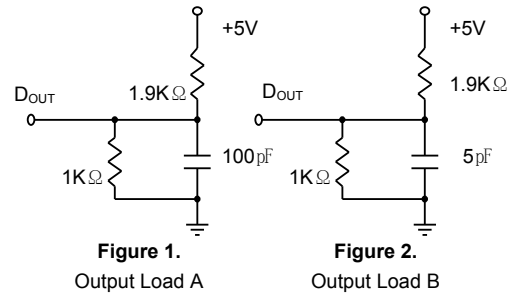
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP.	MAX	UNIT
Input Leakage Current	$V_{IN} = V_{SS}$ to $V_{CC}$	$I_{LI}$	-4	-	4	$\mu A$
Output Leakage Current	$/CE = V_{IH}$ or $/OE = V_{IH}$ or $/WE = V_{IL}$	$I_{LO}$	-4	-	4	$\mu A$
Output high voltage	$I_{OH} = -1.0mA$	$V_{OH}$	2.4	-	-	V
Output low voltage	$I_{OL} = 2.1mA$	$V_{OL}$	-	-	0.4	V
Standby supply current(TTL)	$/CE = V_{IH}$	$I_{SB}$	-	-	12	mA
Standby supply current(COMOS)	Commercial	$/CE \geq V_{CC} - 0.2V$ , $0V \leq V_{IN} \leq 0.2V$ , or $V_{IN} \geq V_{CC} - 0.2V$	-	-	80	$\mu A$
	Industrial		-	-	120	
Operating supply current	Min.cycle,duty=100%, $/CE = V_{IL}$ , $I_{I/O} = 0mA$ , $A_{19} < V_{IL}$ or $A_{19} > V_{IH}$ $A_{20} < V_{IL}$ or $A_{20} > V_{IH}$	$I_{CC}$	-	-	40	mA
Power-fail-detect voltage		$V_{PFD}$	4.30	4.37	4.50	V
Supply switch-over voltage		$V_{SO}$	-	3	-	V

**CAPACITANCE** ( $T_A = 25^\circ C$ ,  $f = 1MHz$ ,  $V_{CC} = 5.0V$ )

DESCRIPTION	CONDITIONS	SYMBOL	MAX	MIN	UNIT
Input Capacitance	Input voltage = 0V	$C_{IN}$	32	-	pF
Input/Output Capacitance	Output voltage = 0V	$C_{I/O}$	40	-	pF

**CHARACTERISTICS (Test Conditions)**

PARAMETER	VALUE
Input pulse levels	0.8 to 2.4V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5V ( unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2



**READ CYCLE** ( $T_A = T_{OPR}$ ,  $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$ )

PARAMETER	SYMBOL	CONDITIONS	-70		-85		-120		-150		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	$t_{RC}$		70	-	85	-	120	-	150	-	ns
Address Access Time	$t_{ACC}$	Output load A	-	70	-	85	-	120	-	150	ns
Chip enable access time	$t_{ACE}$	Output load A	-	70	-	85	-	120	-	150	ns
Output enable to Output valid	$t_{OE}$	Output load A	-	35	-	45	-	60	-	70	ns
Chip enable to output in low Z	$t_{CLZ}$	Output load B	5	-	5	-	5	-	10	-	ns
Output enable to output in low Z	$t_{OLZ}$	Output load B	5	-	0	-	0	-	5	-	ns
Chip disable to output in high Z	$t_{CHZ}$	Output load B	0	25	0	35	0	45	0	60	ns
Output disable to output high Z	$t_{OHZ}$	Output load B	0	25	0	25	0	35	0	50	ns
Output hold from address change	$t_{OH}$	Output load A	10	-	10	-	10	-	10	-	ns

**WRITE CYCLE** ( $T_A = T_{OPR}$ ,  $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$ )

PARAMETER	SYMBOL	CONDITIONS	-70		-85		-120		-150		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	Min	Max	
Write Cycle Time	$t_{WC}$		70	-	85	-	120	-	150	-	ns
Chip enable to end of write	$t_{CW}$	Note 1	65	-	75	-	100	-	100	-	ns
Address setup time	$t_{AS}$	Note 2	0	-	0	-	0	-	0	-	ns
Address valid to end of write	$t_{AW}$	Note 1	65	-	75	-	100	-	90	-	ns
Write pulse width	$t_{WP}$	Note 1	55	-	65	-	85	-	90	-	ns
Write recovery time (write cycle 1)	$t_{WR1}$	Note 3	5	-	5	-	5	-	5	-	ns
Write recovery time (write cycle 2)	$t_{WR2}$	Note 3	15	-	15	-	15	-	15	-	ns
Data valid to end of write	$t_{DW}$		30	-	35	-	45	-	50	-	ns
Data hold time (write cycle 1)	$t_{DH1}$	Note 4	0	-	0	-	0	-	0	-	ns
Data hold time (write cycle 2)	$t_{DH2}$	Note 4	10	-	10	-	10	-	0	-	ns
Write enabled to output in high Z	$t_{WZ}$	Note 5	0	25	0	30	0	40	0	50	ns
Output active from end of write	$t_{OW}$	Note 5	5	-	0	-	0	-	5	-	ns

**NOTE:** 1. A write ends at the earlier transition of /CE going high and /WE going high.

2. A write occurs during the overlap of allow /CE and a low /WE. A write begins at the later transition of /CE going low and /WE going low.

3. Either  $t_{WR1}$  or  $t_{WR2}$  must be met.

4. Either  $t_{DH1}$  or  $t_{DH2}$  must be met.

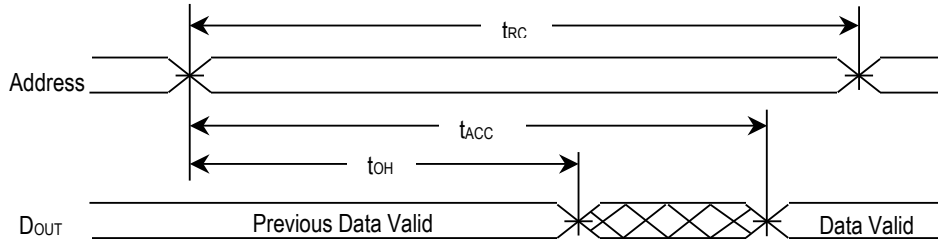
5. If /CE goes low simultaneously with /WE going low or after /WE going low, the outputs remain in high-impedance state.

**POWER-DOWN/POWER-UP CYCLE ( $T_A = T_{OPR}$ ,  $V_{CC} = 5V$ )**

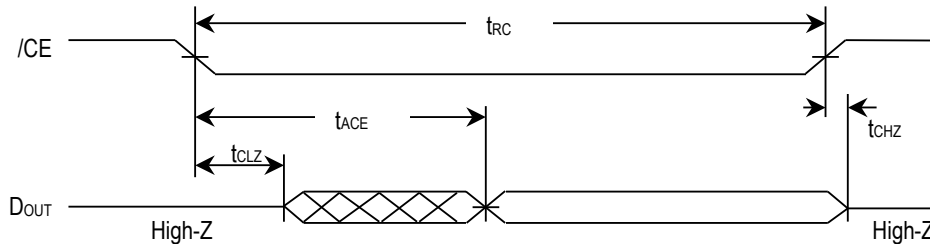
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CC}$ slew, 4.75 to 4.25V	$t_{PF}$		300	-	-	$\mu S$
$V_{CC}$ slew, 4.75 to $V_{SO}$	$t_{FS}$		10	-	-	$\mu S$
$V_{CC}$ slew, $V_{SO}$ to $V_{PFD}$ (max)	$t_{PU}$		0	-	-	$\mu S$
Chip enable recovery time	$t_{CER}$	Time during which SRAM is write-protected after $V_{CC}$ passes $V_{PFD}$ on power-up.	40	80	120	ms
Data-retention time in Absence of $V_{CC}$	$t_{DR}$	$T_A = 25^\circ C$	5	-	-	years
Write-protect time	$t_{WPT}$	Delay after $V_{CC}$ slews down past $V_{PFD}$ before SRAM is Write-protected.	40	100	150	$\mu S$

**TIMING WAVEFORM**

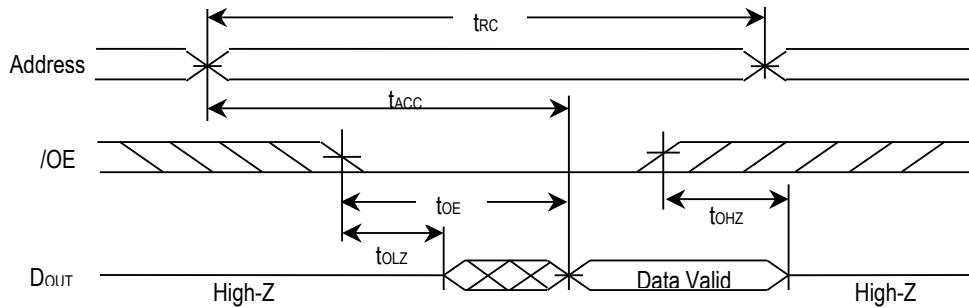
**- Read Cycle No.1 (Address Access)\*1,2**



**- Read Cycle No.2 (/CE Access)\*1,3,4**

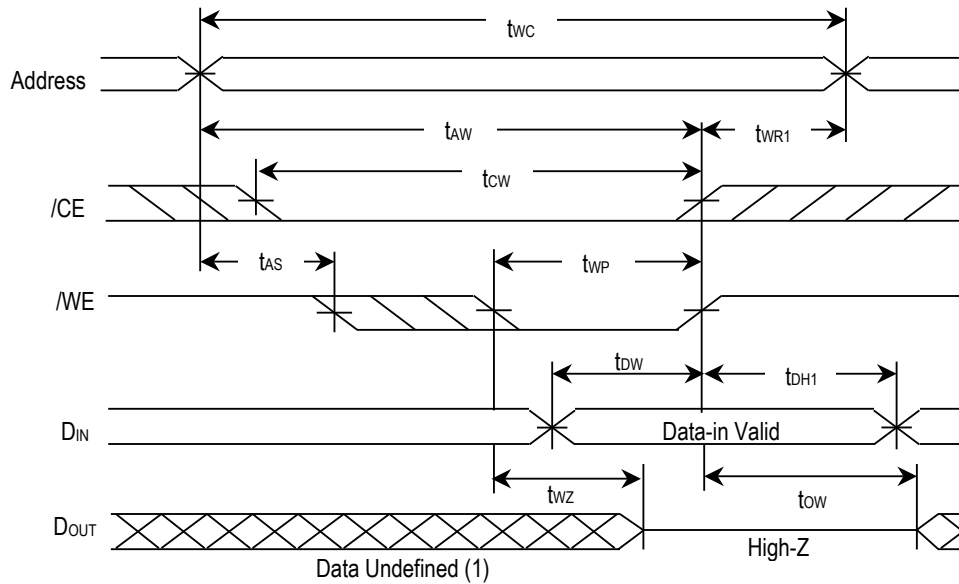


**- Read Cycle No.3 (/OE Access)<sup>\*1,5</sup>**

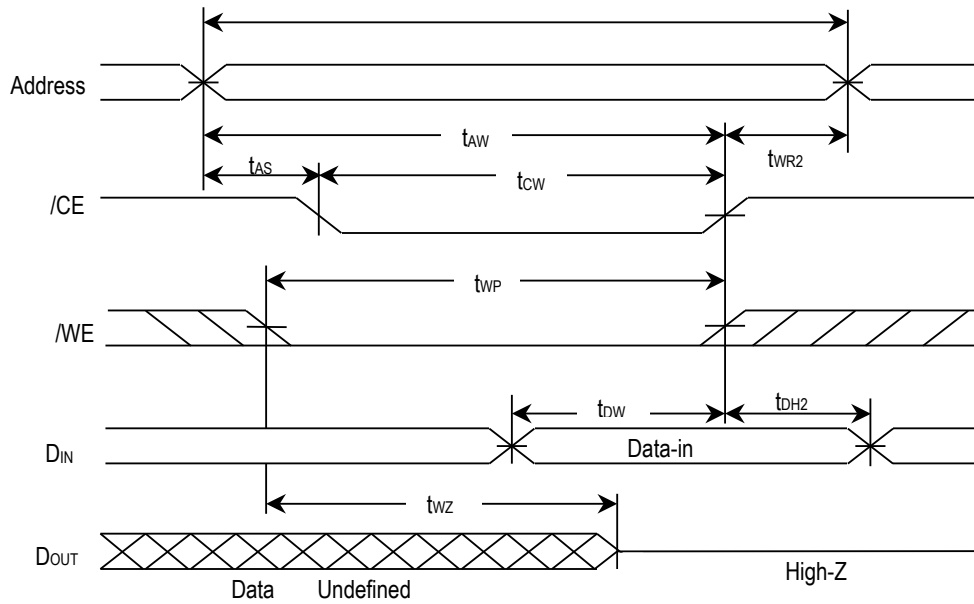


- NOTES:**
1. /WE is held high for a read cycle.
  2. Device is continuously selected: /CE = /OE = V<sub>IL</sub>.
  3. Address is valid prior to or coincident with /CE transition low.
  4. /OE = V<sub>IL</sub>.
  5. Device is continuously selected: /CE = V<sub>IL</sub>.

**- WRITE CYCLE NO.1 (/WE-CONTROLLED)<sup>\*1,2,3</sup>**

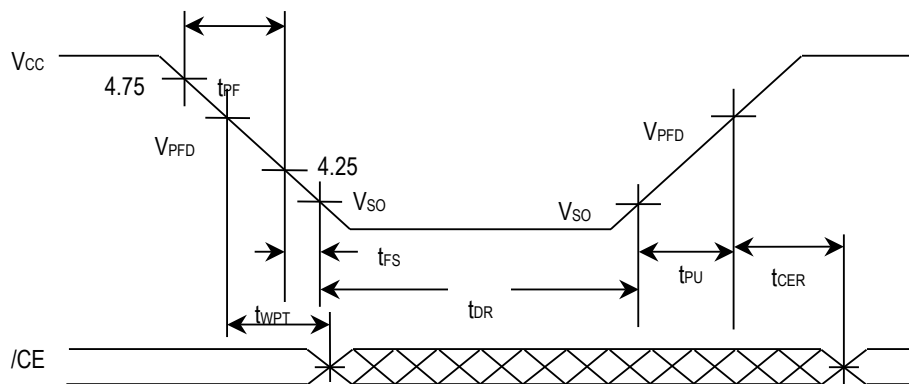


**- WRITE CYCLE NO.2 (/CE-Controlled)\*1,2,3,4,5**



- NOTE:**
1. /CE or /WE must be high during address transition.
  2. Because I/O may be active (/OE low) during this period, data input signals of opposite polarity to the outputs must not be applied.
  3. If /OE is high, the I/O pins remain in a state of high impedance.
  4. Either  $t_{WR1}$  or  $t_{WR2}$  must be met.
  5. Either  $t_{DH1}$  or  $t_{DH2}$  must be met.

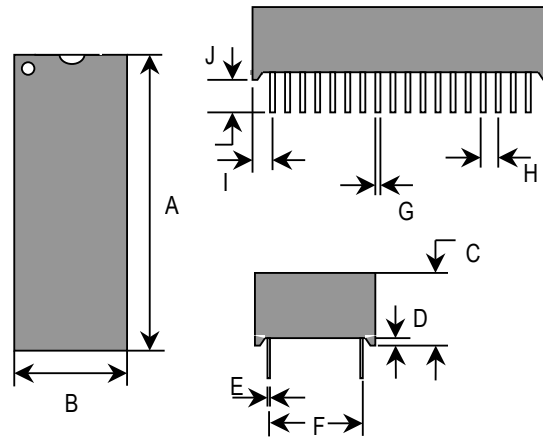
**- POWER-DOWN/POWER-UP TIMING**





**PACKAGE DIMENSION**

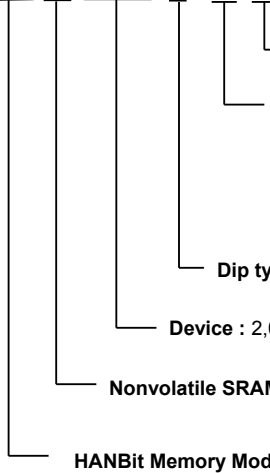
Dimension	Min	Max
A	2.070	2.100
B	0.710	0.740
C	0.365	0.375
D	0.015	-
E	0.008	0.013
F	0.590	0.630
G	0.017	0.023
H	0.090	0.110
I	0.080	0.110
J	0.120	0.150



All dimensions are in inches.

**ODERING INFORMATION**

**H M N 2 M 8 D- 70 I**



Operating Temperature : I = Industrial Temp. (-40~85 °C)  
 Blank = Commercial Temp. (0~70°C)  
 Speed options : 70 = 70 ns  
 85 = 85ns  
 120 = 120ns  
 150 = 150ns

Dip type package  
 Device : 2,048K (2M) x 8 bit

Nonvolatile SRAM

HANBit Memory Module