

N-Channel Super Trench Power MOSFET

Description

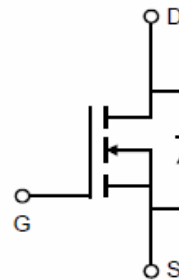
The HMS150N04D uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

General Features

- $V_{DS} = 40V, I_D = 150A$
 $R_{DS(ON)} = 1.6m\Omega$ (typical) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 1.9m\Omega$ (typical) @ $V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Schematic Diagram



Top View



Bottom View

100% UIS TESTED!**100% ΔVds TESTED!**

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
HMS150N04D	HMS150N04D	DFN5X6-8L		-	

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Silicon Limited)	I_D	150	A
Drain Current-Continuous ($T_C = 100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	106	A
Pulsed Drain Current (Package Limited)	I_{DM}	400	A
Maximum Power Dissipation	P_D	88	W
Derating factor		0.7	W/°C
Single pulse avalanche energy (Note 5)	E_{AS}	720	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.42	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	40		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.2	1.5	2.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =75A	-	1.6	1.8	mΩ
		V _{GS} =4.5V, I _D =75A	-	1.9	2.3	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =75A		80	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{ISS}	V _{DS} =20V, V _{GS} =0V, F=1.0MHz	-	6000	7150	PF
Output Capacitance	C _{OSS}		-	1450	1700	PF
Reverse Transfer Capacitance	C _{RSS}		-	100	145	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =20V, I _D =75A V _{GS} =10V, R _G =1.6Ω	-	12.5	-	nS
Turn-on Rise Time	t _r		-	7.0	-	nS
Turn-Off Delay Time	t _{d(off)}		-	50	-	nS
Turn-Off Fall Time	t _f		-	8.5	-	nS
Total Gate Charge	Q _g	V _{DS} =20V, I _D =75A, V _{GS} =10V	-	95	115	nC
Gate-Source Charge	Q _{gs}		-	15		nC
Gate-Drain Charge	Q _{gd}		-	11		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =75A	-		1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	150	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S di/dt = 100A/μs ^(Note3)	-		31	nS
Reverse Recovery Charge	Q _{rr}		-		110	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=20V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Typical Electrical and Thermal Characteristics

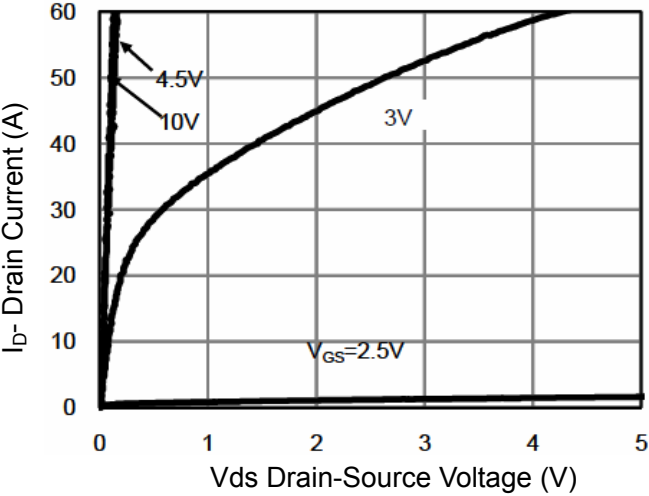


Figure 1 Output Characteristics

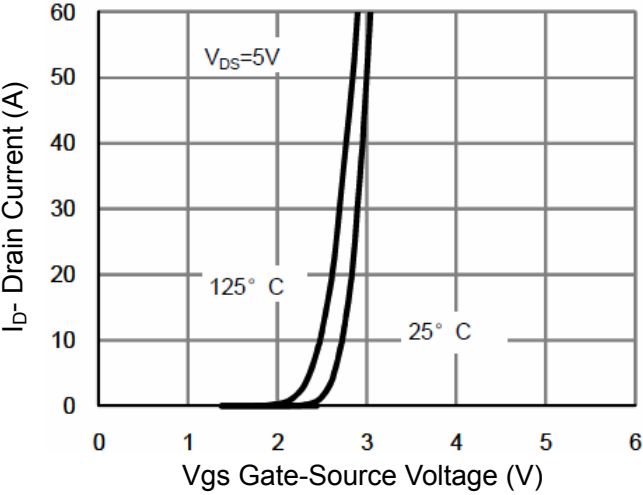


Figure 2 Transfer Characteristics

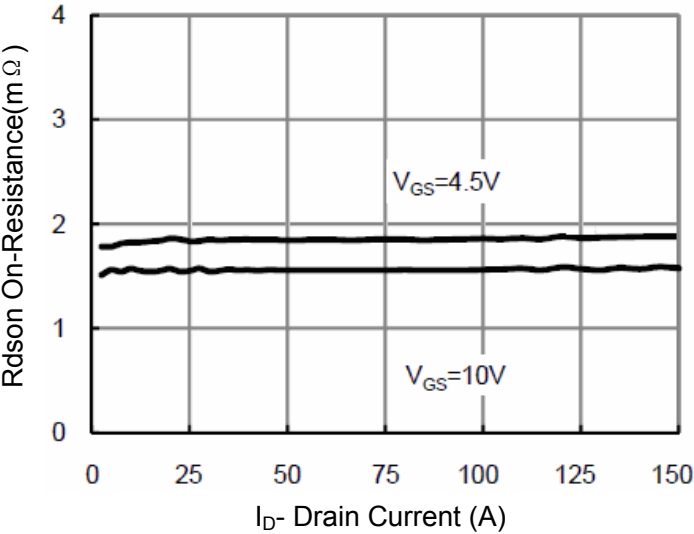


Figure 3 $R_{DS(on)}$ - Drain Current

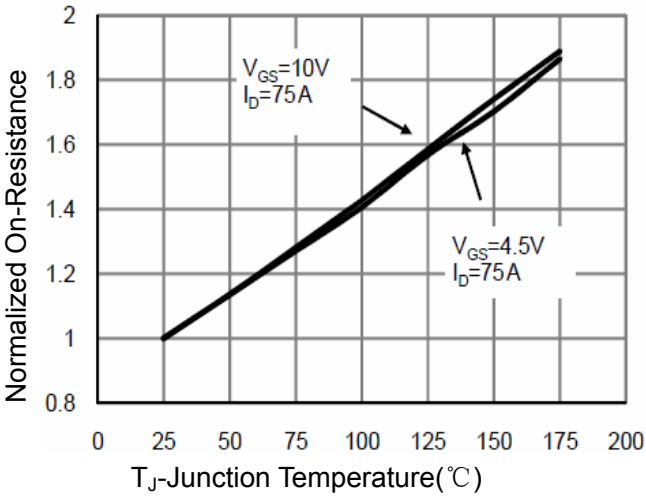


Figure 4 $R_{DS(on)}$ -Junction Temperature

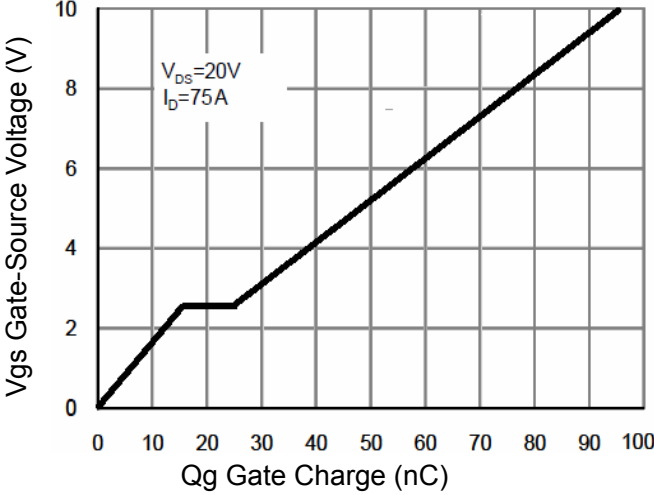


Figure 5 Gate Charge

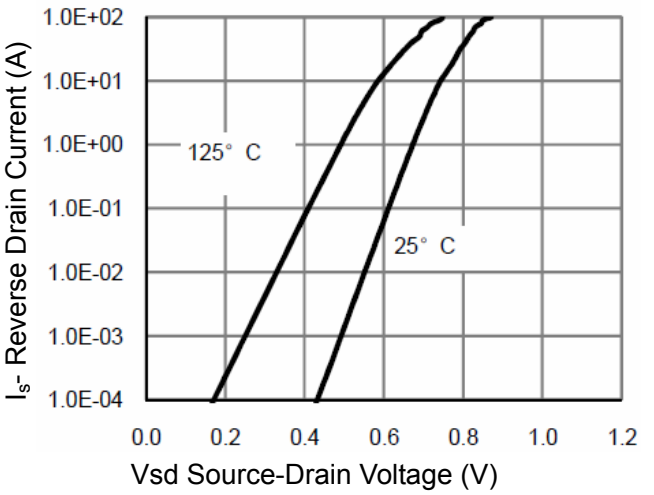


Figure 6 Source- Drain Diode Forward

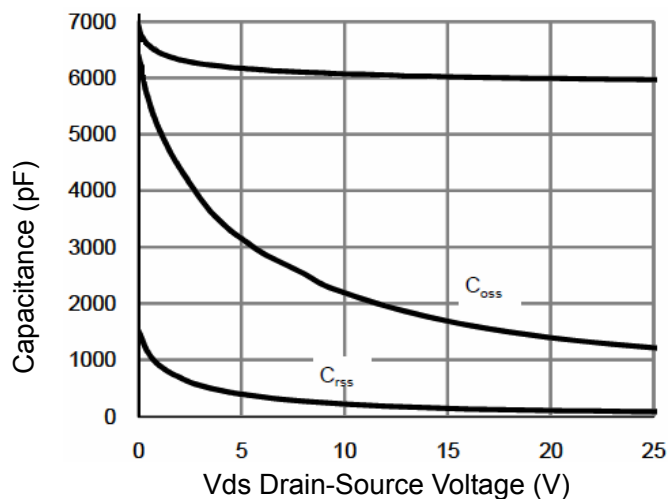


Figure 7 Capacitance vs Vds

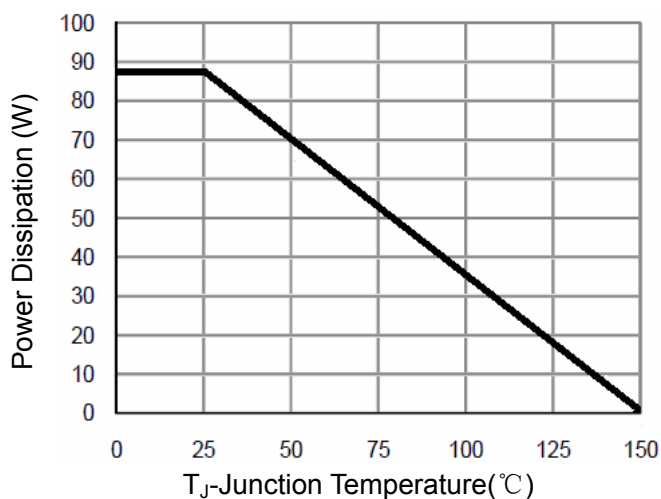


Figure 9 Power De-rating

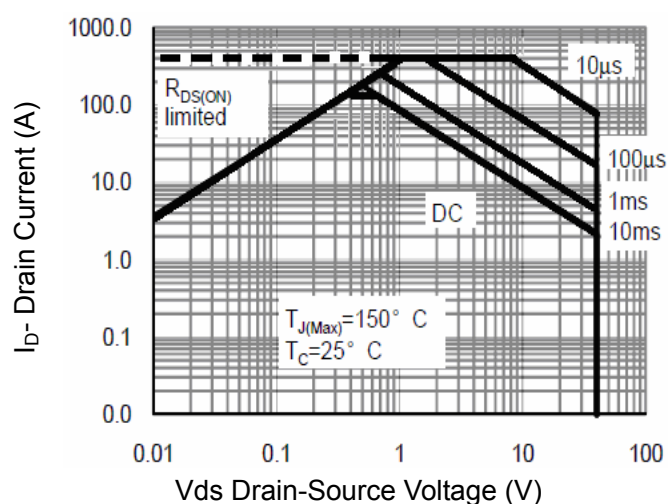


Figure 8 Safe Operation Area

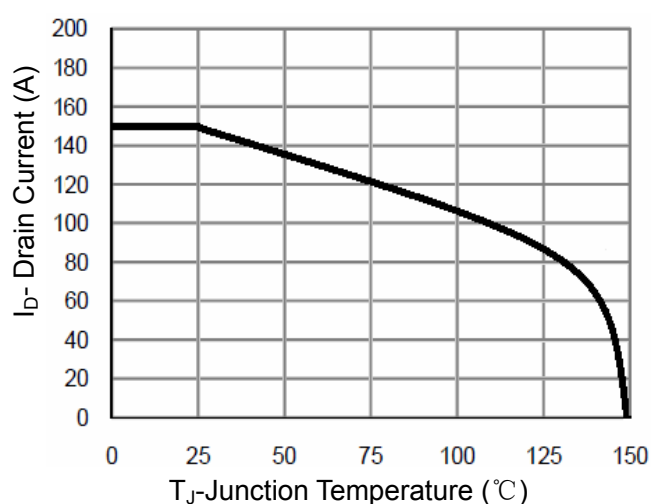


Figure 10 Current De-rating

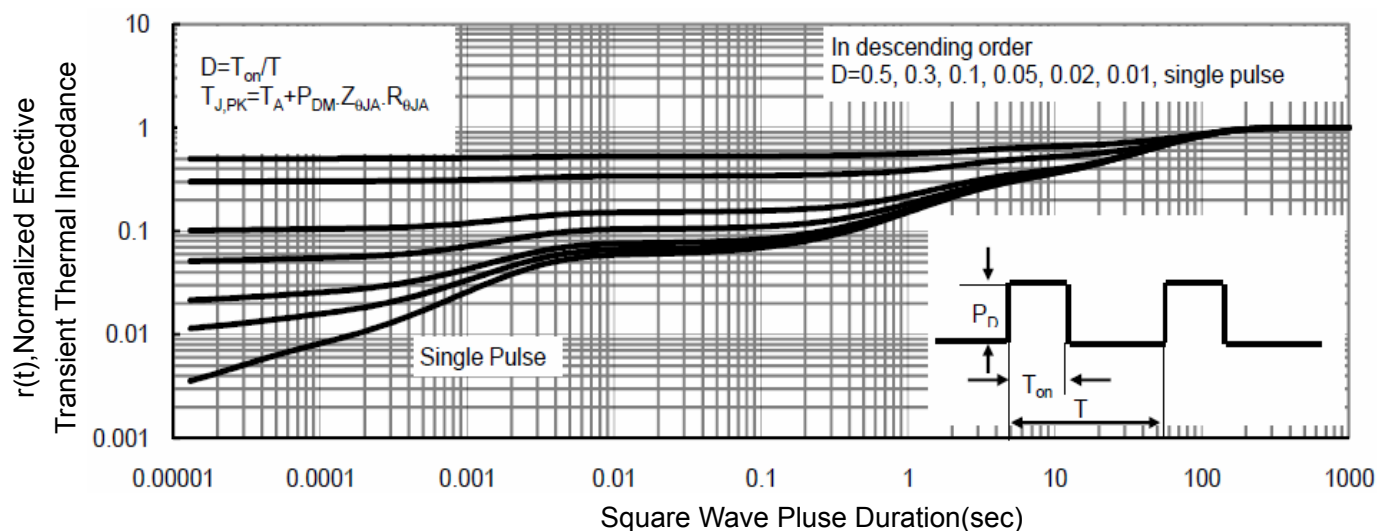
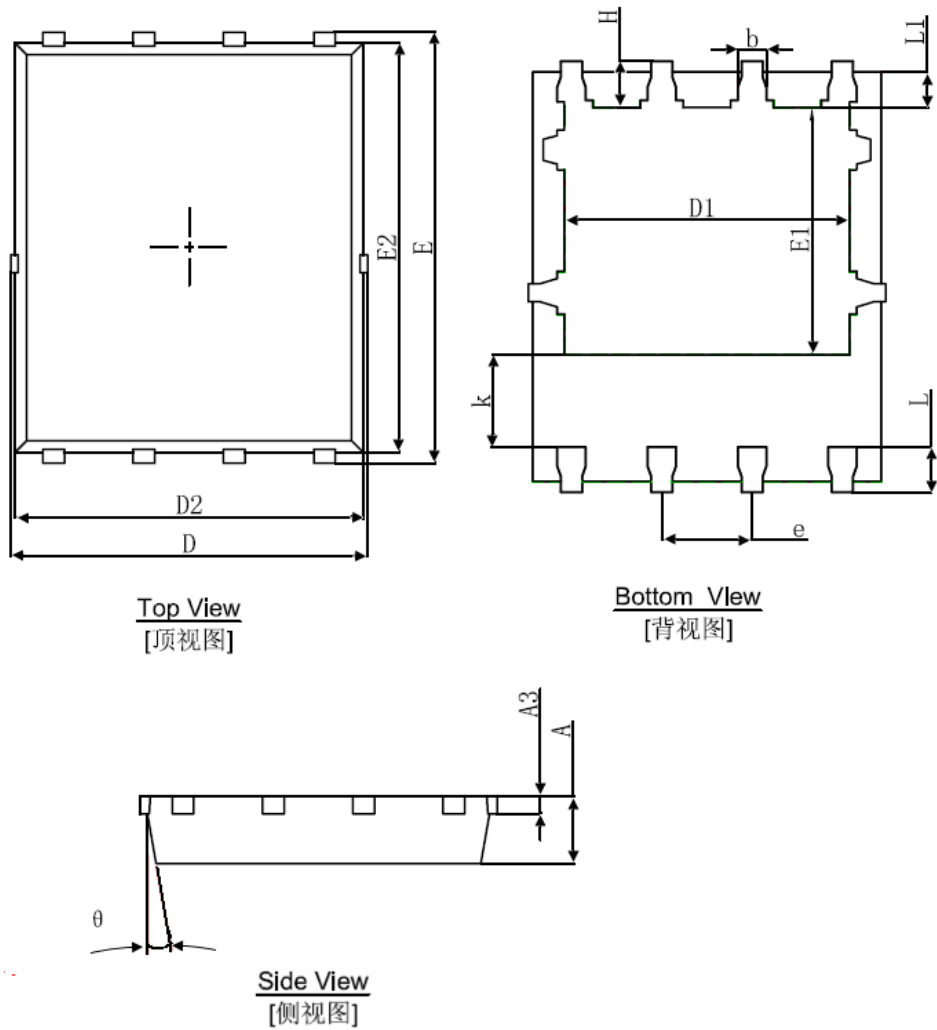


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



Symbol	Diminsions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	8°	12°	8°	12°