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VER. 1.00

4-BIT SINGLE CHIP MICROCOMPUTERS

HMS38112/39112

USER`S MANUAL

- HMS38112
- HMS39112

VER. 1.00

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CHAPTER 1. HMS38112

Outline of characteristics

The HMS38112 is remote control transmitter which uses CMOS technology. This enables transmission code outputs of different configurations, multiple custom code output, and double push key output for easy fabrication.

The HMS38112 is suitable for remote control of TV, VCR, FANS, Air-conditioners, Audio Equipments, Toys, Games etc.

Characteristics

- Program memory : 1,024 bytes
- Data memory : 32×4 bits
- 43 types of instruction set
- 3 levels of subroutine nesting
- Operating frequency : 2.4MHz ~ 4MHz
- Instruction cycle : $f_{OSC}/48$
- CMOS process (Single 3.0V power supply)
- Stop mode (Through internal instruction)
- Released stop mode by key input(mask option)
- Built in Power-on Reset circuit
- Built in Transistor for I.R LED Drive : $I_{OL}=250\text{mA}$ at $V_{DD}=3\text{V}$ and $V_O=0.3\text{V}$
- Built in Low Voltage reset circuit
- Built in a watch dog timer (WDT)
- Low operating voltage : 2.0 ~ 3.6V
- 20 pin PDIP/SOP/SSOP package

Block Diagram

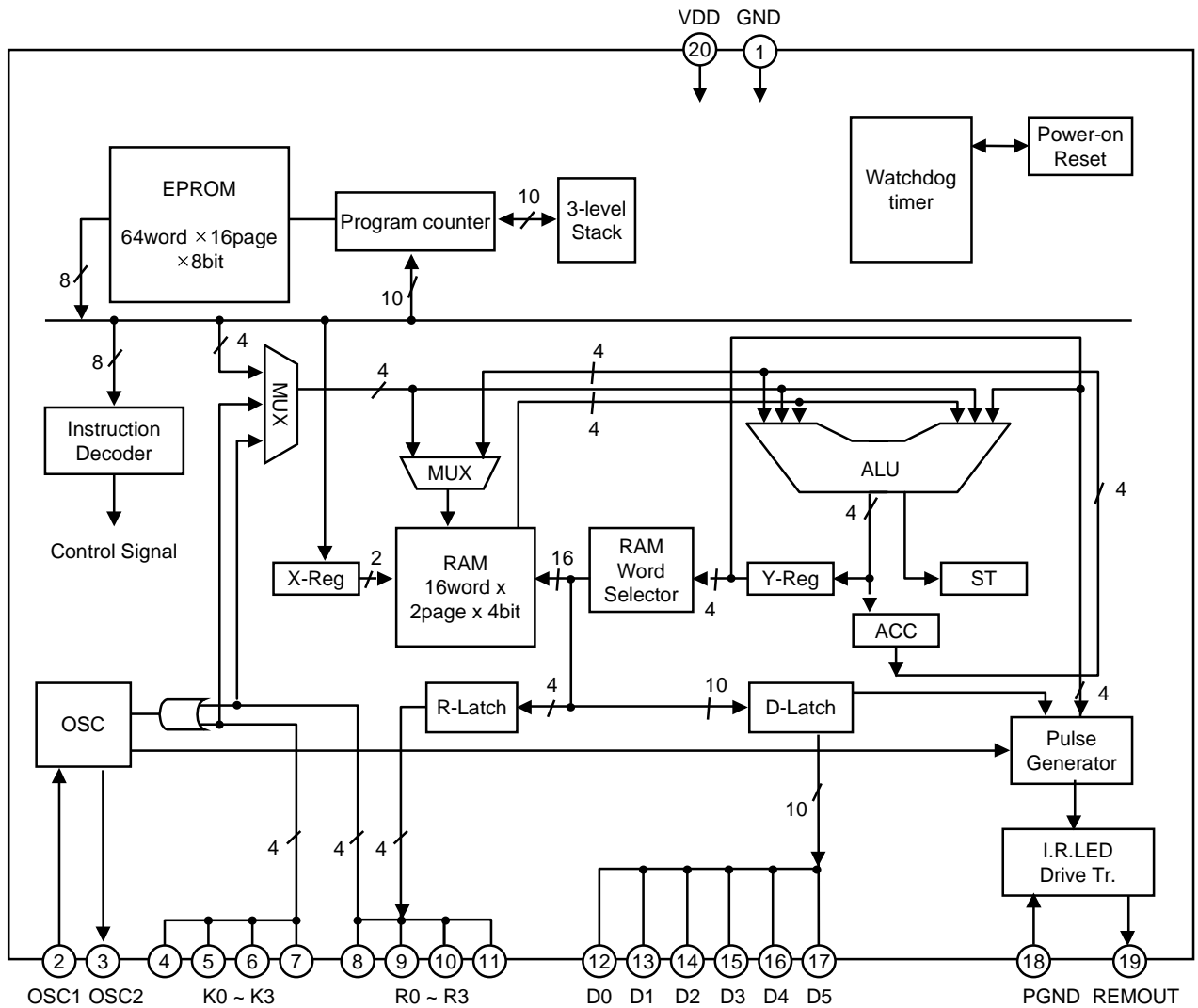


Fig 1-1 Block Diagram

Pin Assignment

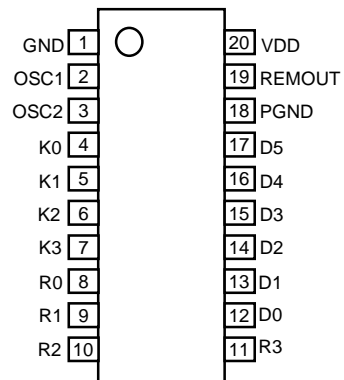


Fig 1-2 HMS38112 Pin Assignment
(20 PIN)

Pin Dimension

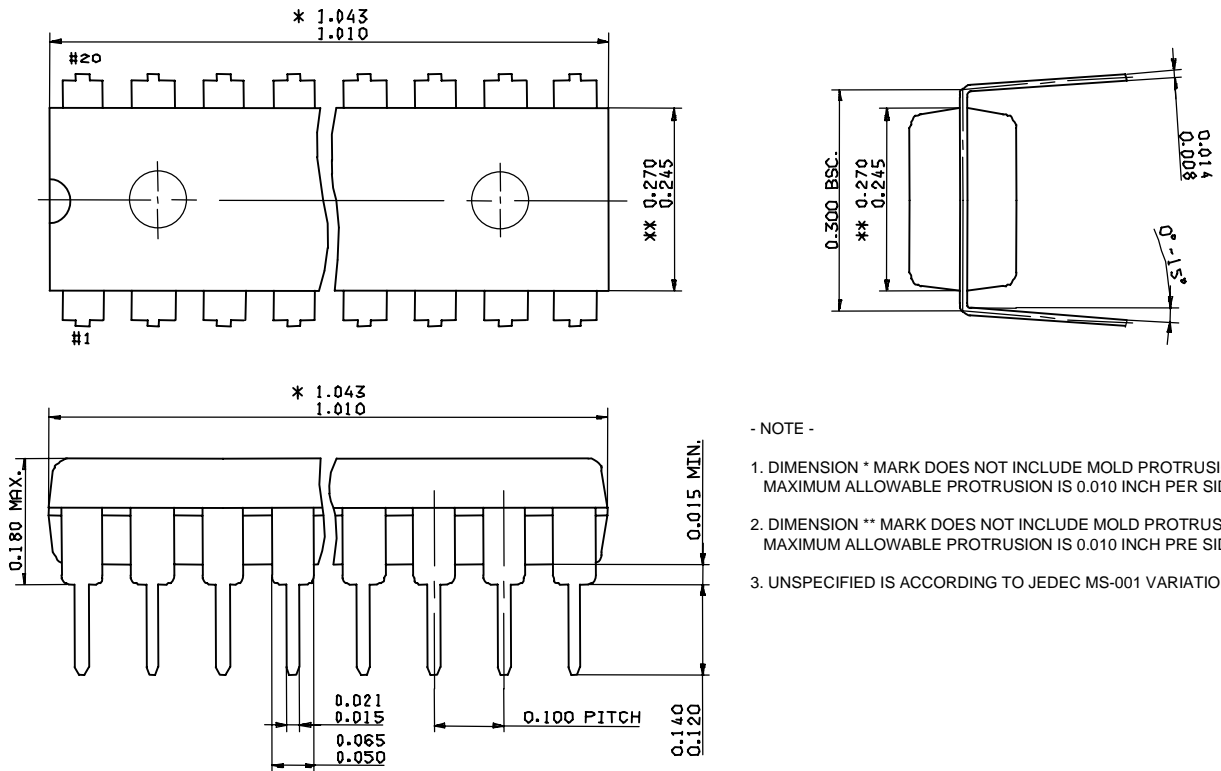


Fig 1-3. 20PDIP (300MIL) Pin Dimension (UNIT : INCH)

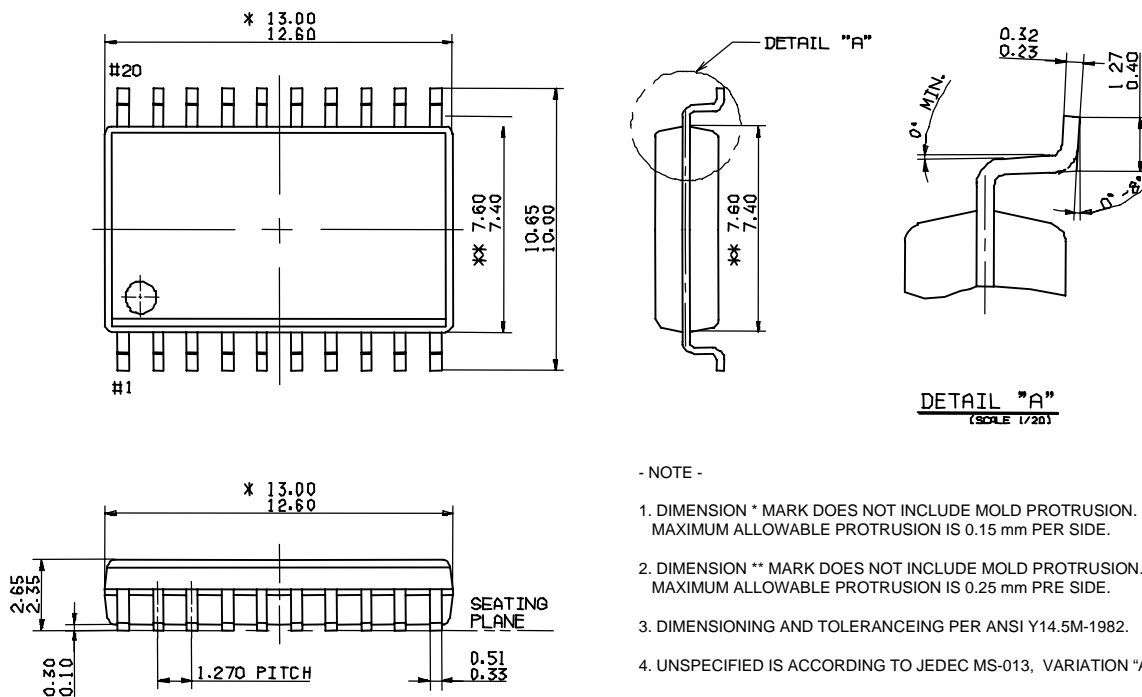
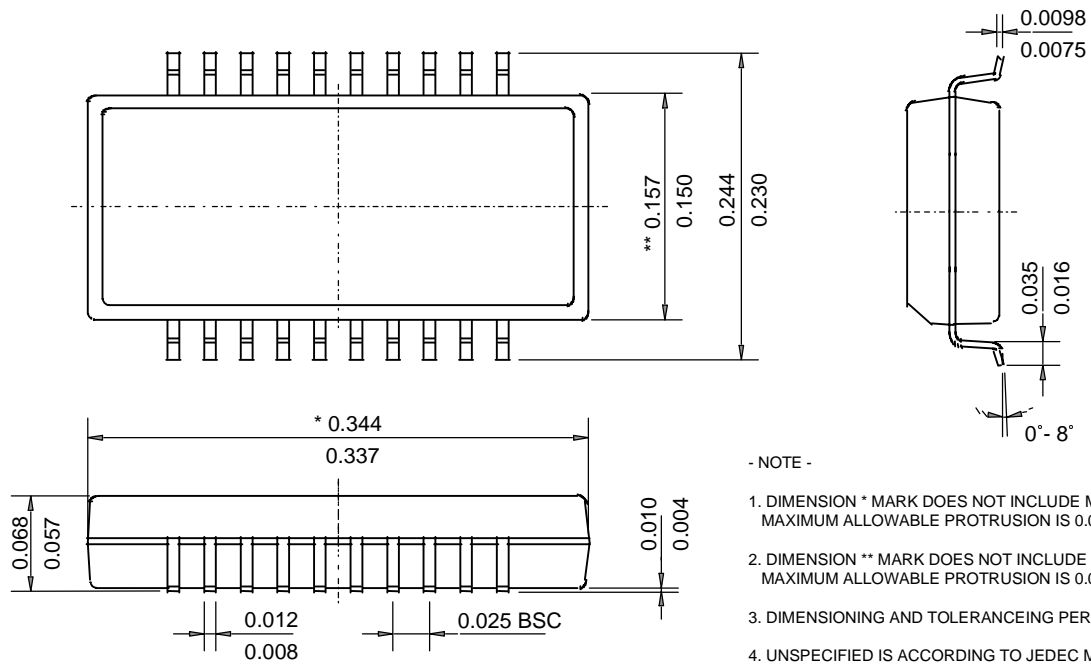


Fig 1-4. 20SOP (300MIL) Pin Dimension (UNIT : mm)



- NOTE -

1. DIMENSION * MARK DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM ALLOWABLE PROTRUSION IS 0.006 INCH PER SIDE.
2. DIMENSION ** MARK DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM ALLOWABLE PROTRUSION IS 0.010 INCH PER SIDE.
3. DIMENSIONING AND TOLERANCEING PER ANSI Y14.5M-1982.
4. UNSPECIFIED IS ACCORDING TO JEDEC MO-137, VARIATION "AD".

Fig 1-5. 20SSOP (150MIL) Pin Dimension (UNIT : inch)

Pin Description and Circuit

Pin Description

Pin	I/O	Function
VDD	-	Connected to 2.0~ 3.6V power supply
GND	-	Connected to 0V power supply.
K0 ~ K3	Input	4-bit input port with built in pull-up resistor. STOP mode is released by "L" input of each pin.
D0 ~ D5	Output	Each can be set and reset independently. The output is the structure of N-channel-open-drain.
R0 ~ R1	Input	2-bit input port with built in pull-up resistor. STOP mode is released by "L" input of each pin.
R2 ~ R3	I/O	2-bit I/O port. (Input mode is set only when each of them output "H".) In outputting, each can be set and reset independently(or at once.) The output is in the form of C-MOS. STOP mode is released by "L" input of each pin.
OSC1	Input	Oscillator input. Input to the oscillator circuit and connection point for ceramic resonator. A feedback resistor is connected between this pin and OSC2.
OSC2	Output	Connect a resonator between this pin and OSC1.
PGND	-	Ground pin for internal high current N-channel transistor. (connected to GND)
REMOUT	Output	High current output port for driving I.R.LED. The output is in the form N-channel open drain.

Pin Circuit

Pin	I/O	I/O circuit	Note
R0 ~ R1	I		<ul style="list-style-type: none"> - Built in MOS Tr for pull-up, about 140kΩ.
R2 ~ R3	I/O		<ul style="list-style-type: none"> - CMOS output. - "H" output at reset. - Built in MOS Tr for pull-up, about 140kΩ.
K0 ~ K3	I		<ul style="list-style-type: none"> - Built in MOS Tr for pull-up, about 140kΩ.
D0 ~ D5	O		<ul style="list-style-type: none"> - Open drain output. - "L" output at reset. - D0~D3 are "L" output at STOP MODE.. - D4 ~D5 pins "Low" or keep before stop mode at STOP MODE (option)
REMOUT	O		<ul style="list-style-type: none"> - Open drain output - Output Tr. Disable at reset.

Pin	I/O	I/O circuit	Note
OSC2	O		<p>- Built in feedback-resistor about 1MΩ</p>
OSC1	I		

Optional Features

The HMS38112 offers the following optional features.

These options are masked.

- I/O terminals having pull-up resistor : R2 ~ R3
- Input terminals having STOP release mode : K0 ~ K3, R0 ~ R3
- Output form at STOP mode : D4 ~D5 pins “L” or keep before stop mode

Electrical Characteristics

Absolute maximum ratings (Ta = 25 °C)

Parameter	Symbol	Max. rating	Unit
Supply Voltage	V_{DD}	-0.3 ~ 5.0	V
Power dissipation	P_D	700 *	mW
Storage temperature range	Tstg	-55 ~ 125	°C
Input voltage	V_{IN}	-0.3 ~ $V_{DD}+0.3$	V
Output voltage	V_{OUT}	-0.3 ~ $V_{DD}+0.3$	V

* Thermal derating above 25 °C : 6mW per degree °C rise in temperature.

Recommended operating condition

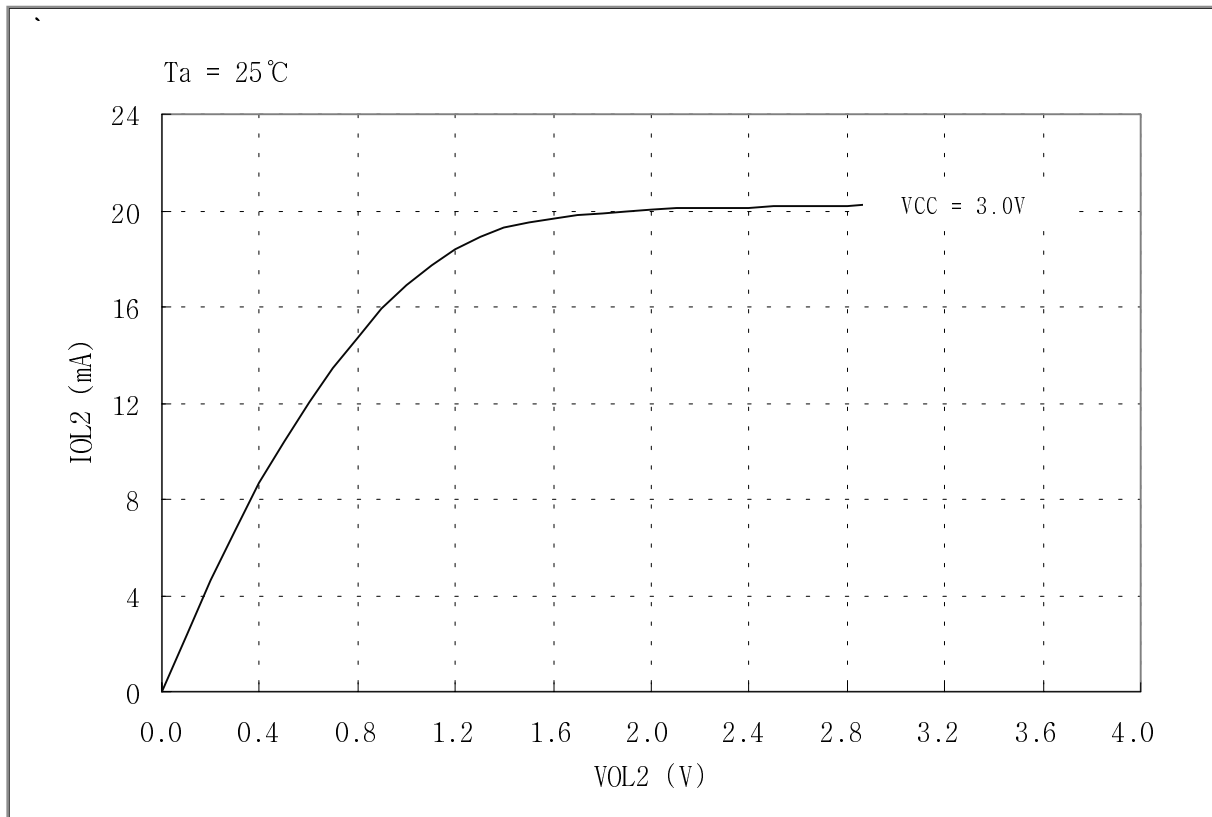
Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	2.4MHz ~ 4MHz	2.0 ~ 3.6	V
Operating temperature	Topr	-	-20 ~ +70	°C

Electrical characteristics (Ta=25°C, V_{DD}= 3V)

Parameter	Symbol	Limits			Unit	Condition	
		Min.	Typ.	Max.			
Input H current	I _{IH}	-	-	1	uA	VI=V _{DD}	
K Pull-up Resistance	R _{PU1}	70	140	300	kΩ	VI=GND	
R Pull-up Resistance	R _{PU2}	70	140	300	kΩ	VI=GND, Output off	
Feedback Resistance	R _{FD}	0.3	1.0	3.0	MΩ	V _{OSC1} =GND, V _{OSC2} =V _{DD}	
K, R input H voltage	V _{IH1}	2.1	-	-	V	-	
K, R input L voltage	V _{IL1}	-	-	0.9	V	-	
D, R output L voltage	V _{OL2} *1	-	0.15	0.4	V	I _{OL} =3mA	
OSC2 output L voltage	V _{OL3}	-	0.4	0.9	V	I _{OL} =150uA	
OSC2 output H voltage	V _{OH3}	2.1	2.5	-	V	I _{OH} =-150uA	
REMOUT output L current	I _{OL1}		250		mA	V _{OL} =0.3V	
REMOUT leakage current	I _{OLK1}	-	-	1	uA	V _{OUT} =V _{DD} , Output off	
D, R output leakage current	I _{OLK2}	-	-	1	uA	V _{OUT} =V _{DD} , Output off	
Current on STOP mode	I _{STP}	-	-	1	uA	At STOP mode	
Operating supply current	I _{DD} *2	-	0.5	1.5	mA	f _{OSC} =4MHz	
System clock frequency	f _{OSC} /48	f _{OSC}	2.4	-	4	MHz	MHZ version

*1 Refer to Fig.1-6 < I_{OL2} vs. V_{OL2} Graph >

*2 I_{DD} is measured at RESET mode.

Fig 1-6. I_{OL2} vs. V_{OL2} Graph. (D, R Port)

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CHAPTER 2. HMS39112

Outline of characteristics

The HMS39112 is remote control transmitter which uses CMOS technology. This enables transmission code outputs of different configurations, multiple custom code output, and double push key output for easy fabrication.

The HMS39112 is suitable for remote control of TV, VCR, FANS, Air-conditioners, Audio Equipments, Toys, Games etc.

It is possible to structure the 8 x 7 key matrix.

Characteristics

- Program memory : 1,024 bytes
- Data memory : 32 × 4 bits
- 43 types of instruction set
- 3 levels of subroutine nesting
- Operating frequency : 2.4MHz ~ 4MHz
- Instruction cycle : $f_{OSC}/48$
- CMOS process (Single 3.0V power supply)
- Stop mode (Through internal instruction)
- Released stop mode by key input(mask option)
- Built in Power-on Reset circuit
- Built in Low Voltage reset circuit
- Built in a watch dog timer (WDT)
- Low operating voltage : 2.0 ~ 3.6V
- 20 pin PDIP/SOP/SSOP package

Block Diagram

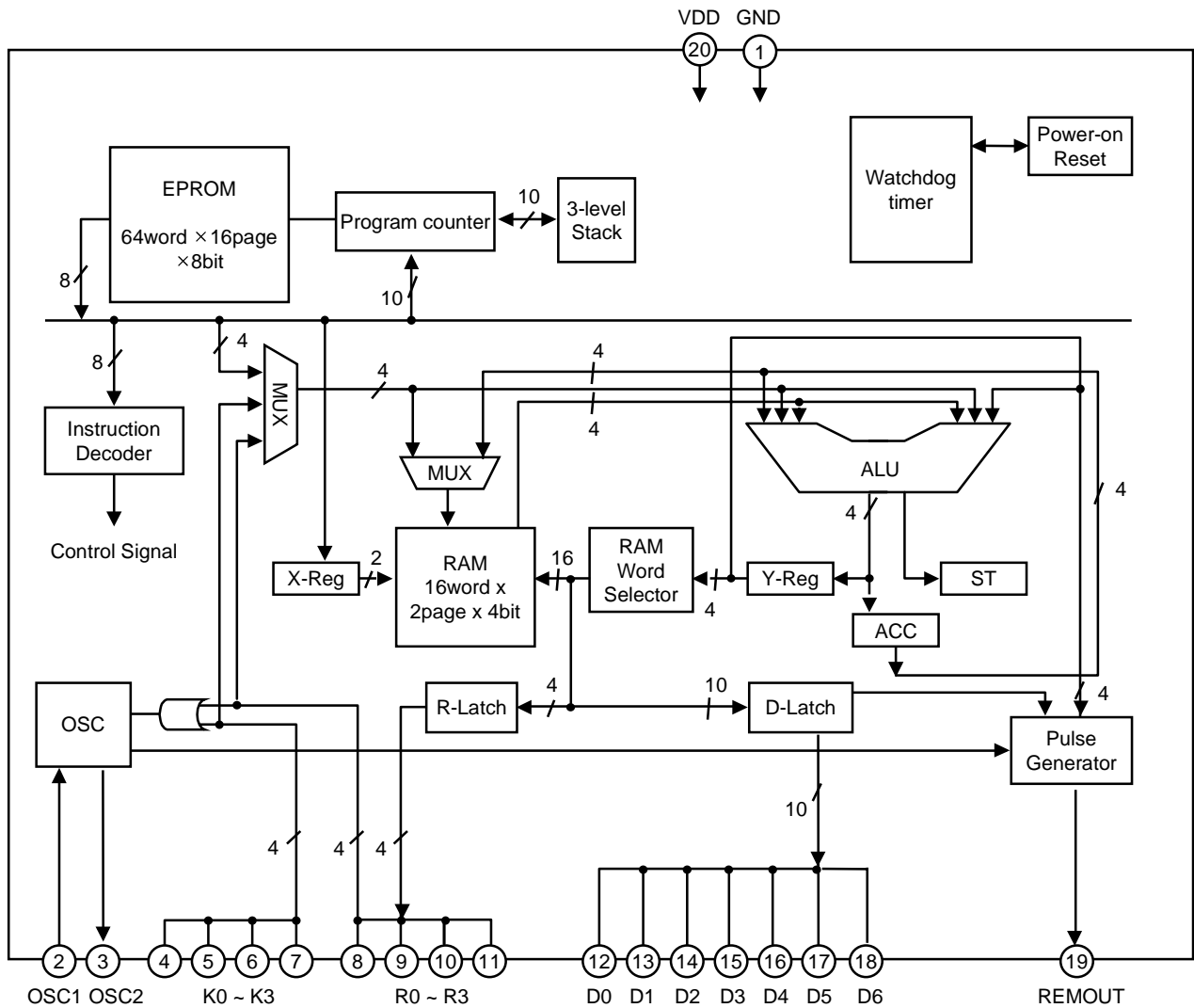


Fig 2-1 Block Diagram

Pin Assignment

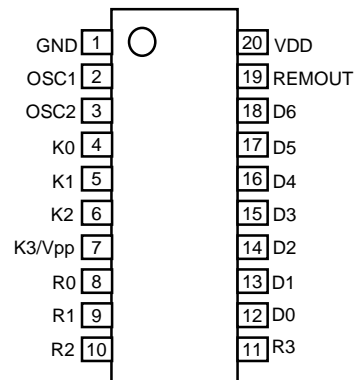


Fig 2-2 HMS39112 Pin Assignment
(20 PIN)

Pin Dimension

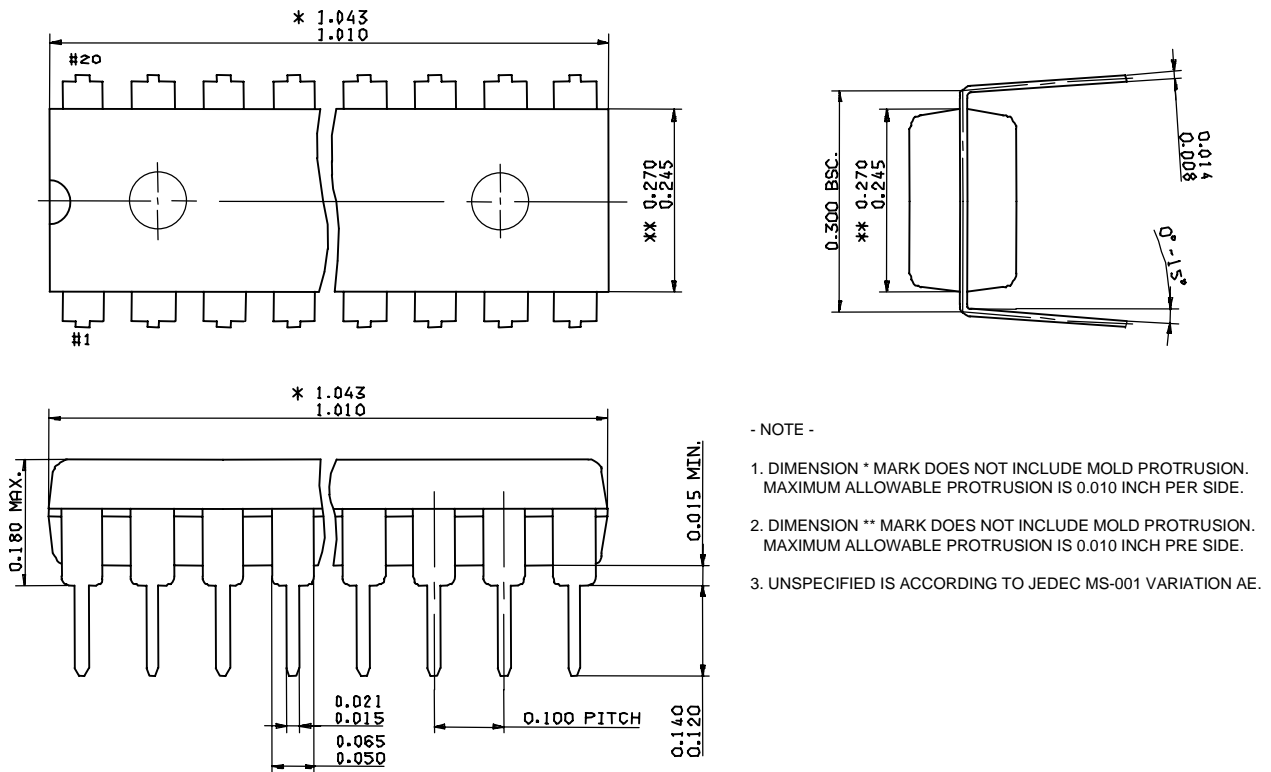


Fig 2-3. 20PDIP (300MIL) Pin Dimension (UNIT : INCH)

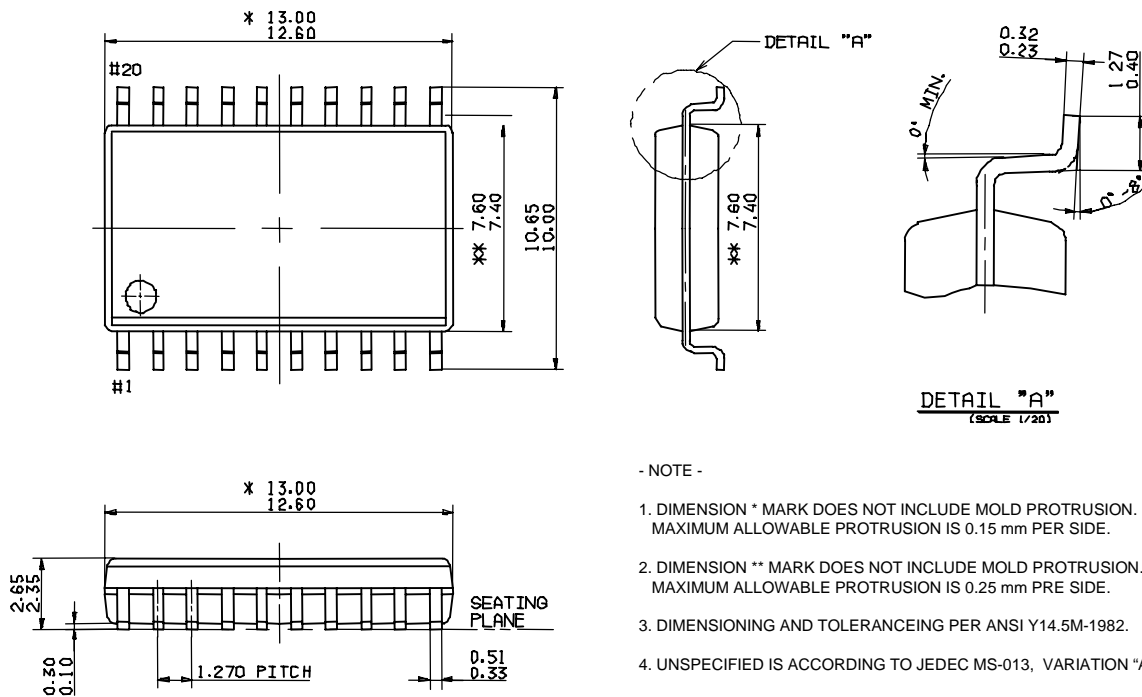
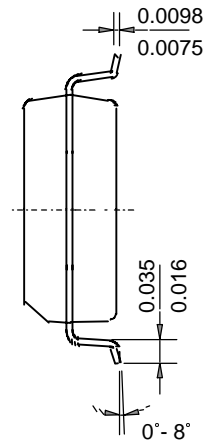
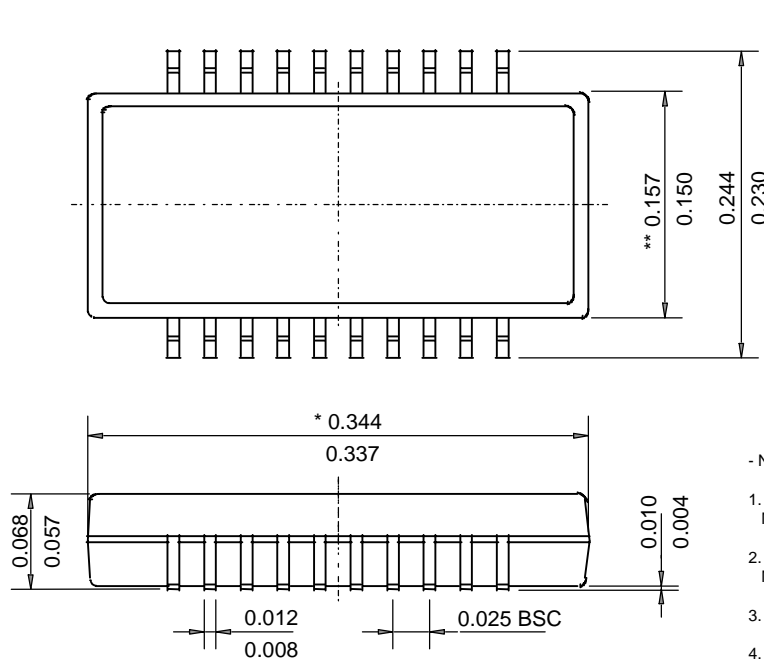


Fig 2-4. 20SOP (300MIL) Pin Dimension (UNIT : mm)



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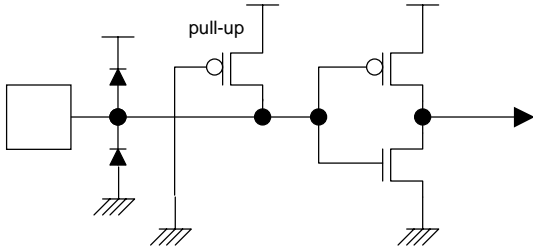
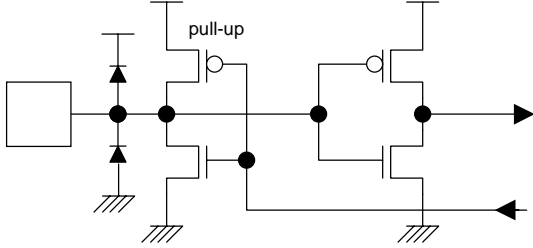
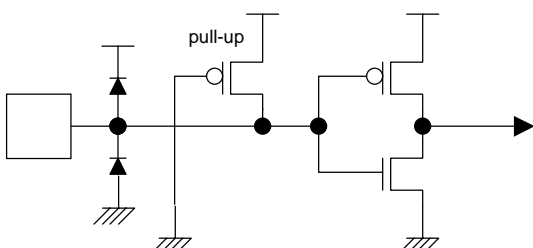
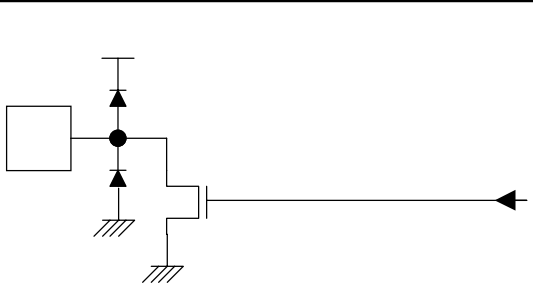
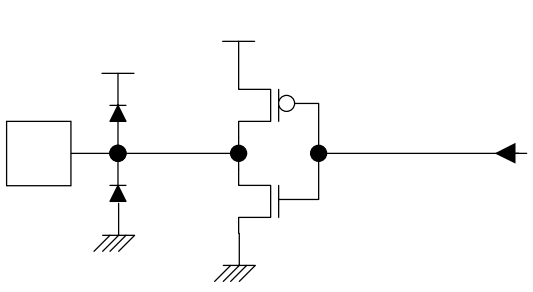
Fig 2-5. 20SSOP (150MIL) Pin Dimension (UNIT : INCH)

Pin Description and Circuit

Pin Description

Pin	I/O	Function
VDD	-	Connected to 2.0~ 3.6V power supply
GND	-	Connected to 0V power supply.
K0 ~ K3	Input	4-bit input port with built in pull-up resistor. STOP mode is released by "L" input of each pin.(masked option)
D0 ~ D6	Output	Each can be set and reset independently. The output is the structure of N-channel-open-drain.
R0 ~ R1	Input	2-bit input port with built in pull-up resistor. STOP mode is released by "L" input of each pin.(masked option)
R2 ~ R3	I/O	2-bit I/O port. (Input mode is set only when each of them output "H".) In outputting, each can be set and reset independently(or at once.) The output is in the form of C-MOS. STOP mode is released by "L" input of each pin. Pull-up resistor and STOP release mode can be respectively selected as masked option for each pin.(It is released by "L" input at STOP)
OSC1	Input	Oscillator input. Input to the oscillator circuit and connection point for ceramic resonator. A feedback resistor is connected between this pin and OSC2.
OSC2	Output	Connect a resonator between this pin and OSC1.
REMOUT	Output	High current output port for driving I.R.LED. The output is in the form N-channel open drain.

Pin Circuit

Pin	I/O	I/O circuit	Note
R0 ~ R1	I		- Built in MOS Tr for pull-up, about 140kΩ.
R2 ~ R3	I/O		- CMOS output. - "H" output at reset. - Built in MOS Tr for pull-up, about 140kΩ.
K0 ~ K3	I		- Built in MOS Tr for pull-up, about 140kΩ.
D0 ~ D6	O		- Open drain output. - "L" output at reset. - D0~D3 are "L" output at STOP MODE. - D4 ~D6 pins "L" or keep before stop mode At STOP MODE(option)
REMOUT	O		- Open drain output - "L" output at reset. - High current output source.

Pin	I/O	I/O circuit	Note
OSC2	O		- Built in feedback-resistor about 1MΩ
OSC1	I		

Optional Features

The HMS39112 offers the following optional features.

These options are masked.

- I/O terminals having pull-up resistor : R2 ~ R3
- Input terminals having STOP release mode : K0 ~ K3, R0 ~ R3
- Output form at STOP mode : D4 ~D6 pins “L” or keep before stop mode

Electrical Characteristics

Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Max. rating	Unit
Supply Voltage	V_{DD}	-0.3 ~ 5.0	V
Power dissipation	P_D	700 *	mW
Storage temperature range	Tstg	-55 ~ 125	°C
Input voltage	V_{IN}	-0.3 ~ $V_{DD}+0.3$	V
Output voltage	V_{OUT}	-0.3 ~ $V_{DD}+0.3$	V

* Thermal derating above 25°C : 6mW per degree °C rise in temperature.

Recommended operating condition

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	2.4MHz ~ 4MHz	2.0 ~ 3.6	V
Operating temperature	Topr	-	-20 ~ +70	°C

Electrical characteristics (Ta=25°C, V_{DD}= 3V)

Parameter	Symbol	Limits			Unit	Condition	
		Min.	Typ.	Max.			
Input H current	I _{IH}	-	-	1	uA	VI=V _{DD}	
K Pull-up Resistance	R _{PU1}	70	140	300	kΩ	VI=GND	
R Pull-up Resistance	R _{PU2}	70	140	300	kΩ	VI=GND, Output off	
Feedback Resistance	R _{FD}	0.3	1.0	3.0	MΩ	V _{OSC1} =GND, V _{OSC2} =V _{DD}	
K, R input H voltage	V _{IH1}	2.1	-	-	V	-	
K, R input L voltage	V _{IL1}	-	-	0.9	V	-	
D, R output L voltage	V _{OL2} *1	-	0.15	0.4	V	I _{OL} =3mA	
OSC2 output L voltage	V _{OL3}	-	0.4	0.9	V	I _{OL} =150uA	
OSC2 output H voltage	V _{OH3}	2.1	2.5	-	V	I _{OH} =-150uA	
REMOUT output L current	I _{OL1} *2	0.5	1.1	3	mA	V _{OL1} =0.4V	
REMOUT output H current	I _{OH1} *3	-5	-15	-30	mA	V _{OH1} =2V	
D, R output leakage current	I _{OLK2}	-	-	1	uA	V _{OUT} =V _{DD} , Output off	
Current on STOP mode	I _{STP}	-	-	1	uA	At STOP mode	
Operating supply current	I _{DD} *4	-	0.5	1.5	mA	f _{OSC} =4MHz	
System clock frequency	f _{OSC} /48	f _{OSC}	2.4	-	4	MHz	MHz version

*1 Refer to Fig.2-6 < I_{OL2} vs. V_{OL2} Graph>

*2 Refer to Fig.2-7 < I_{OL1} vs. V_{OL1} Graph>

*3 Refer to Fig.2-8 < I_{OH1} vs. V_{OH1} Graph>

*4 I_{DD} is measured at RESET mode.

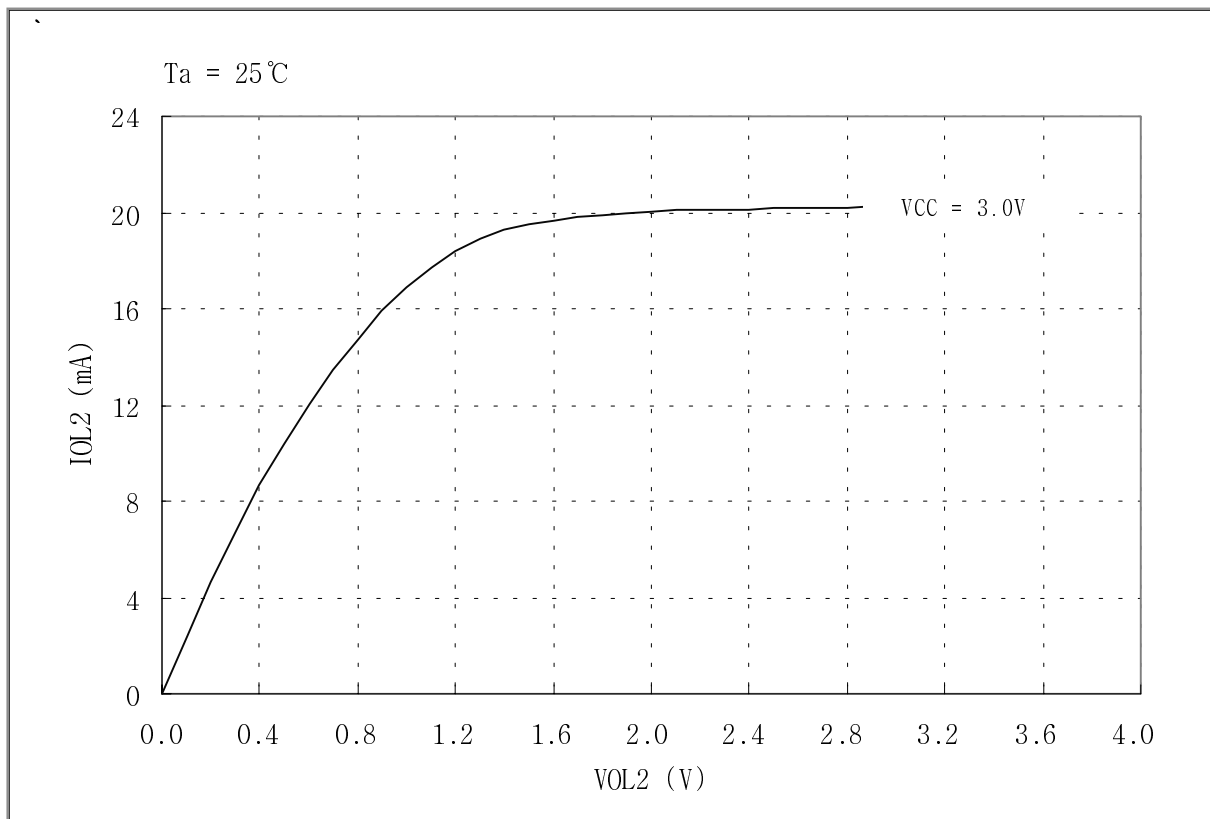
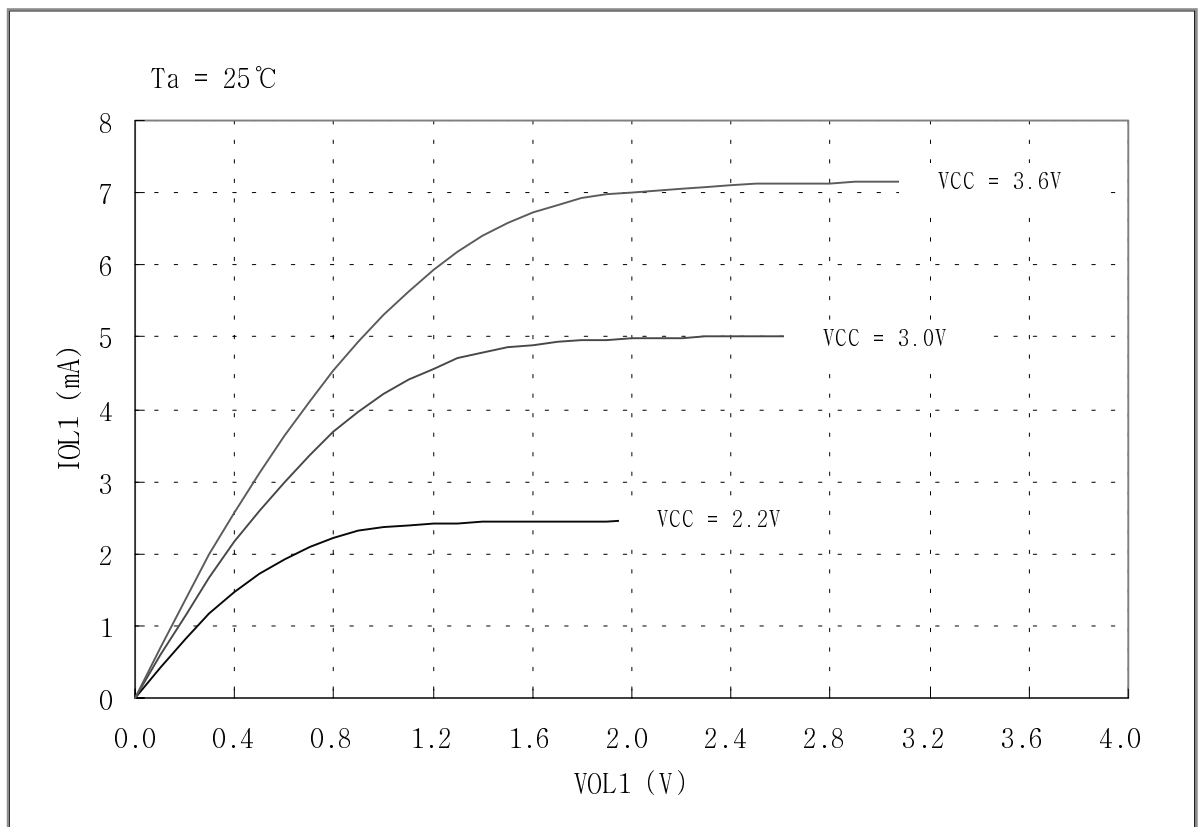
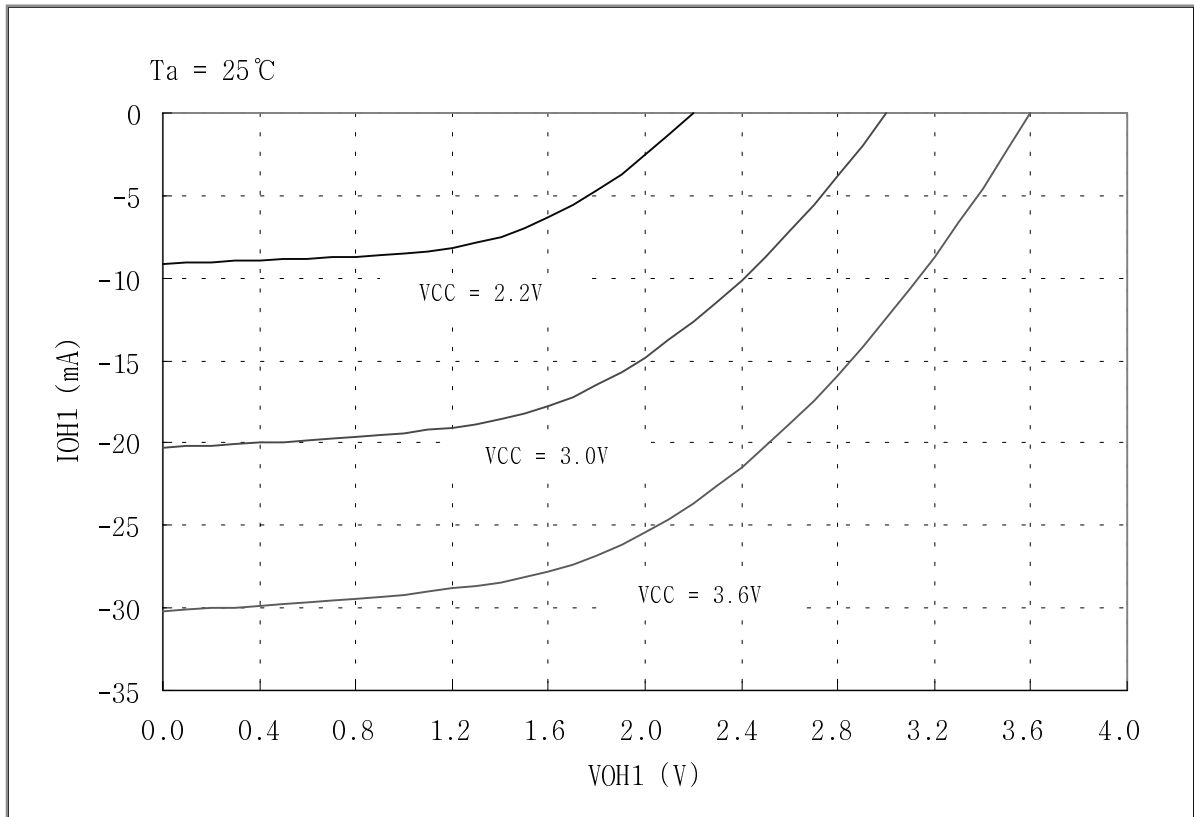
Fig 2-6. I_{OL2} vs. V_{OL2} Graph. (D, R Port)Fig 2-7. I_{OL1} vs V_{OL1} Graph (REMOUT Port)

Fig 2-8. I_{OH1} vs V_{OH1} Graph (REMOUT Port)



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CHAPTER 3. Architecture

Program Memory

The HMS38112/39112 can incorporate maximum 1,024 words (64 words × 16 pages × 8bits) for program memory. Program counter PC (A0~A5) and page address register (A6~A9) are used to address the whole area of program memory having an instruction (8bits) to be next executed.

The program memory consists of 64 words on each page, and thus each page can hold up to 64 steps of instructions.

The program memory is composed as shown below.

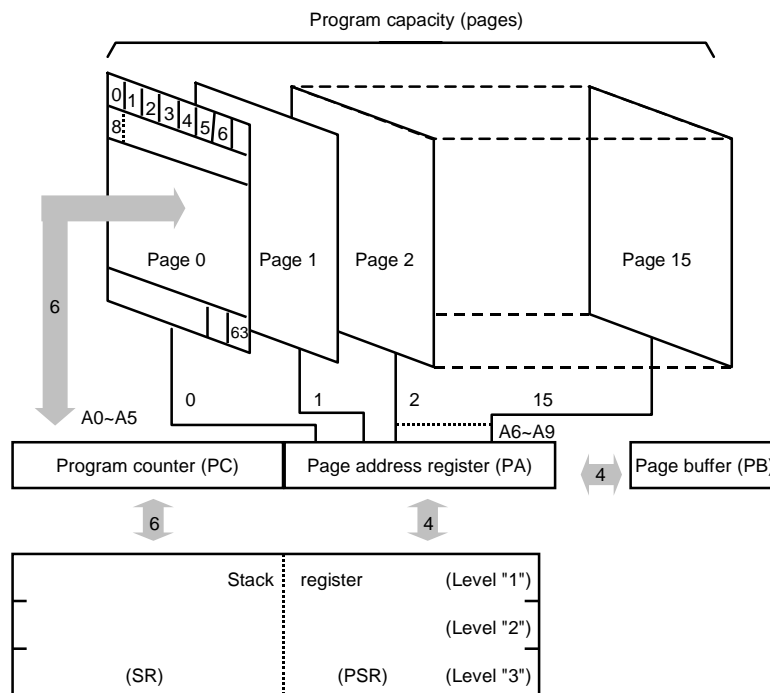


Fig 3-1 Configuration of Program Memory

Address Register

The following registers are used to address the ROM.

- Page address register (PA) :
Holds ROM's page number (0~Fh) to be addressed.
- Page buffer register (PB) :
Value of PB is loaded by an LPBI command when newly addressing a page.
Then it is shifted into the PA when rightly executing a branch instruction (BR) and a subroutine call (CAL).
- Program counter (PC) :
Available for addressing word on each page.
- Stack register (SR) :
Stores returned-word address in the subroutine call mode.

(1) Page address register and page buffer register :

Address one of pages #0 to #15 in the EPROM by the 4-bit binary counter. Unlike the program counter, the page address register is usually unchanged so that the program will repeat on the same page unless a page changing command is issued. To change the page address, take two steps such as (1) writing in the page buffer what page to jump (execution of LPBI) and (2) execution of BR or CAL, because instruction code is of eight bits so that page and word can not be specified at the same time.

In case a return instruction (RTN) is executed within the subroutine that has been called in the other page, the page address will be changed at the same time.

(2) Program counter :

This 6-bit binary counter increments for each fetch to address a word in the currently addressed page having an instruction to be next executed.

For easier programming, at turning on the power, the program counter is reset to the zero location. The PA is also set to "0". Then the program counter specifies the next address in random sequence.

When BR, CAL or RTN instructions are decoded, the switches on each step are turned off not to update the address. Then, for BR or CAL, address data are taken in from the instruction operands (a_0 to a_5), or for RTN, and address is fetched from stack register No. 1.

(3) Stack register :

This stack register provides two stages each for the program counter (6bits) and the page address register (4bits) so that subroutine nesting can be made on two levels.

Data Memory (RAM)

Up to 32 nibbles (16 words × 2pages × 4bits) is incorporated for storing data. The whole data memory area is indirectly specified by a data pointer (X,Y). Page number is specified by zero bit of X register, and words in the page by 4 bits in Y-register. Data memory is composed in 16 nibbles/page. Figure 4-2 shows the configuration.

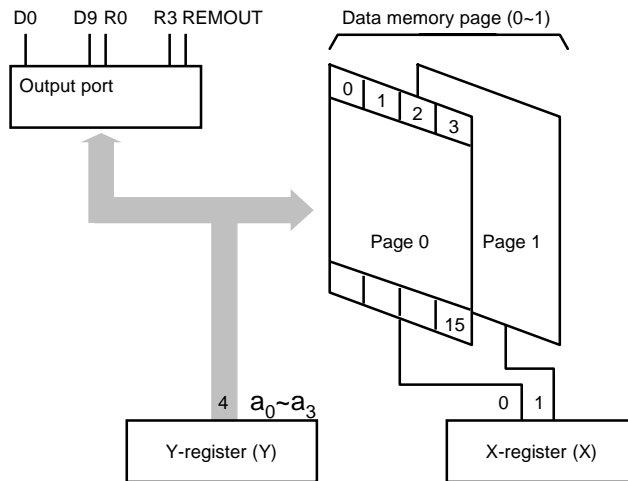


Fig 3-2 Composition of Data Memory

X-register (X)

X-register is consist of 2bit, X0 is a data pointer of page in the RAM, X1 is reserved.

	X1=0	X1=1
Y=0	D0	Reserved
Y=1	D1	Reserved

Table 3-1 Mapping table between X and Y register

Y-register (Y)

Y-register has 4 bits. It operates as a data pointer or a general-purpose register. Y-register specifies an address ($a_0 \sim a_3$) in a page of data memory, as well as it is used to specify an output port. Further it is used to specify a mode of carrier signal outputted from the REMOUT port. It can also be treated as a general-purpose register on a program.

Accumulator (A_{CC})

The 4-bit register for holding data and calculation results.

Arithmetic and Logic Unit (ALU)

In this unit, 4bits of adder/comparator are connected in parallel as it's main components and they are combined with status latch and status logic (flag.)

(1) Operation circuit (ALU) :

The adder/comparator serves fundamentally for full addition and data comparison. It executes subtraction by making a complement by processing an inversed output of A_{CC} (A_{CC}+1)

(2) Status logic :

This is to bring an ST, or flag to control the flow of a program. It occurs when a specified instruction is executed in three cases such as overflow or underflow in operation and two inputs unequal.

State Counter (SC)

A fundamental machine cycle timing chart is shown below. Every instruction is one byte length. Its execution time is the same. Execution of one instruction takes 6 clocks for fetch cycle and 6 clocks for execute cycle (12 clocks in total). Virtually these two cycles proceed simultaneously, and thus it is apparently completed in 6 clocks (one machine cycle). Exceptionally BR, CAL and RTN instructions is normal execution time since they change an addressing sequentially. Therefore, the next instruction is prefetched so that its execution is completed within the fetch cycle.

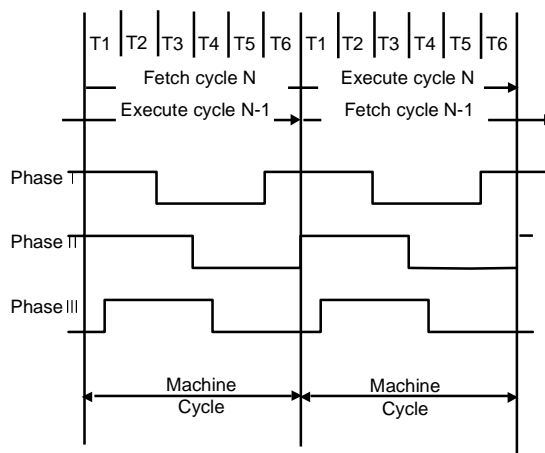


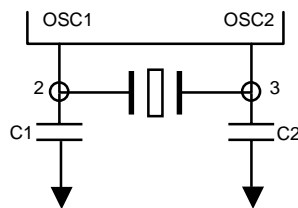
Fig. 3-3 Fundamental timing chart

Clock Generator

The HMS38112/39112 have an internal clock oscillator. The oscillator circuit is designed to operate with an external ceramic resonator.

Oscillator circuit is able to organize by connecting ceramic resonator to outside.

* It is necessary to connect capacitor to outside in order to change ceramic resonator, you must refer to a manufacturer`s resonator matching guide.

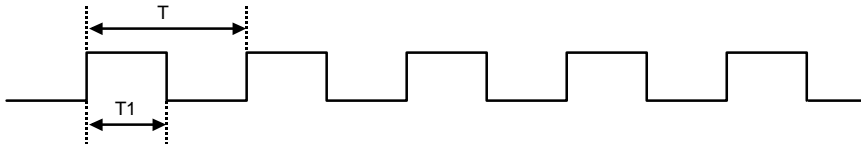


HMS 38112	3.64MHz	4.00MHz
MURATA	CSTLS3M64G56-B0	CSTLS3M64G56-B0
CORETECH	CRTL3.64MR	CRTL4.00MR
TDK	FCR3.64MC5	FCR4.0MC5

* All type have the built-in loading capacitors.

Pulse Generator

The following frequency and duty ratio are selected for carrier signal outputted from the REMOUT port depending on a PMR (Pulse Mode Register) value set in a program.



PMR	REMOUT signal	
0	$T=1/f_{PUL} = 96/f_{OSC}$,	$T1/T = 1/2$
1	$T=1/f_{PUL} = 96/f_{OSC}$,	$T1/T = 1/3$
2	$T=1/f_{PUL} = 64/f_{OSC}$,	$T1/T = 1/2$
3	$T=1/f_{PUL} = 64/f_{OSC}$,	$T1/T = 1/4$
4	$T=1/f_{PUL} = 88/f_{OSC}$,	$T1/T = 4/11$
5	No Pulse (same to D0 ~ D9)	
6	$T=1/f_{PUL} = 96/f_{OSC}$,	$T1/T = 1/4$
7	No pulse (same to D0 ~ D9)	

* Default value is "0"

Table 3-2 PMR selection table

Reset Operation

HMS38112/39112 have three reset sources. One is a built-in Power-on reset circuit, another is a built-in Low VDD Detection circuit, the other is the overflow of Watch Dog Timer (WDT). All reset operations are internal in the HMS38112.

Built-in Power On Reset Circuit

HMS38112/39112 has a built-in Power-on reset circuit consisting of an about $1\text{M}\Omega$ Resistor and a 3pF Capacitor. When the Power-on reset pulse occurs, system reset signal is latched and WDT is cleared. After the overflow time of WDT (2^{13} x System clock time), system reset signal is released.

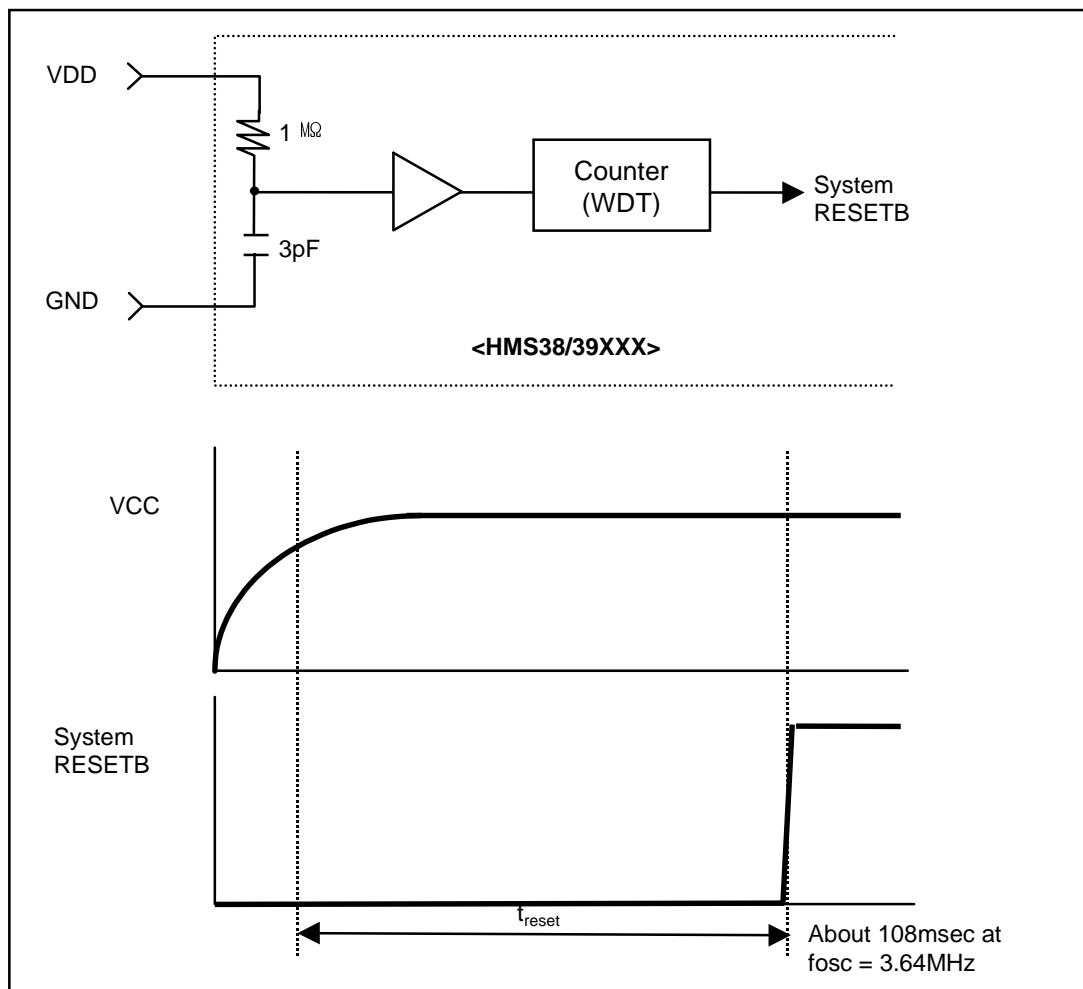


Fig. 3-4 Power-On Reset Circuit and Timing Chart

Built-in Low VDD Reset Circuit

HMS38112/39112 have a Low VDD detection circuit.

If VDD become Reset Voltage of Low VDD Detection circuit at a active status, system reset occur and WDT is cleared.

After VDD is increased upper Reset Voltage again, WDT is re-counted and if WDT is overflowed, system reset is released.

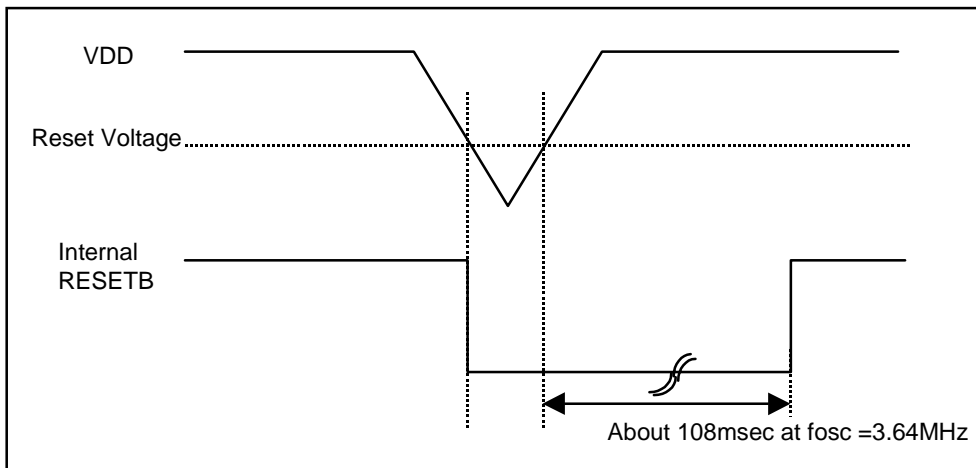


Fig. 3-5 Low Voltage Detection diagram

Watch Dog Timer (WDT)

Watch dog timer is organized binary of 14 steps. The signal of $f_{OSC}/48$ cycle comes in the first step of WDT after WDT reset. If this counter was overflowed, reset signal automatically come out so that internal circuit is initialized.

The overflow time is $8 \times 6 \times 2^{13}/f_{OSC}$ (108.026ms at $f_{OSC} = 3.64\text{MHz}$)

Normally, the binary counter must be reset before the overflow by using reset instruction (WDTR), Power-on reset pulse or Low VDD detection pulse.

* It is constantly reset in STOP mode. When STOP is released, counting is restarted. (Refer to STOP Operation>)

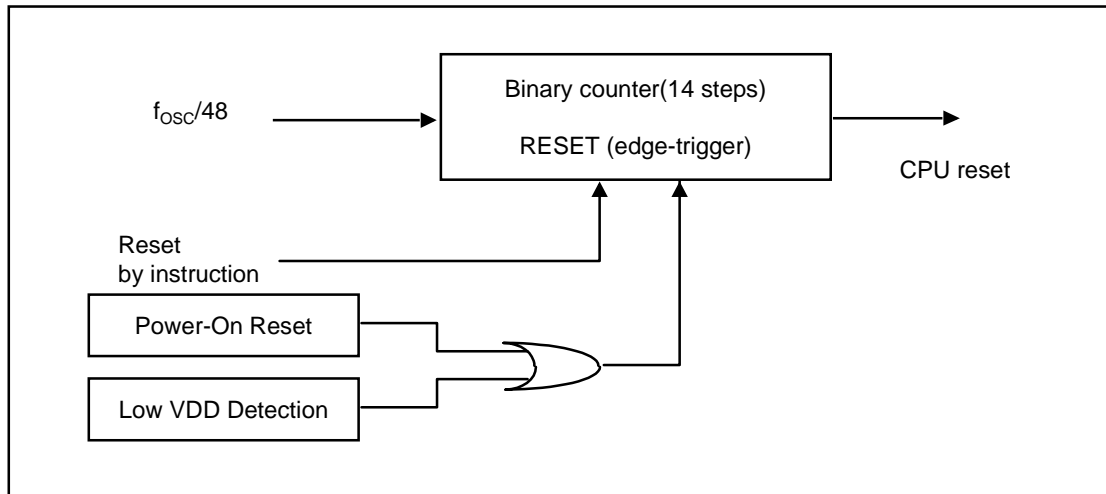


Fig 3-6 Block Diagram of Watch-dog Timer

STOP Operation

Stop mode can be achieved by STOP instructions.

In stop mode :

1. Oscillator is stopped, the operating current is low.
2. Watch dog timer is reset, D0~D3 output and REMOUT output are "L" .
3. Part other than WDT, D0~D3 output and REMOUT output have a value before come into stop mode.

Stop mode is released when one of K or R input is going to "L".

1. State of D0~D3 output and REMOUT output is return to state of before stop mode is achieved.
2. After $2^{10} \times$ System clock time for stable oscillating, first instruction start to operate.
3. In return to normal operation, WDT is counted from zero again.

But, at executing stop instruction, if one of K or R input is chosen to "L", stop instruction is same to NOP instruction.

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CHAPTER 4. Instruction

INSTRUCTION FORMAT

All of the 43 instruction in HMS38112/39112 is format in two fields of OP code and operand which consist of eight bits. The following formats are available with different types of operands.

*Format I

All eight bits are for OP code without operand.

*Format II

Two bits are for operand and six bits for OP code.

Two bits of operand are used for specifying bits of RAM and X-register (bit 1 and bit 7 are fixed at "0")

*Format III

Four bits are for operand and the others are OP code.

Four bits of operand are used for specifying a constant loaded in RAM or Y-register, a comparison value of compare command, or page addressing in ROM.

*Format IV

Six bits are for operand and the others are OP code.

Six bits of operand are used for word addressing in the ROM.

Chapter 4. Instruction

INSTRUCTION TABLE

The HMS38112/39112 provides the following 43 basic instructions.

	Category	Mnemonic	Function	ST ¹
1	Register to Register	LAY	$A \leftarrow Y$	S
2		LYA	$Y \leftarrow A$	S
3		LAZ	$A \leftarrow 0$	S
4	RAM to Register	LMA	$M(X,Y) \leftarrow A$	S
5		LMAIY	$M(X,Y) \leftarrow A, Y \leftarrow Y+1$	S
6		LYM	$Y \leftarrow M(X,Y)$	S
7		LAM	$A \leftarrow M(X,Y)$	S
8		XMA	$A \leftrightarrow M(X,Y)$	S
9	Immediate	LYI i	$Y \leftarrow i$	S
10		LMIIY i	$M(X,Y) \leftarrow i, Y \leftarrow Y+1$	S
11		LXI n	$X \leftarrow n$	S
12	RAM Bit Manipulation	SEM n	$M(n) \leftarrow 1$	S
13		REM n	$M(n) \leftarrow 0$	S
14		TM n	TEST $M(n) = 1$	E
15	ROM Address	BR a	if $ST = 1$ then Branch	S
16		CAL a	if $ST = 1$ then Subroutine call	S
17		RTN	Return from Subroutine	S
18		LPBI i	$PB \leftarrow i$	S
19	Arithmetic	AM	$A \leftarrow A + M(X,Y)$	C
20		SM	$A \leftarrow M(X,Y) - A$	B
21		IM	$A \leftarrow M(X,Y) + 1$	C
22		DM	$A \leftarrow M(X,Y) - 1$	B
23		IA	$A \leftarrow A + 1$	S
24		IY	$Y \leftarrow Y + 1$	C
25		DA	$A \leftarrow A - 1$	B

	Category	Mnemonic	Function	ST ^{*1}
26	Arithmetic	DY	$Y \leftarrow Y - 1$	B
27		EORM	$A \leftarrow A \oplus M(X,Y)$	S
28		NEGA	$A \leftarrow \bar{A} + 1$	Z
29	Comparison	ALEM	TEST $A \leq M(X,Y)$	E
30		ALEI i	TEST $A \leq i$	E
31		MNEZ	TEST $M(X,Y) \neq 0$	N
32		YNEA	TEST $Y \neq A$	N
33		YNEI i	TEST $Y \neq i$	N
34		KNEZ	TEST $K \neq 0$	N
35		RNEZ	TEST $R \neq 0$	N
36	Input / Output	LAK	$A \leftarrow K$	S
37		LAR	$A \leftarrow R$	S
38		SO	Output(Y) \leftarrow 1 at HMS39112, 0 at HMS38112	S
39		RO	Output(Y) \leftarrow 0 at HMS39112, 1 at HMS39112	S
40	Control	WDTR	Watch Dog Timer Reset	S
41		STOP	Stop operation	S
42		LPY	$PMR \leftarrow Y$	S
43		NOP	No operation	S

Note) i = 0~f, n = 0~3, a = 6bit PC Address

*1 Column ST indicates conditions for changing status. Symbols have the following meanings

- S : On executing an instruction, status is unconditionally set.
- C : Status is only set when carry or borrow has occurred in operation.
- B : Status is only set when borrow has not occurred in operation.
- E : Status is only set when equality is found in comparison.
- N : Status is only set when equality is not found in comparison.
- Z : Status is only set when the result is zero.

Port Operation

Value of X-reg	Value of Y-reg	Operation
0 or 1	0 ~ 6	SO : D(Y) ← 1(High-Z) RO : D(Y) ← 0
0 or 1	8	REMOUT port repeats "H" and "L" in pulse frequency. (When PMR = 5, it is fixed at "H") SO : REMOUT(PMR) ← 1 at HMS39112, 0 at HMS38112 RO : REMOUT(PMR) ← 0 at HMS39112, 1 at HMS38112
0 or 1	9	SO : D0 ~ D6 ← 1 (High-Z) RO : D0 ~ D6 ← 0
0 or 1	C ~ D	SO : R(Y-Ah) ← 1 RO : R(Y-Ah) ← 0
0 or 1	E	SO : R2 ~ R3 ← 1 RO : R2 ~ R3 ← 0
0 or 1	F	SO : D0 ~ D6 ← 1(High-Z), R2 ~ R3 ← 1 RO : D0 ~ D6 ← 0, R2 ~ R3 ← 0

DETAILS OF INSTRUCTION SYSTEM

All 43 basic instructions of the HMS38112/39112 are one by one described in detail below.

Description Form

Each instruction is headlined with its mnemonic symbol according to the instructions table given earlier.

Then, for quick reference, it is described with basic items as shown below. After that, detailed comment follows.

- Items :

- Naming : Full spelling of mnemonic symbol
- Status : Check of status function
- Format : Categorized into I to IV
- Operand : Omitted for Format I
- Function

(1) LAY

Naming : Load Accumulator from Y-Register
Status : Set
Format : I
Function : $A \leftarrow Y$
<Comment> Data of four bits in the Y-register is unconditionally transferred to the accumulator. Data in the Y-register is left unchanged.

(2) LYA

Naming : Load Y-register from Accumulator
Status : Set
Format : I
Function : $Y \leftarrow A$
<Comment> Load Y-register from Accumulator

(3) LAZ

Naming : Clear Accumulator
Status : Set
Format : I
Function : $A \leftarrow 0$
<Comment> Data in the accumulator is unconditionally reset to zero.

(4) LMA

Naming : Load Memory from Accumulator
Status : Set
Format : I
Function : $M(X,Y) \leftarrow A$
<Comment> Data of four bits from the accumulator is stored in the RAM location addressed by the X-register and Y-register. Such data is left unchanged.

(5) LMAIY

Naming : Load Memory from Accumulator and Increment Y-Register
Status : Set
Format : I
Function : $M(X,Y) \leftarrow A, Y \leftarrow Y+1$
<Comment> Data of four bits from the accumulator is stored in the RAM location addressed by the X-register and Y-register. Such data is left unchanged.

(6) LYM

Naming : Load Y-Register form Memory
 Status : Set
 Format : I
 Function : $Y \leftarrow M(X,Y)$
 <Comment> Data from the RAM location addressed by the X-register and Y-register is loaded into the Y-register. Data in the memory is left unchanged.

(7) LAM

Naming : Load Accumator from Memory
 Status : Set
 Format : I
 Function : $A \leftarrow M(X,Y)$
 <Comment> Data from the RAM location addressed by the X-register and Y-register is loaded into the Y-register. Data in the memory is left unchanged.

(8) XMA

Naming : Exchanged Memory and Accumulator
 Status : Set
 Format : I
 Function : $M(X,Y) \leftrightarrow A$
 <Comment> Data from the memory addressed by X-register and Y-register is exchanged with data from the accumulator. For example, this instruction is useful to fetch a memory word into the accumulator for operation and store current data from the accumulator into the RAM. The accumulator can be restored by another XMA instruction.

(9) LYI i

Naming : Load Y-Register from Immediate
 Status : Set
 Format : III
 Operand : Constant $0 \leq i \leq 15$
 Function : $Y \leftarrow i$
 <Purpose> To load a constant in Y-register. It is typically used to specify Y-register in a particular RAM word address, to specify the address of a selected output line, to set Y-register for specifying a carrier signal outputted from OUT port, and to initialize Y-register for loop control. The accumulator can be restored by another XMA instruction.
 <Comment> Data of four bits from operand of instruction is transferred to the Y-register.

(10) LMIIY i

Naming : Load Memory from Immediate and Increment Y-Register
Status : Set
Format : III
Operand : Constant $0 \leq i \leq 15$
Function : $M(X,Y) \leftarrow i, Y \leftarrow Y + 1$
<Comment> Data of four bits from operand of instruction is stored into the RAM location addressed by the X-register and Y-register. Then data in the Y-register is incremented by one.

(11) LXI n

Naming : Load X-Register from Immediate
Status : Set
Format : II
Operand : X file address $0 \leq n \leq 3$
Function : $X \leftarrow n$
<Comment> A constant is loaded in X-register. It is used to set X-register in an index of desired RAM page. Operand of 1 bit of command is loaded in X-register.

(12) SEM n

Naming : Set Memory Bit
Status : Set
Format : II
Operand : Bit address $0 \leq n \leq 3$
Function : $M(X,Y,n) \leftarrow 1$
<Comment> Depending on the selection in operand of operand, one of four bits is set as logic 1 in the RAM memory addressed in accordance with the data of the X-register and Y-register.

(13) REM n

Naming : Reset Memory Bit
Status : Set
Format : II
Operand : Bit address $0 \leq n \leq 3$
Function : $M(X,Y,n) \leftarrow 0$
<Comment> Depending on the selection in operand of operand, one of four bits is set as logic 0 in the RAM memory addressed in accordance with the data of the X-register and Y-register.

(14) TM n

Naming : Test Memory Bit
 Status : Comparison results to status
 Format : II
 Operand : Bit address $0 \leq n \leq 3$
 Function : $M(X,Y,n) \leftarrow 1?$
 $ST \leftarrow 1$ when $M(X,Y,n)=1$, $ST \leftarrow 0$ when $M(X,Y,n)=0$
 <Purpose> A test is made to find if the selected memory bit is logic. 1
 Status is set depending on the result.

(15) BR a

Naming : Branch on status 1
 Status : Conditional depending on the status
 Format : IV
 Operand : Branch address a (Addr)
 Function : When $ST = 1$, $PA \leftarrow PB$, $PC \leftarrow a(Addr)$
 When $ST = 0$, $PC \leftarrow PC + 1$, $ST \leftarrow 1$
 Note : PC indicates the next address in a fixed sequence that is actually pseudo-random count.
 <Purpose> For some programs, normal sequential program execution can be change.
 A branch is conditionally implemented depending on the status of results obtained by executing the previous instruction.
 <Comment>

- Branch instruction is always conditional depending on the status.
 - a. If the status is reset (logic 0), a branch instruction is not rightly executed but the next instruction of the sequence is executed.
 - b. If the status is set (logic 1), a branch instruction is executed as follows.
- Branch is available in two types - short and long. The former is for addressing in the current page and the latter for addressing in the other page. Which type of branch to execute is decided according to the PB register. To execute a long branch, data of the PB register should in advance be modified to a desired page address through the LPBI instruction.

(17) RTN

Naming : Return from Subroutine
 Status : Set
 Format : |
 Function : $PC \leftarrow SR1$ $PA, PB \leftarrow PSR1$
 $SR1 \leftarrow SR2$ $PSR1 \leftarrow PSR2$
 $SR2 \leftarrow SR3$ $PSR2 \leftarrow PSR3$
 $SR3 \leftarrow SR3$ $PSR3 \leftarrow PSR2$
 $ST \leftarrow 1$

<Purpose> Control is returned from the called subroutine to the calling program.

<Comment> Control is returned to its home routine by transferring to the PC the data of the return address that has been saved in the stack register (SR1).
 At the same time, data of the page stack register (PSR1) is transferred to the PA and PB.

(18) LPBI i

Naming : Load Page Buffer Register from Immediate
 Status : Set
 Format : III
 Operand : ROM page address $0 \leq i \leq 15$
 Function : $PB \leftarrow i$

<Purpose> A new ROM page address is loaded into the page buffer register (PB).
 This loading is necessary for a long branch or call instruction.

<Comment> The PB register is loaded together with three bits from 4 bit operand.

(19) AM

Naming : Add Accumulator to Memory and Status 1 on Carry
 Status : Carry to status
 Format : |
 Function : $A \leftarrow M(X,Y)+A, ST \leftarrow 1(\text{when total} > 15),$
 $ST \leftarrow 0(\text{when total} \leq 15)$

<Comment> Data in the memory location addressed by the X and Y-register is added to data of the accumulator. Results are stored in the accumulator. Carry data as results is transferred to status. When the total is more than 15, a carry is caused to put "1" in the status. Data in the memory is not changed.

(23) IA

Naming : Increment Accumulator
Status : Set
Format : |
Function : $A \leftarrow A+1$
<Comment> Data of the accumulator is incremented by one. Results are returned to the accumulator.
A carry is not allowed to have effect upon the status.

(24) IY

Naming : Increment Y-Register and Status 1 on Carry
Status : Carry to status
Format : |
Function : $Y \leftarrow Y + 1$ $ST \leftarrow 1$ (when $Y = 15$)
 $ST \leftarrow 0$ (when $Y < 15$)
<Comment> Data of the Y-register is incremented by one and results are returned to the Y-register.
Carry data as results is transferred to the status. When the total is more than 15, the status is set.

(25) DA

Naming : Decrement Accumulator and Status 1 on Borrow
Status : Carry to status
Format : |
Function : $A \leftarrow A - 1$ $ST \leftarrow 1$ (when $A \geq 1$)
 $ST \leftarrow 0$ (when $A = 0$)
<Comment> Data of the accumulator is decremented by one. As a result (by addition of Fh), if a borrow is caused, the status is reset to "0" by logic. If the data is more than one, no borrow occurs and thus the status is set to "1".

(36) LAK

Naming : Load Accumulator from K
 Status : Set
 Format : |
 Function : $A \leftarrow K$
 <Comment> Data on K are transferred to the accumulator

(37) LAR

Naming : Load Accumulator from R
 Status : Set
 Format : |
 Function : $A \leftarrow R$
 <Comment> Data on R are transferred to the accumulator

(38) SO

Naming : Set Output Register Latch
 Status : Set
 Format : |
 Function : $D(Y) \leftarrow 1$ $0 \leq Y \leq 7$
 $REMOUT \leftarrow 1(PMR=5)$ $Y = 8$
 $D0\sim D9 \leftarrow 1$ (High-Z) $Y = 9$
 $R(Y) \leftarrow 1$ $Ah \leq Y \leq Dh$
 $R \leftarrow 1$ $Y = Eh$
 $D0\sim D9, R \leftarrow 1$ $Y = Fh$

<Purpose> A single D output line is set to logic 1, if data of Y-register is between 0 to 7.
 Carrier frequency come out from REMOUT port, if data of Y-register is 8.
 All D output line is set to logic 1, if data of Y-register is 9.
 It is no operation, if data of Y-register between 10 to 15.
 When Y is between Ah and Dh, one of R output lines is set at logic 1.

<Comment> When Y is Eh, the output of R is set at logic 1.
 When Y is Fh, the output D0~D9 and R are set at logic 1.
 Data of Y-register is between 0 to 7, selects appropriate D output.
 Data of Y-register is 8, selects REMOUT port.
 Data of Y-register is 9, selects all D port.
 Data in Y-register, when between Ah and Dh, selects an appropriate R output (R0~R3).
 Data in Y-register, when it is Eh, selects all of R0~R3.
 Data in Y-register, when it is Fh, selects all of D0~D9 and R0~R3.

(39) RO

Naming : Reset Output Register Latch

Status : Set

Format :

Function :
D(Y) ← 0 0 ≤ Y ≤ 7
REMOUT ← 0 Y = 8
D0~D9 ← 0 Y = 9
R(Y) ← 0 Ah ≤ Y ≤ Dh
R ← 0 Y = Eh
D0~D9, R ← 0 Y = Fh

<Purpose> A single D output line is set to logic 0, if data of Y-register is between 0 to 9.
REMOUT port is set to logic 0, if data of Y-register is 9.
All D output line is set to logic 0, if data of Y-register is 9.
When Y is between Ah and Dh, one of R output lines is set at logic 0.

When Y is Eh, the output of R is set at logic 0
When Y is Fh, the output D0~D9 and R are set at logic 1.

<Comment> Data of Y-register is between 0 to 7, selects appropriate D output.
Data of Y-register is 8, selects REMOUT port.
Data of Y-register is 9, selects D port.
Data in Y-register, when between Ah and Dh, selects an appropriate R output (R0~R3).
Data in Y-register, when it is Eh, selects all of R0~R3.
Data in Y-register, when it is Fh, selects all of D0~D9 and R0~R3.

(40) WDTR

Naming : Watch Dog Timer Reset

Status : Set

Format :

Function : Reset Watch Dog Timer (WDT)

<Purpose> Normally, you should reset this counter before overflowed counter for dc watch dog timer. this instruction controls this reset signal.

(41) STOP

Naming : STOP
Status : Set
Format : |
Function : Operate the stop function
<Purpose> Stopped oscillator, and little current.
(See 1-12 page, STOP function.)


(42) LPY

Naming : Pulse Mode Set
Status : Set
Format : |
Function : $PMR \leftarrow Y$
<Comment> Selects a pulse signal outputted from REMOUT port.

(43) NOP

Naming : No Operation
Status : Set
Format : |
Function : No operation

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Guideline for S/W

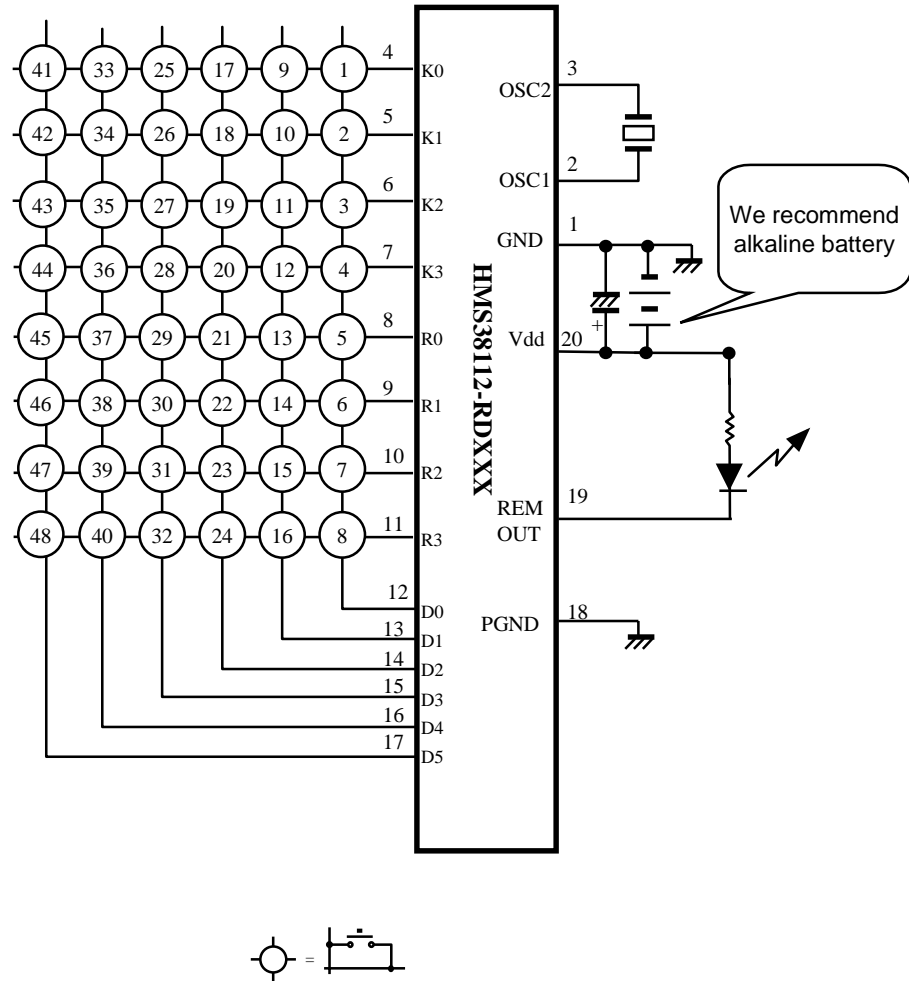
1. All rams need to be initialized to zero in reset address for proper design.
2. Make the output ports `H` after reset.
3. Do not use WDTR instruction in subroutine.
4. Before reading the input port the waiting time should be more than 200uS.
5. To decrease current consumption, make the output port as high in normal routine except for key scan strobe and STOP mode.
6. We recommend you do not use all 64 bytes in a page. You had better write `BR \$` in unused area. This will help you prevent unusual operation of MCU.
7. Be careful not to use long call or branch (CALL,BL) with arithmetic manipulation.
If you want to use branch right after arithmetic manipulation, the long call or branch will be against your intention.

ex) LAR ; The value of R ports -> Accumulator
ALEI 14 ; A ≤ 14 : S = 1, A > 14 : S = 0
BL TRUE ; S is always 1 because BL is composed of LPBI and BR.
----- Fail

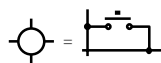
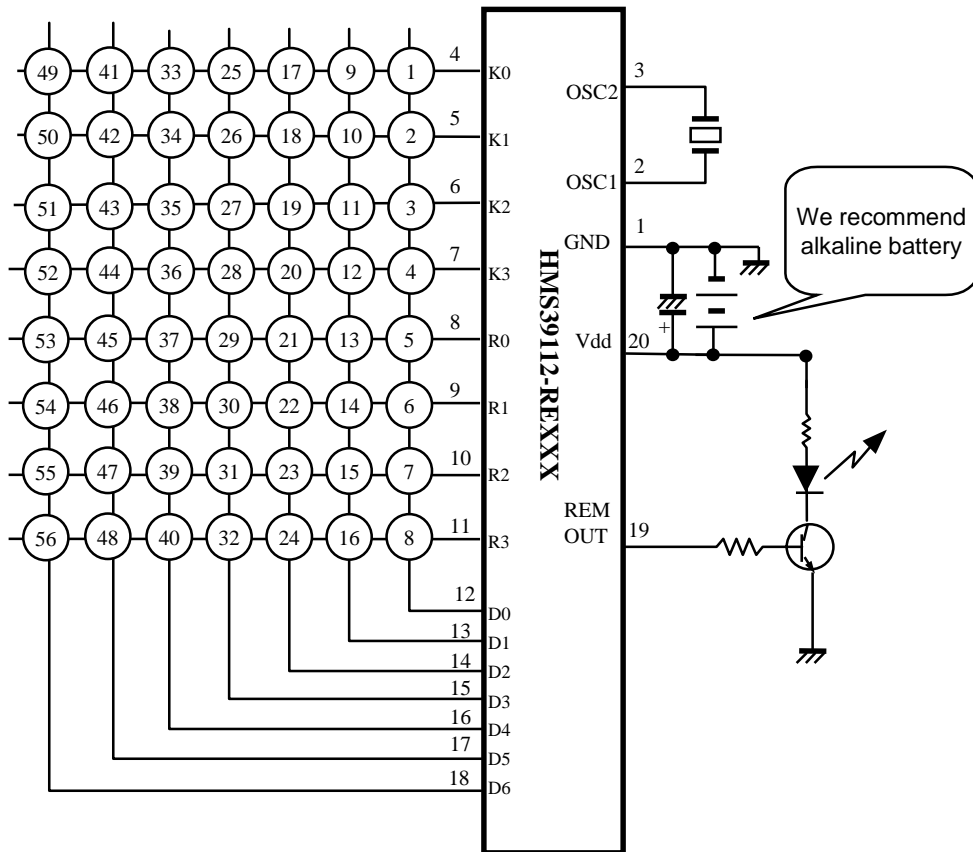
LAR ; The value of R ports -> Accumulator
ALEI 14 ; A ≤ 14 : S = 1, A > 14 : S = 0
BR TRUE ; When S is 1 Branch will occur. Otherwise Branch will not occur and
LAK ; next instruction will be operated.
----- Right

Chapter 5. Application

HMS38112 Circuit Diagram



HMS39112 Circuit Diagram



Chapter 5. Application

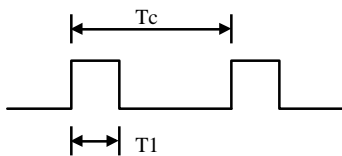
Truth Table for example program

CUSTOM:04H

KEY NO.	DATA(H)	KEY NO.	DATA(H)
K01	00	K29	1 C
K02	01	K30	1 D
K03	02	K31	1 E
K04	03	K32	1 F
K05	04	K33	20
K06	05	K34	21
K07	06	K35	22
K08	07	K36	23
K09	08	K37	24
K10	09	K38	25
K11	0A	K39	26
K12	0B	K40	27
K13	0C	K41	28
K14	0D	K42	29
K15	0E	K43	2A
K16	0F	K44	2B
K17	10	K45	2C
K18	11	K46	2D
K19	12	K47	2E
K20	13	K48	2F
K21	14	K49	30
K22	15	K50	31
K23	16	K51	32
K24	17	K52	33
K25	18	K53	34
K26	19	K54	35
K27	1A	K55	36
K28	1B	K56	37

Output waveform of uPD6121G

A single pulse, modulated with 37.917KHz signal at 3.64MHz



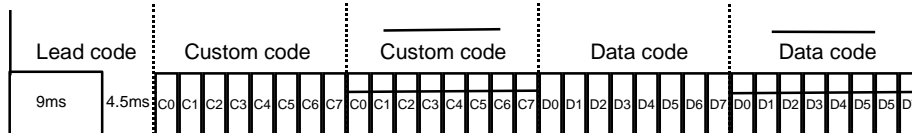
Carrier frequency

$$f_{CAR} = 1/Tc = f_{OSC}/96$$

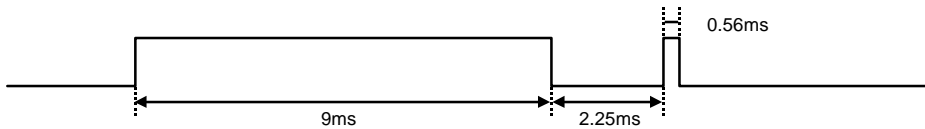
$$\text{Duty ratio} = T1/Tc = 1/3$$

- Configuration of Flame

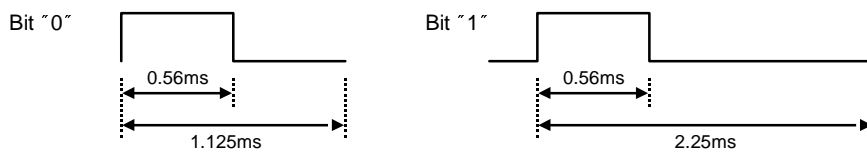
1st flame



- Repeat code

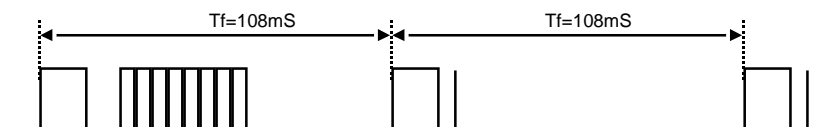


- Bit Description



- Flame Interval : Tf

The transmitted waveform as long as a key is depressed



Chapter 5. Application

Example program - uPD6121G

```
                INCLUDE GMS30K.LIB
:-----:
:          99.9.8
:          This program is example program for GMS39112 BY Hee Jin RYU
:          The format is NEC format
:-----:
:          RAM DEFINE
:          X=0
COUNT         EQU          00
NONE           EQU          00          ;BIT DEFINE
FIRST         EQU          01
REPEAT        EQU          02
INDAT         EQU          01
TOTLKY        EQU          02
POINT         EQU          03
STROBE        EQU          04
CC6L          EQU          06
CC6H          EQU          07
CC7L          EQU          08
CC7H          EQU          09
NEWDTL        EQU          10
NEWDTH        EQU          11
KEYDTL        EQU          12
KEYDTH        EQU          13
OLDL          EQU          14
OLDH          EQU          15
:-----:
:          PG          00
:-----:
RST           LXI          0
              LYI          15          ;RAM CLEAR
CLA           LMIIY
              YNEI          15
              BR            CLA
              LYI          15
              SO
TORO          LYI          6          ; MAKE STROBE PORT LOW BEFORE STOP MODE
              RO
              DY
              BR            TORO
              CALL          TIM10          ; FOR STABLIZATION PORT
              STOP

MAIN         LXI          0
              LYI          15          ;ALL PORT HIGH FOR DECREASING CURRENT CONSUMPTION
              SO
              LYI          COUNT
              LMIIY
KEY          LYI          1
              LPY
              LYI          COUNT
              REM          FIRST
              REM          NONE
SCAN        LYI          INDAT
              LMIIY          15
CLR         LMIIY          0
              YNEI          KEYDTL
              BR            CLR
              CALL          SCAN1
              WDTR          ; DON'T USE WDTR IN SUBROUTINE
              LYI          TOTLKY
              MNEZ
              BR            KEY11
              LYI          COUNT
              TM            NONE
              BR            RST
              SEM          NONE
              BR            SCAN
KEY11       LYM
              YNEI          1
              BR            MAIN
              BL            KEY12
```

Chapter 5. Application

```

DTCOM      CAL      COMPARE1
           ALEI      0
           BR        DTCOM1
           BL        TIM11
DTCOM1     DY
           CAL      COMPARE1
           ALEI      0
           BR        DATAC
           BR        RRTN
DATAC      LYI      0
           RTN
COMPARE1   LAM
           IY
           IY
           EORM
RRTN       RTN

           NOP
           BR        $          : END ADDRESS
:-----
           PG        01
:-----
           BR        $          : START ADDRESS
SCAN1     LYI      POINT
           LYM
           RO
           CALL     TIM30      : DELAY FOR KEY SCAN
           LAK
           ALEI     14
           CAL      KSAVE
           LAR
           ALEI     14
           CAL      RSAVE
           LYI     15
           SO
           LYI      POINT
           IM
           LMA
           ALEI     6
           BR        SCAN1
           RTN

KSAVE     NOP
           BR        SAVE
RSAVE     LYI      NEWDTL
           SEM      2
SAVE      LYI      INDAT
           LMAIY
           IM
           LMAIY
           LAM
           LYI      STROBE
           LMA
           RTN

COUN      LYI      COUNT
           TM       FIRST
           BR       KEY25
           SEM      FIRST

KEY26     LYI      NEWDTL
           CALL     DTMOVE
           LYI      2
           CALL     DLY65M
           BL       SCAN

KEY25     LYI      NEWDTL
           CALL     DTCOM
           YNEI     0
           BR       KEY26

```

Chapter 5. Application

```

        LYI      KEYDTL
        CALL    DTCOM
        YNEI    0
        BR      KEY31

KEY 32  LYI      KEYDTL
        CALL    DTMOVE
        BL      CUSREAD

KEY 31  LYI      COUNT
        REM     REPEAT
        BR      KEY32

        NOP
        BR      $
;-----
        PG      02
;-----
        BR      $

KEY 12  LYI      STROBE
        TM      0
        BR      LOOPA
        NOP
        BR      LOOPB
LOOPA   LYI      NEWDTL
        SEM     3
LOOPB   LYI      STROBE
        LAM
        LYI      NEWDTH

        ALEI    1
        BR      NT0
        ALEI    3
        BR      NT1
        ALEI    5
        BR      NT2
        LMIIY   3
        BR      CNVE

NT0     LMIIY   0
        CALL    TIM04
        BR      CNVE

NT1     LMIIY   1
        NOP
        NOP
        BR      CNVE

NT2     LMIIY   2
        NOP

CNVE    LYI      INDAT
        LAM
        LYI      0
        ALEI    6
        BR      DWKEY
        ALEI    7
        BR      CON4      ; 3
        ALEI    10
        BR      DWKEY
        ALEI    11
        BR      CON3      ; 2
        ALEI    12
        BR      DWKEY
        ALEI    13
        BR      CON2      ; 1
        ALEI    14
        BR      CONV      ; 0

DWKEY   BL      MAIN
CON4    IY
CON3    CALL    TIM03
        IY
        CALL    TIM03

```

```

CON2      IY
          NOP
CONV      LAY
          LYI      NEWDTL
          AM
          LMA
          BL      COUN
          NOP
          BR      $
-----
          PG      03
-----
          BR      $
CUSREAD   LYI      CC6L
          LMIY     4
          LMIY     0
          LMIY     11
          LMIY     15
CUSCOM    LYI      NEWDTL
          CALL     BAR      :Y=NEWDTL
          LYI      8
          SO      :HEAD
          LYI      9
          CALL     DLY65M
          CALL     TIM27
          LYI      8
          RO      :HEAD RO
          LYI      1
          CALL     DLY65M
          CALL     TIM29
          LYI      COUNT
          TM      REPEAT
          BR      HD1
FULCOD    LYI      1
          CALL     DLY65M
          CALL     TIM34
          LYI      POINT
          LMIY     CC6L
          BL      TX
HD1       CALL     PULSE0
          LYI      10
          CAL      DLY65M
          CAL      DLY65M
          CAL      DLY65M
          WDTR
          CAL      DLY65M
          CAL      DLY65M
          CALL     TIM52
          BL      DDLY1
DLY65M    CALL     TIM63
DLY65M1   DY
          BR      DLY65M
          RTN
          IA      :UNUSED INSTRUCTION IS WRITTEN IN BLANK AREA
          DA
          LAY
          LYA
          LAZ
          XMA
          KNEZ
          RNEZ
          ALEM
          NOP
          BR      $
-----
          PG      04
-----

```

Chapter 5. Application

```

PULSE      BR      $
PULSE0     CALL    TIM05
           LYI     8
           SO
           CALL    TIM41
           RO
           LYI     POINT
           LYM
           BL      TIM31

HGHOULT    CALL    TIM60
           BL      TIM25

TX         CAL     PULSE0
           TM      0
           CAL     HGHOULT
           CAL     PULSE
           TM      1
           CAL     HGHOULT
           CAL     PULSE
           TM      2
           CAL     HGHOULT
           CAL     PULSE
           TM      3
           CAL     HGHOULT
           LYI     POINT
           IM
           LMA
           ALE1    13
           BR      TX

ENDTX      CAL     PULSE0
           WDTR
           LYI     COUNT
           SEM     REPEAT
           LYI     9
           CALL    DLY65M
           CALL    TIM33
DDL1       LYI     0
           CALL    DLY65M
           CALL    DLY65M
           CALL    TIM54
           BL      KEY

bar        cal     bar1
bar1       im
           nega
COMPART    IY
           IY
           LMA
           DY
           RTN

DTMOVE     CAL     DTMOVE1
DTMOVE1    LAM
           BR      COMPART

           NOP
           BR      $
;-----
           PG      05
;-----
           BR      $

TIM65      NOP
TIM64      NOP
TIM63      NOP
TIM62      NOP
TIM61      NOP
TIM60      NOP
TIM59      NOP
TIM58      NOP

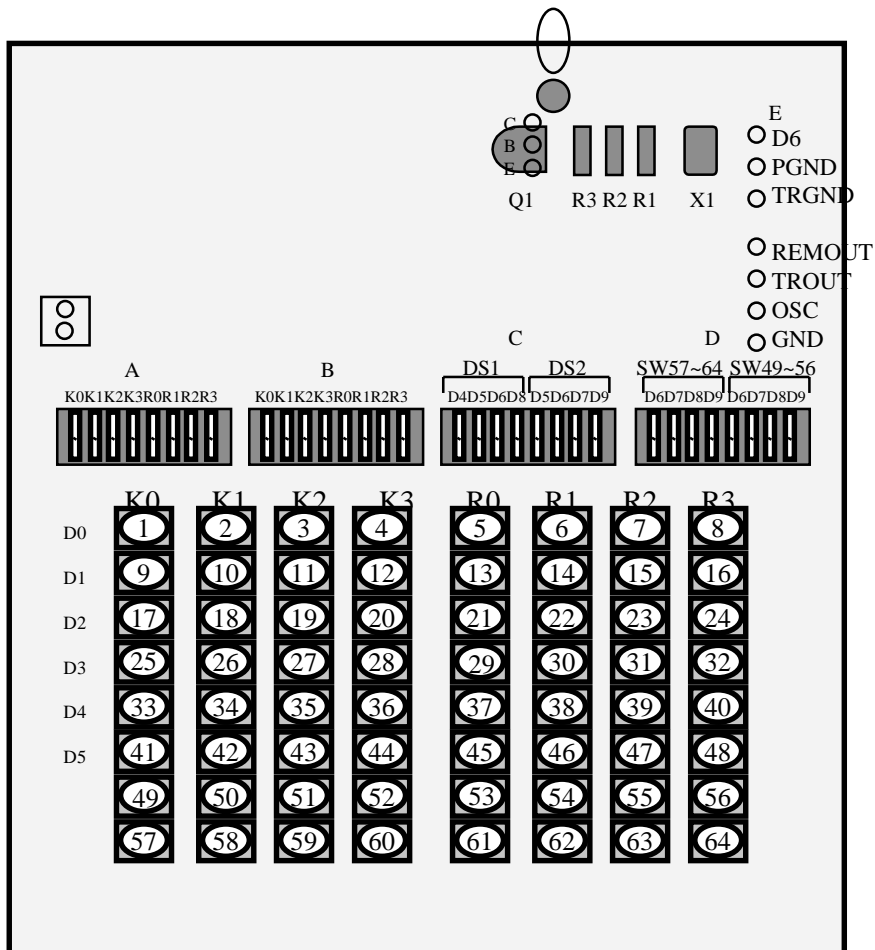
```

TIM57 NOP
TIM56 NOP
TIM55 NOP
TIM54 NOP
TIM53 NOP
TIM52 NOP
TIM51 NOP
TIM50 NOP
TIM49 NOP
TIM48 NOP
TIM47 NOP
TIM46 NOP
TIM45 NOP
TIM44 NOP
TIM43 NOP
TIM42 NOP
TIM41 NOP
TIM40 NOP
TIM39 NOP
TIM38 NOP
TIM37 NOP
TIM36 NOP
TIM35 NOP
TIM34 NOP
TIM33 NOP
TIM32 NOP
TIM31 NOP
TIM30 NOP
TIM29 NOP
TIM28 NOP
TIM27 NOP
TIM26 NOP
TIM25 NOP
TIM24 NOP
TIM23 NOP
TIM22 NOP
TIM21 NOP
TIM20 NOP
TIM19 NOP
TIM18 NOP
TIM17 NOP
TIM16 NOP
TIM15 NOP
TIM14 NOP
TIM13 NOP
TIM12 NOP
TIM11 NOP
TIM10 NOP
TIM09 NOP
TIM08 NOP
TIM07 NOP
TIM06 NOP
TIM05 NOP
TIM04 NOP
TIM03 RTN

Chapter 5. Application

HMS38112 TEST B/D Example

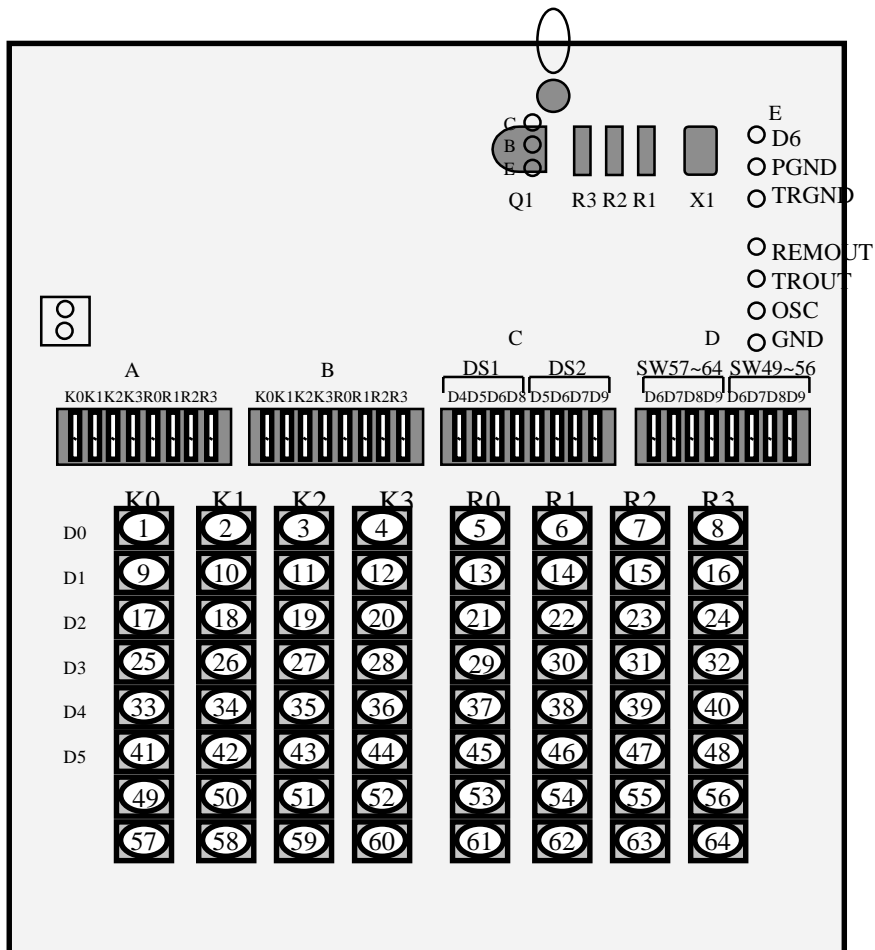
1. Attach resonator to X1
2. Connect base and collector at Q1
3. Connect PGND and TRGND with jumper at E



- * DS1 is connected to A. If D6 switch is on among DS1, A becomes D6 port.
- * DS2 is connected to B. If D7 switch is on among DS2, B becomes D7 port.
- * If D6 switch among SW49~SW56 is on at D, the key 49~56 can be used as D6 port.
- * If D7 switch among SW57~SW64 is on at D, the key 57~64 can be used as D7 port.
- * note : the position of SW49~56 and SW57~64 in B/D is changed. The reference position is right.
- * If you want to increase the remote controller valid distance, you try to disconnect R2 resistor and lessen R1 resistor.

HMS39112 TEST B/D Example

1. Attach resonator to X1
2. Attach 2222A transistor to Q1
3. Connect PGND and D6 with jumper at E
4. Attach about 150Ω to R3.



- * DS1 is connected to A. If D6 switch is on among DS1, A becomes D6 port.
- * DS2 is connected to B. If D7 switch is on among DS2, B becomes D7 port.
- * If D6 switch among SW49~SW56 is on at D, the key 49~56 can be used as D6 port.
- * If D7 switch among SW57~SW64 is on at D, the key 57~64 can be used as D7 port.
- * note : the position of SW49~56 and SW57~64 in B/D is changed. The reference position is right.
- * If you want to increase the remote controller valid distance, you try to disconnect R2 resistor and lessen R1 resistor.

