HMS39C7092

32-bit Embedded Flash MCU

On-Chip Flash Memory Programming Guide

ver 1.0

MagnaChip

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Contents

Figures

Tables

Chapter 1

Algorithms for On-chip Flash Memory

1.1 Programming and Erasing Internal Flash Memory

A software method, using the CPU, is employed to program and erase flash memory in the on-board programming modes. There are five flash memory operation modes: normal read mode, pre-program/program mode, erase mode, pre-program/program-verify mode, and erase verify mode. The transitions to these modes are made by setting FMCR register.
The flash memory cannot be read while being programmed or erased. Therefore, the program (user program) that controls flash memory program/erase should be located and executed in on-chip RAM or external memory.

1.1.1 Program and Program-Verify Mode

When writing data or programs to flash memory, the program flowchart shown in ***Figure 1.1*** should be followed. Flash Memory of HMS39C7092 can be programmed 16 bits at one time. In Program Verify, the data written in program mode is read to check whether it has been correctly written in the flash memory. If result of verify read at a certain address is not same as the progammed data of this address, progam must be retried to the time when Verify read result and the progammed data are matched.
However, if the program/program verify sequence is repeated **N_PGM**† times and verify read result is not same as programmed data, it is program fail.

†Refer to the Table 3.3 On-chip Flash programming parameters

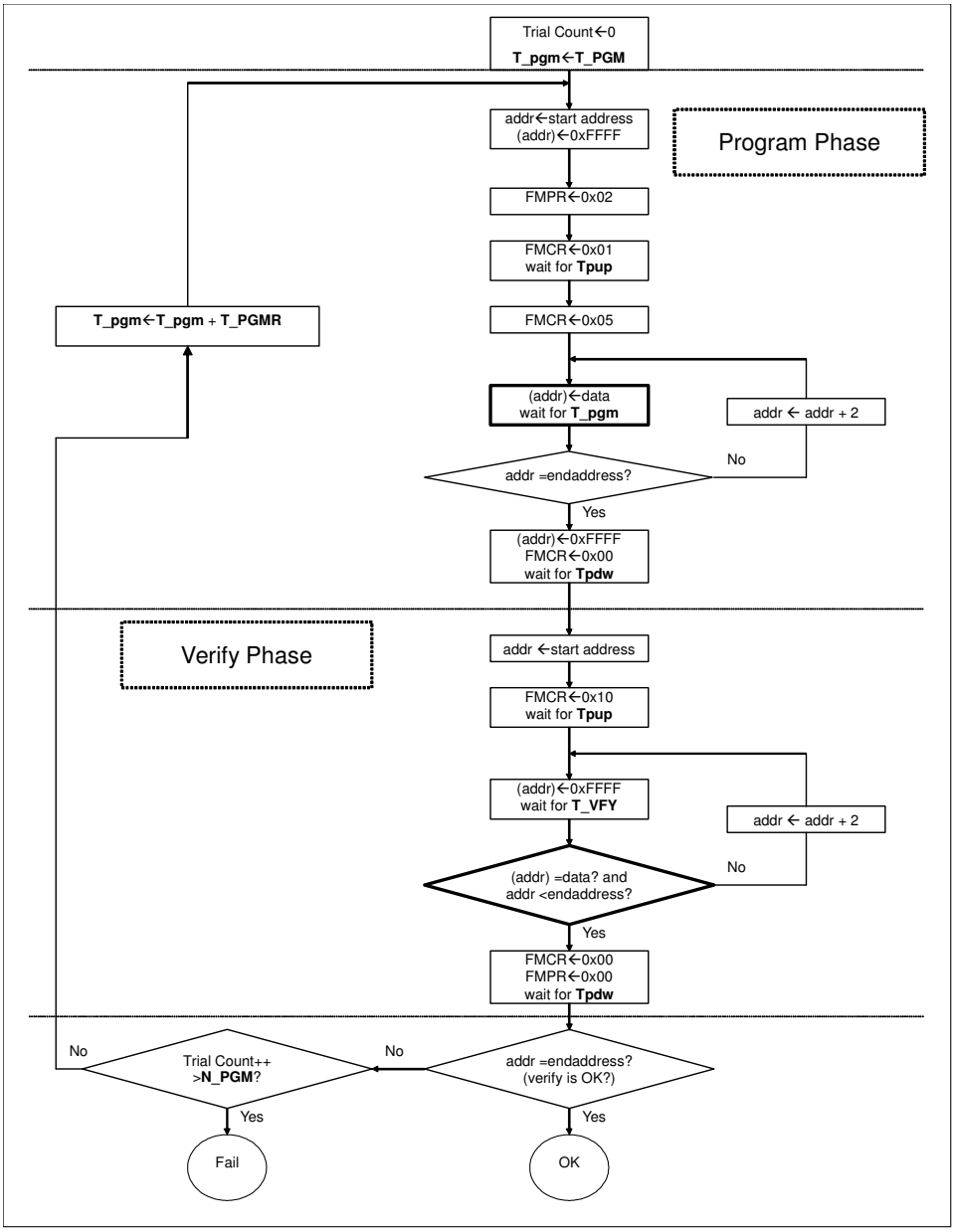

Figure 1.1 Flash Program & Program Verify Sequence

1.1.2 Preprogram and Preprogram-Verify Mode

This is the first step of flash memory erase algorithm. Pre-program & Pre-program Verify must be done before block erase.

The difference between Program and Pre-program is that the purpose of Pre-program is programming not-programmed cell in a certain block that will be erased. Due to Pre-programming before block erase, every cell in the block that will be erased goes to program state , so it is possible to prevent cell from being over-erased after block erase.

When Pre-program mode, program address must start at first address of block to be erased, and increase by 2 to the last address of that block.

The relation between each erase sector and corresponding flash memory address is shown at the ***Table 2.3*** of chapter 2.1.2.

Pre-program needs to do pre-program verify read to ensure that every cell in the block are programmed successfully.

The FMCR setting are the same as program & program verify mode.

The Flow of pre-program and pre-program verify is shown at ***Figure 1.2***

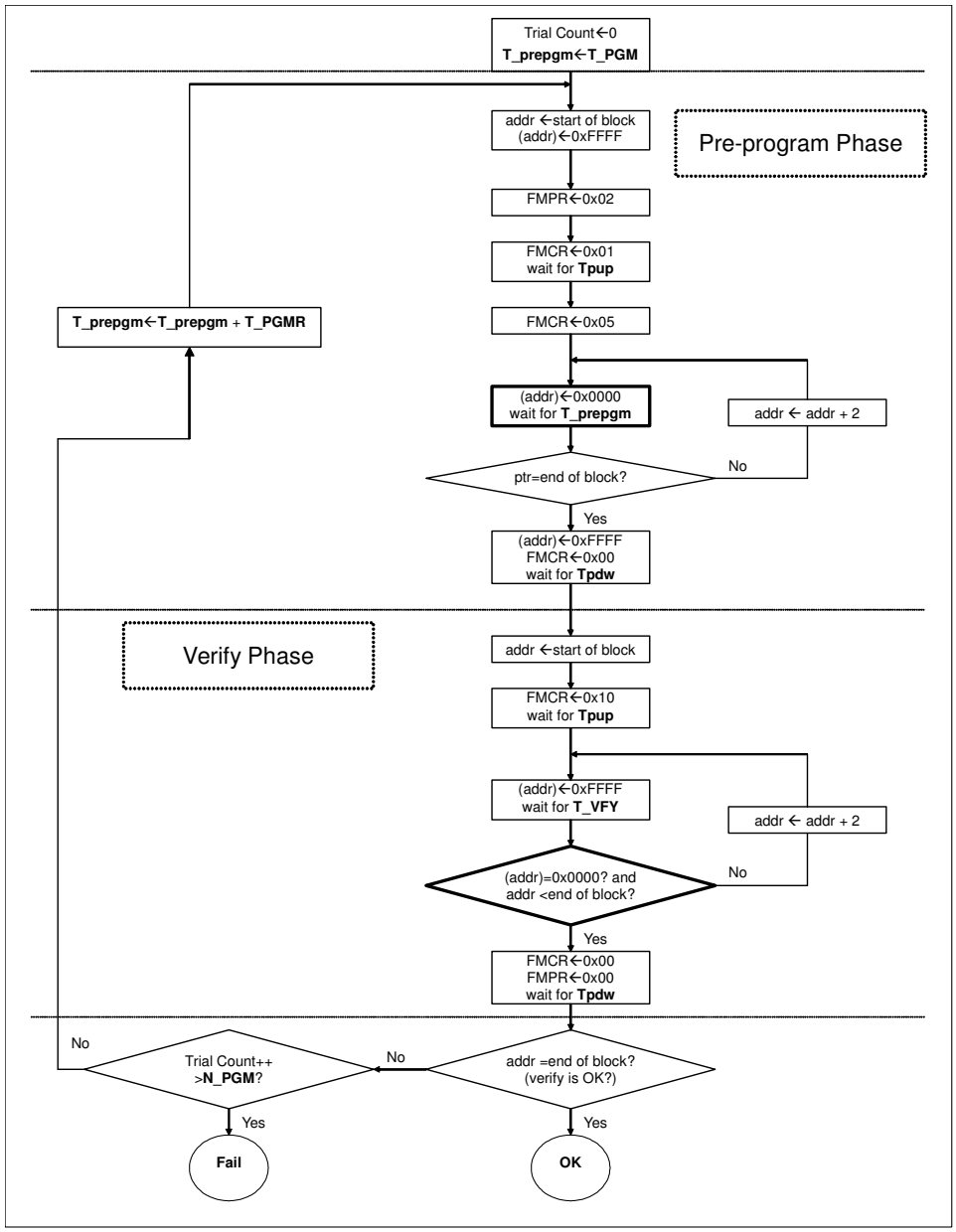

Figure 1.2 Flash Pre-program & Pre-program Verify Sequence

1.1.3 Erase and Erase-Verify Mode

Flash memory erase operation are performed block by block. To erase flash memory, make a setting for the flash memory area to be erased in erase sector register(FESR). If multiple bits of FESR register are set, multiple sectors are erased at one time. The Maximum number of blocks that can be erased at one time is four. After Erase, it is necessary to do Erase verify read to ensure that every cell in the block are erased successively. When Erase verify read mode, verify address must start at first address of block to be erased, and increase by 2 to the last address of that block. The relation between each erase sector and corresponding flash memory address is shown at the ***Table 2.3*** of chapter 2.1.2.

If the result of verify read at a certain address is not 0xFFFF, erase must be retried until the result of Verify read is 0xFFFF. However, if the erase/erase verify sequence is repeated **N_ERASE**† times and the result of verify read is not 0xFFFF, device is erase fail.

The Flow of erase and erase verify is shown at ***Figure 1.3***.

※CAUSION: It is very important not to exceed maximum erase time - Over-Erase. Extreme Over-Erase may destroy the internal flash cells for ever.

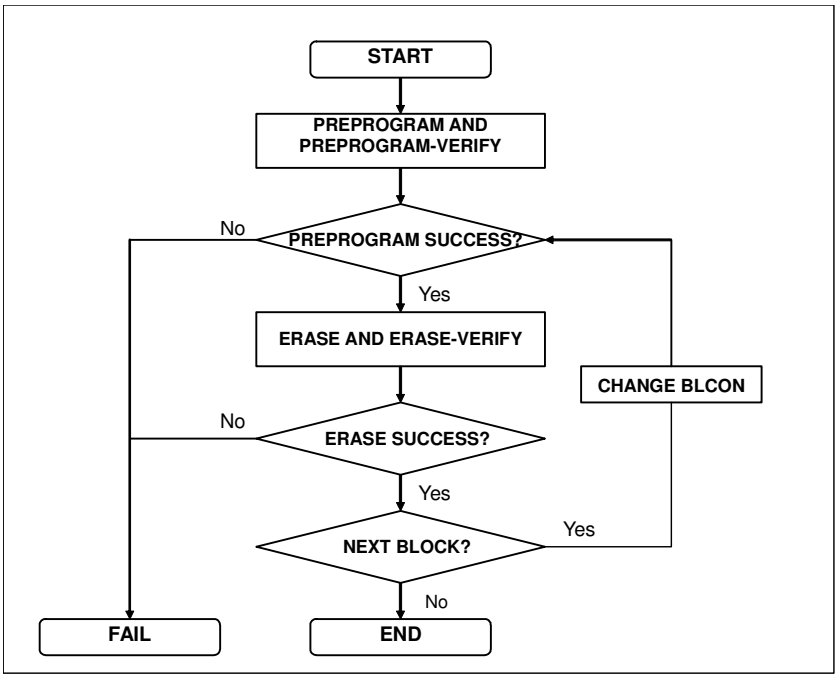

Figure 1.3 Flash Erase Algorithm

†Refer to the Table 3.3 On-chip Flash programming parameters

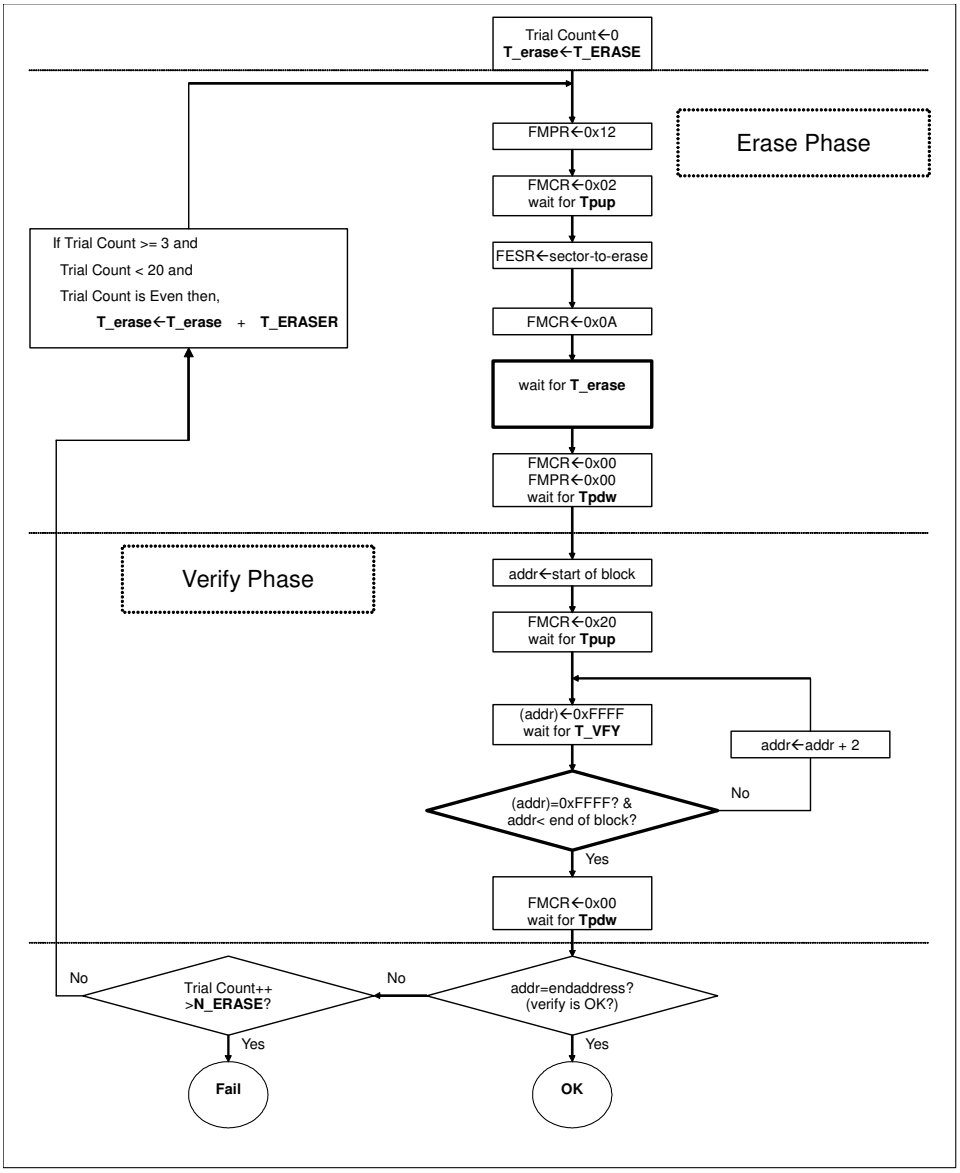

Figure 1.4 Flash Erase and Erase-Verify Sequence

Chapter 2

PROM Mode Interface

2.1 Flash Memory PROM Mode

The HMS39C7092 has a PROM mode as well as the on-board programming modes for programming and erase flash memory. In PROM mode, the on-chip flash memory can be programmed using a 7092 PROM writer.

2.1.1 PROM Mode Setting

Setting MD[2:0] to Mode 1 (001) make HMS39C7092 work as PROM. When PROM mode, Every pins of HMS39C7092 are assigned as PROM mode pins
By setting FR_SEL signal, internal register of flash memory are directly write or read through FD[15:0] as ***Table 2.1***. When value of FR_SEL[2:0] is set and FWEB = rising-edge, FD[15:0] signals are passed into the register that FR_SEL select. When value of FR_SEL[2:0] is set and FOEB is low, the register's value is read through the FD[15:0].
Table 2.2 shows how the different external pins are set to write and read internal register.

Table 2.1 FR_SEL Value for access to internal Register

FR_SEL[2:0]	Read	Write
000	Sense Data	reserved
001	FMAR	FMAR & FMDR
010	FMDR	reserved
011	FMCR	FMCR
100	FESR	FESR
101	FMPR	FMPR

Table 2.2 Setting for Register read/write

Register Mode	Pin Name					
	FRSTB	FCEB	FWEB	FOEB	FD	FA
Read	H	L	H	L	Read Data	Address
Write	H	L	↑	H	Write Data	Address

2.1.2 Memory Map

The memory map of PROM mode are shown at ***Table 2.3***
At PROM mode, on-chip flash is 96K x 16 memory. Therefore, In order to access very next 16bit data to the currently accessed address, address should be changed by '1'(not by '2'), Erase operation is performed by sector, and corresponding address of each sector are shown.

Table 2.3 Erase Sector Register

Sector No.	Sector Size	FA [17:1]	Internal Address
0	8KB (4K-word)	0x00000 ~ 0x00FFF	0x0800_0000
1	8KB (4K- word)	0x01000 ~ 0x01FFF	0x0800_2000
2	24KB (12K- word)	0x02000 ~ 0x04FFF	0x0800_4000
3	24KB (12K- word)	0x05000 ~ 0x07FFF	0x0800_A000
4	32KB (16K- word)	0x08000 ~ 0x0BFFF	0x0801_0000
5	32KB (16K- word)	0x0C000 ~ 0x0FFFF	0x0801_8000
6	32KB (16K- word)	0x10000 ~ 0x13FFF	0x0802_0000
7	32KB (16K- word)	0x14000 ~ 0x17FFF	0x0802_8000

2.1.3 PROM Mode Operation

Each flash memory operation, such as program, erase, read are made by writing and reading the flash memory internal register. ***Table 2.4*** shows different flash memory operation and register read/write sequence of each operation. Every operation except for memory normal read and erase, the 1'st and 2'nd cycles are deciding which operation will be performed, and 4'th cycle is setting flash memory address to be programmed and verified. Therefore, only 3'th cycle need to be repeated if another flash memory address is programmed or verified repeatedly after first address. At Erase operation, 3'rd and 4'th cycle have to be repeated.
At Verify read operation (Pre-Program/program Verify and erase verify), In order to get the result of verify read, it is necessary to execute memory normal read operation after 4'th cycle.

Table 2.4 Setting for Flash PROM read/write

Operation	1st Cycle			2nd Cycle			3rd Cycle			4th Cycle		
	FR_SEL	Dir	Addr / Data	FR_SEL	Dir	Addr / Data	FR_SEL	Dir	Addr / Data	FR_SEL	Dir	Addr / Data
Normal Read	000	R	RA / Din									
Program/ Pre-program	101	W	X / 02	011	W	X / 01	011	W	- / 05	001	W	WA / Dout
Erase	101	W	X / 12	011	W	X / 02	100	W	X / SN	011	W	X / 0A
Pre-program Verify	101	W	X / 02	011	W	X / 10	-	-	- / -	001	W	RA / Din
Erase Verify Read	101	W	X / 00	011	W	X / 20	-	-	- / -	011	W	RA / Din

*RA: Read Address WA: Write address Din: Read data Dout: Program data
X: don't care R: Read W: Write SN: Erase Sector Number(see ***Table 2.3***)

2.1.4 Timing Diagram and AC/DC Characteristics (preliminary)

This timing diagram follows the sequence that is shown on ***Table 3.2***.

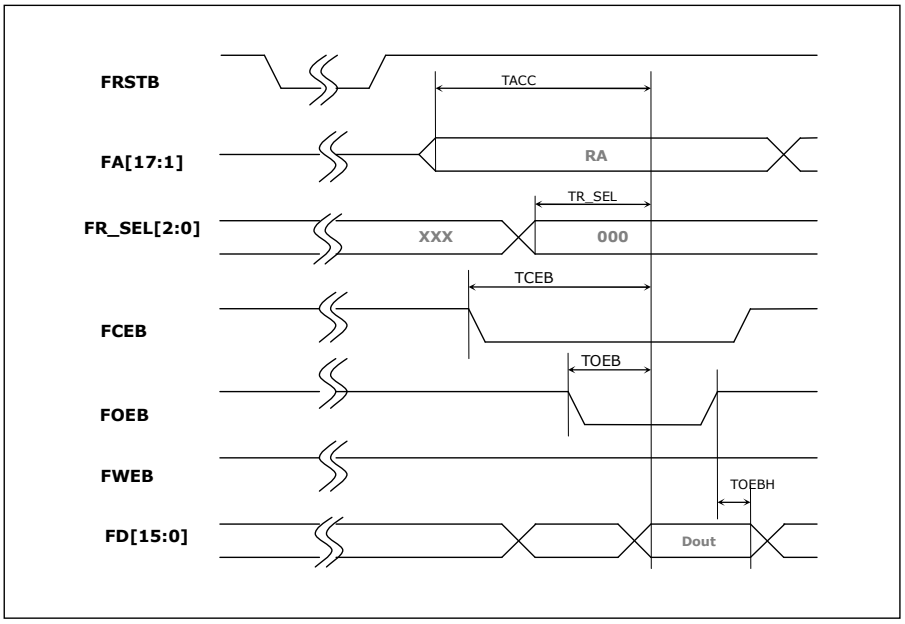

Figure 2.1 Timing Diagram of Read

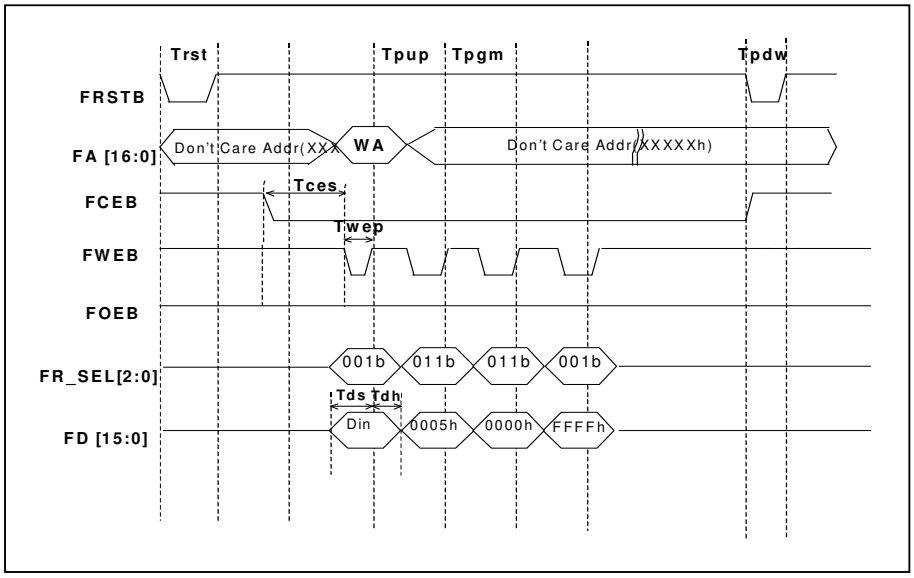

Figure 2.2 Timing Diagram of Pre-Program/Program

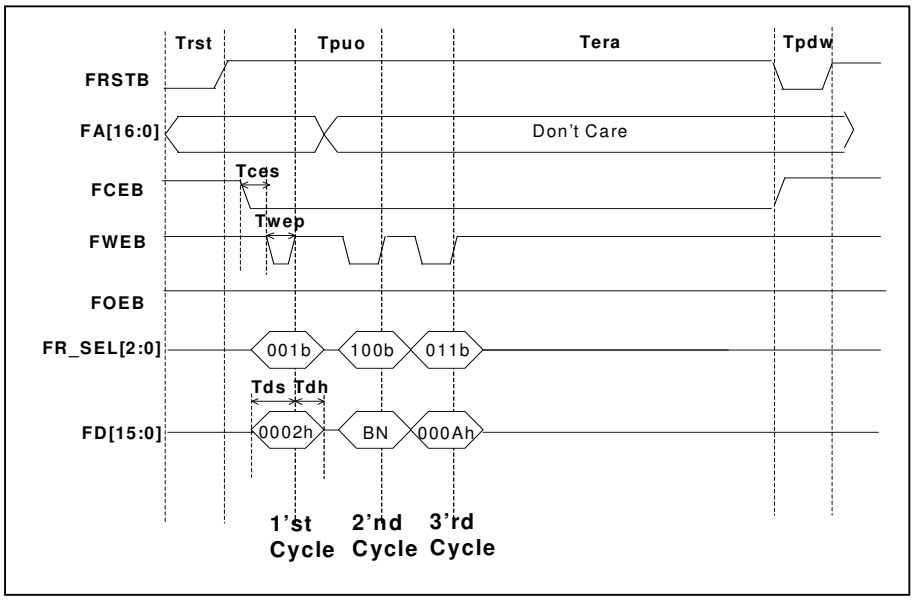

Figure 2.3 Timing Diagram of Erase

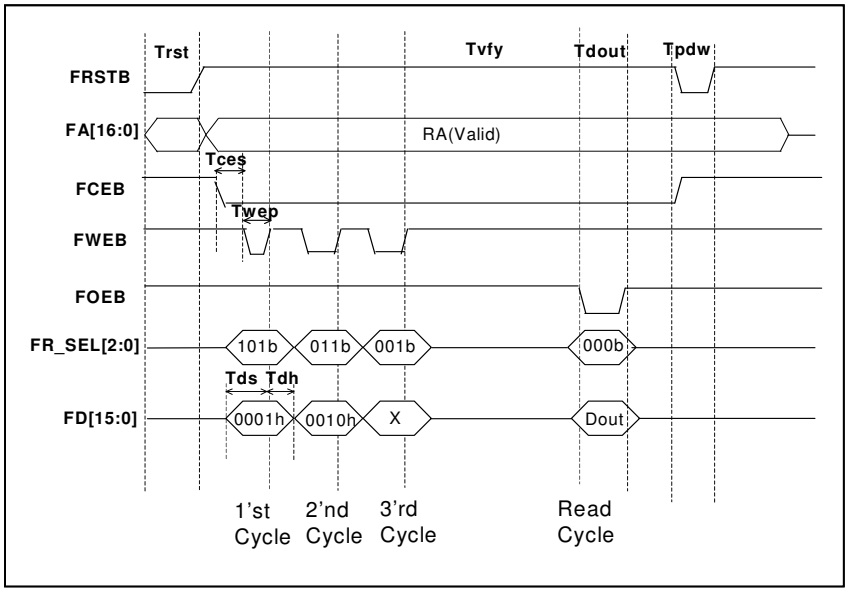

Figure 2.4 Timing Diagram of Pre-Program/Program Verify

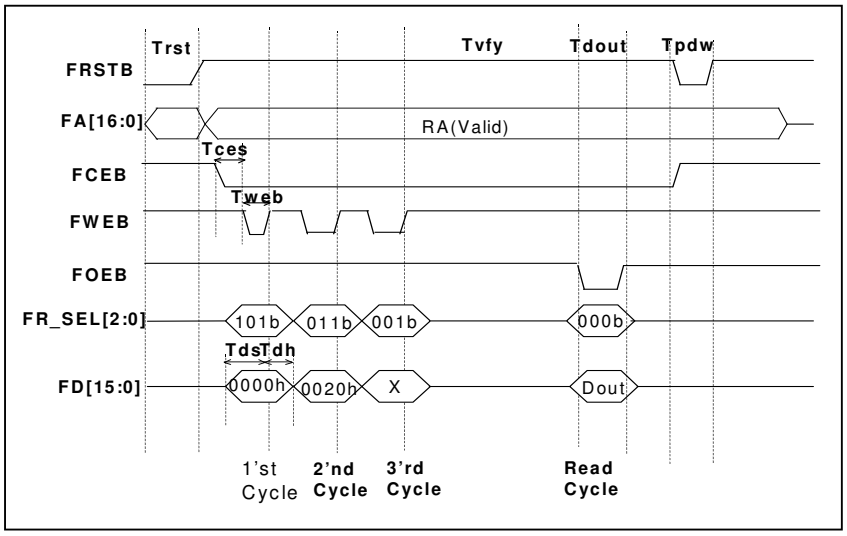

Figure 2.5 Timing Diagram of Erase Verify

Chapter 3

Electrical Characteristics and Operational Parameters

Table 3.1 DC Characteristics

(V_{DD} = 3.3V, Vss = 0V, FTVPPD = 5V, Ta = 25℃)

Items		Symbols	Min	Typ	Max	Units	Conditions
Input high voltage		Vih	0.7x V_{DD}	-	V_{DD} +0.5	V	
Input low voltage		Vil	-0.5	-	0.3x V_{DD}	V	
Output high voltage		Voh	2.4	-	-	V	Ioh=0.8mA
Output low voltage		Vol	-	-	0.4	V	Iol=0.8mA
Vcc current	Read	Idd	-	20	40	mA	
	Program	Idd	-	40	80	mA	
	Erase	Idd	-	25	50	mA	
FXTVPPD Current	Program	Ippd	-	10	20	mA	

Table 3.2 AC Characteristics

(V_{DD} = 3.3V, Vss = 0V, FTVPPD = 5V, Ta = 25℃)

Items	Symbols	Min	Typ	Max	Units
CEB output delay time	TCEB	-	90	130	ns
OEB output delay time	TOEB	-	5	10	ns
Output disable delay time	TOEBH	1	2	-	ns
R_SEL output delay time	TR_SEL	-	1	2	ns
Access time	TACC	-	90	130	ns
Reset Pulse Width	Trst	300	500	-	us
Power up time	Tpup	8	10	-	us
Discharge time(program,verify) Discharge time(erase)	Tpdw	1 10	10 20	-	us us
Program time	Tpgm	20	30	-	us
CEB Setup time	Tces	100	200	-	us
WEB Pulse Width	Twep	100	200	-	ns
WEB rise time	Tr	-	20	30	ns
WEB fall time	Tf	-	20	30	ns
Data Setup time	Tds	50	150	-	ns
Data Hold time	Tdh	50	80	-	ns
Erase time	Tera	100	500	10000	us
Verify Setup time	Tvfy	5	10	-	us
Verify Data out time	Tdout	90	-	-	ns

***Table* 3.3 Programing Parameters**

(V_{DD} = 3.3V, Vss = 0V, FXTVPPD = 5V, Ta = 25℃)

Items	Symbols	Min	Typ	Max	Units
program iteration	**N_PGM**	-	-	50	count
erase iteration	**N_ERASE**	-	-	50	count
program time	**T_PGM**	10	-	-	us
program retry time	**T_PGMR**	0	-	-	us
erase time	**T_ERASE**	100	-	10000	us
erase retry time	**T_ERASER**	100	-	1000	us
verify time	**T_VFY**	5	10	-	us