DDR3 SDRAM Unbuffered DIMMs
Based on 1Gb A version

HMT164U6AFP(R)6C
HMT112U6AFP(R)8C
HMT112U7AFP(R)8C
HMT125U6AFP(R)8C
HMT125U7AFP(R)8C

** Contents are subject to change without prior notice.

Revision History

Revision No.	History	Draft Date	Remark
0.01	Initial draft for internal review	Nov. 2007	Preliminary
0.02	Added IDD & Halogen-free products	Mar. 2008	Preliminary
0.1	Initial Specification Release. Corrected typo on package ball feature.	Dec 2008	

Table of Contents

1. Description

This Hynix unbuffered Dual In-Line Memory Module(DIMM) series consists of 1Gb A version. DDR3 SDRAMs in Fine Ball Grid Array(FBGA) packages on a 240 pin glass-epoxy substrate. This DDR3 Unbuffered DIMM series based on 1Gb A ver. provide a high performance 8 byte interface in 133.35mm width form factor of industry standard. It is suitable for easy interchange and addition.

1.1 Device Features & Ordering Information

1.1.1 Features

- VDD=VDDQ=1.5V
- VDDSPD=3.3V to 3.6V
- Fully differential clock inputs (CK, /CK) operation
- Differential Data Strobe (DQS, /DQS)
- On chip DLL align DQ, DQS and /DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10, and (11) supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- 8K refresh cycles /64ms
- DDR3 SDRAM Package: JEDEC standard 78ball FBGA(x4/x8), 96ball FBGA(x16) with support balls
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- Auto Self Refresh supported
- On Die Thermal Sensor supported (JEDEC optional)

1.1.2 Ordering Information

Part Name	Density	Org.	# of DRAMs	# of ranks	Materials	ECC	TS
HMT164U6AFP6C-S6/S5/G8/G7/H9/H8	512MB	64Mx64	4	1	Lead-free	None	No
HMT164U6AFR6C-S6/S5/G8/G7/H9/H8	512MB	64Mx64	4	1	Halogen-free	None	No
HMT112U6AFP8C-S6/S5/G8/G7/H9/H8	1GB	128Mx64	8	1	Lead free	None	No
HMT112U6AFR8C-S6/S5/G8/G7/H9/H8	1GB	128Mx64	8	1	Halogen-free	None	No
HMT112U7AFP8C-S6/S5/G8/G7/H9/H8	1GB	128Mx72	9	1	Lead free	ECC	Yes
HMT112U7AFR8C-S6/S5/G8/G7/H9/H8	1GB	128Mx72	9	1	Halogen-free	ECC	Yes
HMT125U6AFP8C-S6/S5/G8/G7/H9/H8	2GB	256Mx64	16	2	Lead free	None	No
HMT125U6AFR8C-S6/S5/G8/G7/H9/H8	2GB	256Mx64	16	2	Halogen-free	None	No
HMT125U7AFP8C-S6/S5/G8/G7/H9/H8	2GB	256Mx72	18	2	Lead free	ECC	Yes
HMT125U7AFR8C-S6/S5/G8/G7/H9/H8	2GB	256Mx72	18	2	Halogen-free	ECC	Yes

1.2 Speed Grade & Key Parameters

MT/S	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Unit
Grade	-S6	-S5	-G8	-G7	-H9	-H8	-P1	-P9	
tCK(min)	2.5		1.875		1.5		1.25		ns
CAS Latency	6	5	8	7	9	8	10	9	tCK
tRCD(min)	15	12.5	15	13.125	13.5	12	12.5	11.25	ns
tRP(min)	15	12.5	15	13.125	13.5	12	12.5	11.25	ns
tRAS(min)	37.5	37.5	37.5	37.5	36	36	35	35	ns
tRC(min)	52.5	50	52.5	50.625	49.5	48	47.25	46.25	ns
CL-tRCD-tRP	6-6-6	5-5-5	8-8-8	7-7-7	9-9-9	8-8-8	10-10-10	9-9-9	tCK

1.3 Address Table

	512MB	1GB	1GB	2GB	2GB
Organization	64M x 64	128M x 64	128M x 72	256M x 64	256M x 72
Refresh Method	8K/64ms	8K/64ms	8K/64ms	8K/64ms	8K/64ms
Row Address	A0-A12	A0-A13	A0-A13	A0-A13	A0-A13
Column Address	A0-A9	A0-A9	A0-A9	A0-A9	A0-A9
Bank Address	BA0-BA2	BA0-BA2	BA0-BA2	BA0-BA2	BA0-BA2
Page Size	2KB	1KB	1KB	1KB	1KB
# of Rank	1	1	1	2	2
# of Device	4	8	9	16	18

2. Pin Architecture

2.1 Pin Definition

Pin Name	Description	Pin Name	Description
A0–A13	SDRAM address bus	SCL	I^2C serial bus clock for EEPROM
BA0–BA2	SDRAM bank select	SDA	I^2C serial bus data line for EEPROM
$\overline{RAS}$	SDRAM row address strobe	SA0–SA2	I^2C slave address select for EEPROM
$\overline{CAS}$	SDRAM column address strobe	V_{DD}*	SDRAM core power supply
$\overline{WE}$	SDRAM write enable	V_{DDQ}*	SDRAM I/O Driver power supply
$\overline{S}0$–$\overline{S}1$	DIMM Rank Select Lines	$V_{REF}DQ$	SDRAM I/O reference supply
CKE0–CKE1	SDRAM clock enable lines	$V_{REF}CA$	SDRAM command/address reference supply
ODT0–ODT1	On-die termination control lines	V_{SS}	Power supply return (ground)
DQ0–DQ63	DIMM memory data bus	V_{DDSPD}	Serial EEPROM positive power supply
CB0–CB7	DIMM ECC check bits	NC	Spare pins (no connect)
DQS0–DQS8	SDRAM data strobes (positive line of differential pair)	TEST	Memory bus analysis tools (unused on memory DIMMS)
$\overline{DQS}0$–$\overline{DQS}8$	SDRAM data strobes (negative line of differential pair)	RESET	Set DRAMs to Known State
DM0–DM8	SDRAM data masks/high data strobes (x8-based x72 DIMMs)	V_{TT}	SDRAM I/O termination supply
CK0–CK1	SDRAM clocks (positive line of differential pair)	RFU	Reserved for future use
$\overline{CK}0$–$\overline{CK}1$	SDRAM clocks (negative line of differential pair)	-	-

***The V_{DD} and $V_{DD}Q$ pins are tied common to a single power-plane on these designs**

2.2 Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0–CK1 $\overline{CK0}$–$\overline{CK1}$	SSTL	Differential crossing	CK and $\overline{CK}$ are differential clock inputs. All the DDR3 SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is reference to the crossing of CK and $\overline{CK}$ (Both directions of crossing).
CKE0–CKE1	SSTL	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{S}$0–$\overline{S}$1	SSTL	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	SSTL	Active Low	$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (ALONG WITH $\overline{S}$) define the command being entered.
ODT0–ODT1	SSTL	Active High	When high, termination resistance is enabled for all DQ, DQS, $\overline{DQS}$ and DM pins, assuming this function is enabled in the Mode Register 1 (MR1).
V_{REF}DQ	Supply		Reference voltage for SSTL15 I/O inputs.
V_{REF}CA	Supply		Reference voltage for SSTL 15 command/address inputs.
V_{DD}Q	Supply		Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For all current DDR3 unbuffered DIMM designs, V_{DD}Q shares the same power plane as V_{DD} pins.
BA0–BA2	SSTL	—	Selects which SDRAM bank of eight is activated.
A0–A13	SSTL	—	During a Bank Activate command cycle, Address input defines the row address (RA0–RA15). During a Read or Write command cycle, Address input defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12($\overline{BC}$) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped).
DQ0–DQ63, CB0–CB7	SSTL	—	Data and Check Bit Input/Output pins.
DM0–DM8	SSTL	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR3 SDRAM input buffers, and core logic. V_{DD} and V_{DD}Q pins are tied to V_{DD}/V_{DD}Q planes on these modules.

Symbol	Type	Polarity	Function
$\overline{DQS0}$–$\overline{DQS8}$ DQS0–DQS8	SSTL	Differential crossing	Data strobe for input and output data.
SA0–SA2		—	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA		—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to V_{DDSPD} to act as a pullup on the system board.
SCL		—	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to V_{DDSPD} to act as a pullup on the system board.
V_{DDSPD}	Supply		Power supply for SPD EEPROM. This supply is separate from the V_{DD}/$V_{DD}Q$ power plane. EEPROM supply is operable from 3.0V to 3.6V.

2.3 Pin Assignment

Front Side(left 1–60)			Back Side(right 121–180)			Front Side(left 61–120)			Back Side(right 181–240)		
Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC
1	$V_{REF}DQ$	$V_{REF}DQ$	121	V_{SS}	V_{SS}	61	A2	A2	181	A1	A1
2	V_{SS}	V_{SS}	122	DQ4	DQ4	62	V_{DD}	V_{DD}	182	V_{DD}	V_{DD}
3	DQ0	DQ0	123	DQ5	DQ5	63	CK1	CK1	183	V_{DD}	V_{DD}
4	DQ1	DQ1	124	V_{SS}	V_{SS}	64	$\overline{CK1}$	$\overline{CK1}$	184	CK0	CK0
5	V_{SS}	V_{SS}	125	DM0	DM0	65	V_{DD}	V_{DD}	185	$\overline{CK0}$	$\overline{CK0}$
6	$\overline{DQS0}$	$\overline{DQS0}$	126	NC	NC	66	V_{DD}	V_{DD}	186	V_{DD}	V_{DD}
7	DQS0	DQS0	127	V_{SS}	V_{SS}	67	$V_{REF}CA$	$V_{REF}CA$	187	NC	NC
8	V_{SS}	V_{SS}	128	DQ6	DQ6	68	NC	NC	188	A0	A0
9	DQ2	DQ2	129	DQ7	DQ7	69	V_{DD}	V_{DD}	189	V_{DD}	V_{DD}
10	DQ3	DQ3	130	V_{SS}	V_{SS}	70	A10	A10	190	$BA1^2$	$BA1^2$
11	V_{SS}	V_{SS}	131	DQ12	DQ12	71	$BA0^2$	$BA0^2$	191	V_{DD}	V_{DD}
12	DQ8	DQ8	132	DQ13	DQ13	72	V_{DD}	V_{DD}	192	$\overline{RAS}$	$\overline{RAS}$
13	DQ9	DQ9	133	V_{SS}	V_{SS}	73	$\overline{WE}$	$\overline{WE}$	193	$\overline{S0}$	$\overline{S0}$
14	V_{SS}	V_{SS}	134	DM1	DM1	74	$\overline{CAS}$	$\overline{CAS}$	194	V_{DD}	V_{DD}
15	$\overline{DQS1}$	$\overline{DQS1}$	135	NC	NC	75	V_{DD}	V_{DD}	195	ODT0	ODT0
16	DQS1	DQS1	136	V_{SS}	V_{SS}	76	S1	S1	196	A13	A13

NC = No Connect; RFU = Reserved Future Use

1. NC pins should not be connected to anything on the DIMM, including bussing within the NC group.
2. Address pins A3–A8 and BA0 and BA1 can be mirrored or not mirrored. Please refer to Section 4.1 for more information on mirrored addresses.

Front Side(left 1–60)			Back Side(right 121–180)			Front Side(left 61–120)			Back Side(right 181–240)		
Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC
17	VSS	VSS	137	DQ14	DQ14	77	ODT1	ODT1	197	VDD	VDD
18	DQ10	DQ10	138	DQ15	DQ15	78	VDD	VDD	198	NC	NC
19	DQ11	DQ11	139	VSS	VSS	79	NC	NC	199	VSS	VSS
20	VSS	VSS	140	DQ20	DQ20	80	VSS	VSS	200	DQ36	DQ36
21	DQ16	DQ16	141	DQ21	DQ21	81	DQ32	DQ32	201	DQ37	DQ37
22	DQ17	DQ17	142	VSS	VSS	82	DQ33	DQ33	202	VSS	VSS
23	VSS	VSS	143	DM2	DM2	83	VSS	VSS	203	DM4	DM4
24	$\overline{DQS2}$	$\overline{DQS2}$	144	$\overline{NC}$	$\overline{NC}$	84	$\overline{DQS4}$	$\overline{DQS4}$	204	NC	NC
25	DQS2	DQS2	145	VSS	VSS	85	DQS4	DQS4	205	VSS	VSS
26	VSS	VSS	146	DQ22	DQ22	86	VSS	VSS	206	DQ38	DQ38
27	DQ18	DQ18	147	DQ23	DQ23	87	DQ34	DQ34	207	DQ39	DQ39
28	DQ19	DQ19	148	VSS	VSS	88	DQ35	DQ35	208	VSS	VSS
29	VSS	VSS	149	DQ28	DQ28	89	VSS	VSS	209	DQ44	DQ44
30	DQ24	DQ24	150	DQ29	DQ29	90	DQ40	DQ40	210	DQ45	DQ45
31	DQ25	DQ25	151	VSS	VSS	91	DQ41	DQ41	211	VSS	VSS
32	VSS	VSS	152	DM3	DM3	92	VSS	VSS	212	DM5	DM5
33	$\overline{DQS3}$	$\overline{DQS3}$	153	NC	NC	93	$\overline{DQS5}$	$\overline{DQS5}$	213	NC	NC
34	DQS3	DQS3	154	VSS	VSS	94	DQS5	DQS5	214	VSS	VSS
35	VSS	VSS	155	DQ30	DQ30	95	VSS	VSS	215	DQ46	DQ46
36	DQ26	DQ26	156	DQ31	DQ31	96	DQ42	DQ42	216	DQ47	DQ47
37	DQ27	DQ27	157	VSS	VSS	97	DQ43	DQ43	217	VSS	VSS
38	VSS	VSS	158	NC	CB4	98	VSS	VSS	218	DQ52	DQ52
39	NC	CB0	159	NC	CB5	99	DQ48	DQ48	219	DQ53	DQ53
40	NC	CB1	160	VSS	VSS	100	DQ49	DQ49	220	VSS	VSS
41	VSS	VSS	161	DM8	DM8	101	VSS	VSS	221	DM6	DM6
42	NC	$\overline{DQS8}$	162	NC	NC	102	$\overline{DQS6}$	$\overline{DQS6}$	222	NC	NC
43	NC	DQS8	163	VSS	VSS	103	DQS6	DQS6	223	VSS	VSS
44	VSS	VSS	164	NC	CB6	104	VSS	VSS	224	DQ54	DQ54
45	NC	CB2	165	NC	CB7	105	DQ50	DQ50	225	DQ55	DQ55
46	NC	CB3	166	VSS	VSS	106	DQ51	DQ51	226	VSS	VSS
47	VSS	VSS	167	NC	NC	107	VSS	VSS	227	DQ60	DQ60

NC = No Connect; RFU = Reserved Future Use

1. NC pins should not be connected to anything on the DIMM, including bussing within the NC group.
2. Address pins A3–A8 and BA0 and BA1 can be mirrored or not mirrored. Please refer to Section 4.1 for more information on mirrored addresses.

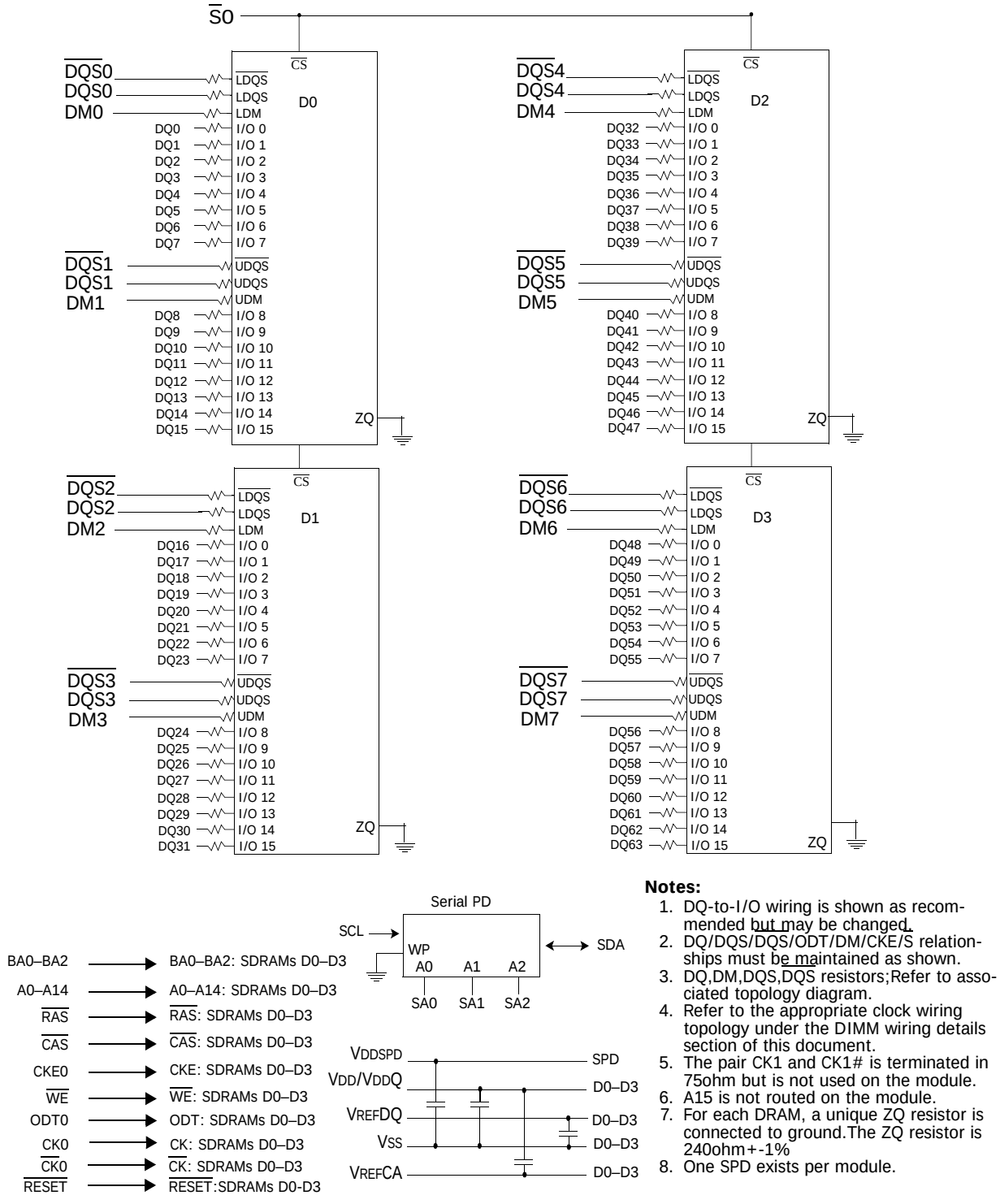
Front Side(left 1–60)			Back Side(right 121–180)			Front Side(left 61–120)			Back Side(right 181–240)		
Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC
48	NC	NC	168	Reset	Reset	108	DQ56	DQ56	228	DQ61	DQ61
KEY			KEY			109	DQ57	DQ57	229	VSS	VSS
49	NC	NC	169	CKE1/NC	CKE1/NC	110	VSS	VSS	230	DM7	DM7
50	CKE0	CKE0	170	VDD	VDD	111	$\overline{DQS7}$	$\overline{DQS7}$	231	NC	NC
51	VDD	VDD	171	NC	NC	112	DQS7	DQS7	232	VSS	VSS
52	BA2	BA2	172	NC	NC	113	VSS	VSS	233	DQ62	DQ62
53	NC	NC	173	VDD	VDD	114	DQ58	DQ58	234	DQ63	DQ63
54	VDD	VDD	174	A12	A12	115	DQ59	DQ59	235	VSS	VSS
55	All	All	175	A9	A9	116	VSS	VSS	236	VDDSPD	VDDSPD
56	A7[2]	A7[2]	176	VDD	VDD	117	SA0	SA0	237	SA1	SA1
57	VDD	VDD	177	A8[2]	A8[2]	118	SCL	SCL	238	SDA	SDA
58	A5[2]	A5[2]	178	A6[2]	A6[2]	119	SA2	SA2	239	VSS	VSS
59	A4[2]	A4[2]	179	VDD	VDD	120	VTT	VTT	240	VTT	VTT
60	VDD	VDD	180	A3[2]	A3[2]						

NC = No Connect; RFU = Reserved Future Use

1. NC pins should not be connected to anything on the DIMM, including bussing within the NC group.
2. Address pins A3–A8 and BA0 and BA1 can be mirrored or not mirrored. Please refer to Section 4.1 for more information on mirrored addresses.

3. Functional Block Diagram

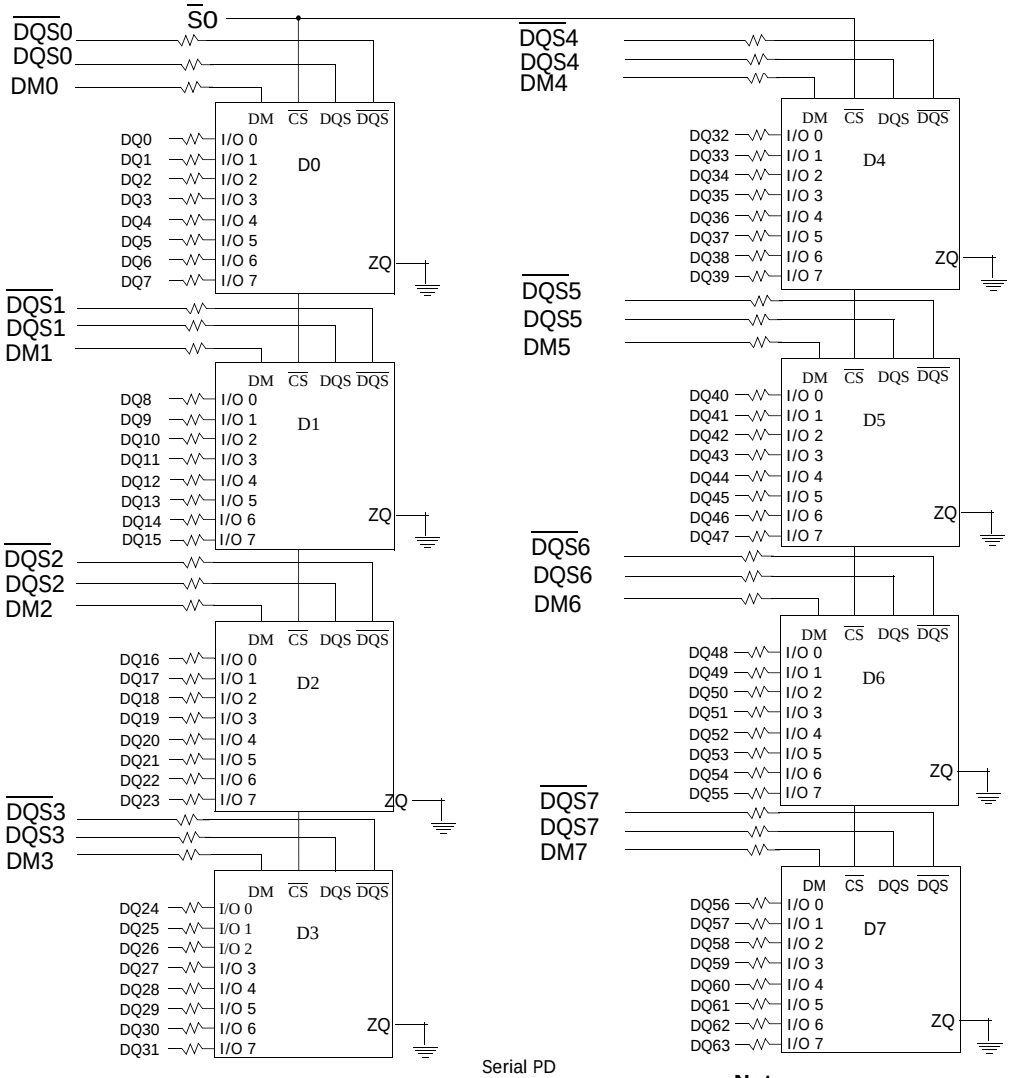
3.1 512MB, 64Mx64 Module(1Rank of x16)

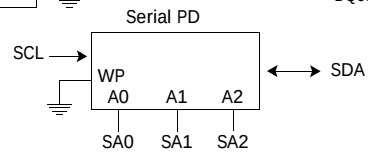


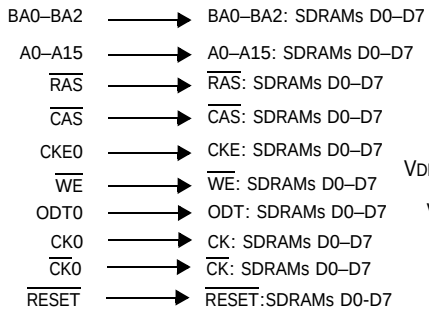
Notes:

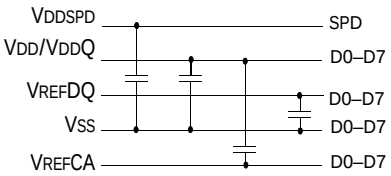
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. DQ,DM,DQS,DQS resistors;Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of this document.
5. The pair CK1 and CK1# is terminated in 75ohm but is not used on the module.
6. A15 is not routed on the module.
7. For each DRAM, a unique ZQ resistor is connected to ground.The ZQ resistor is 240ohm+-1%
8. One SPD exists per module.

3.2 1GB, 128Mx64 Module(1Rank of x8)





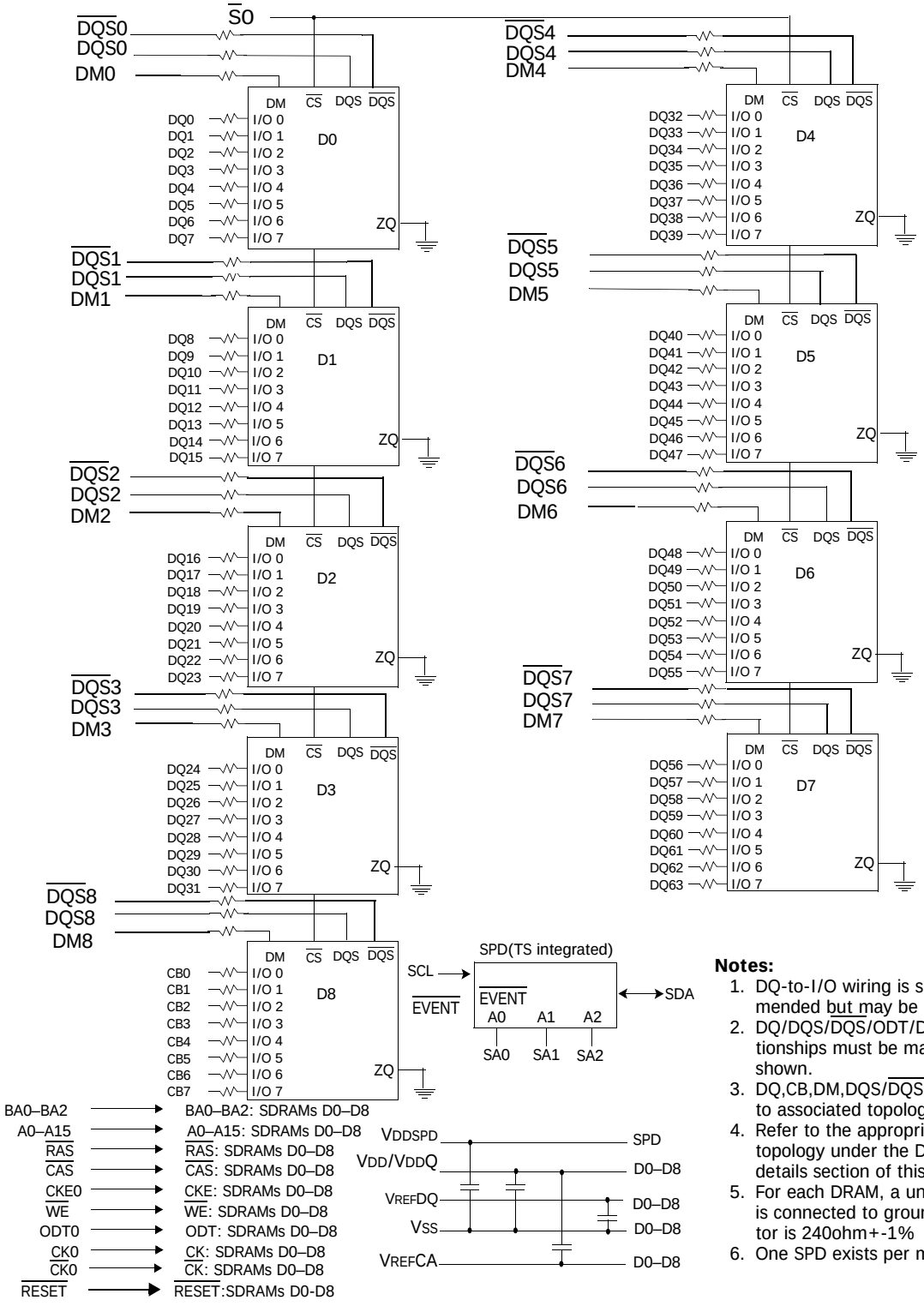




Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. DQ,DM,DQS/DQS resistors;Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of this document.
5. Refer to Section 3.1 of this document for details on address mirroring.
6. For each DRAM, a unique ZQ resistor is connected to ground.The ZQ resistor is 240ohm+-1%
7. One SPD exists per module.

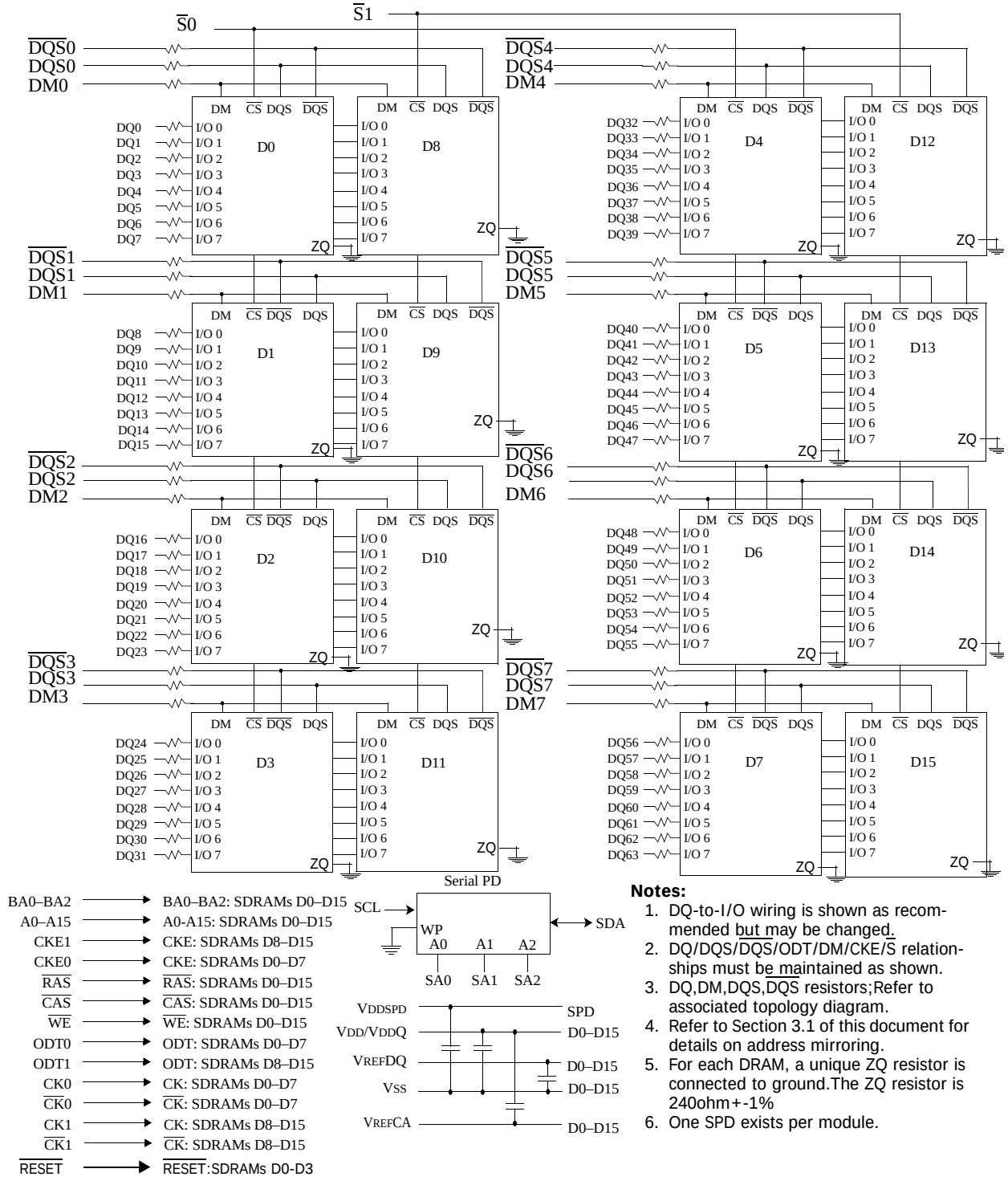
3.3 1GB, 128Mx72 Module(1Rank of x8)



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. DQ,CB,DM,DQS/DQS resistors;Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of this document.
5. For each DRAM, a unique ZQ resistor is connected to ground.The ZQ resistor is 240ohm+-1%
6. One SPD exists per module.

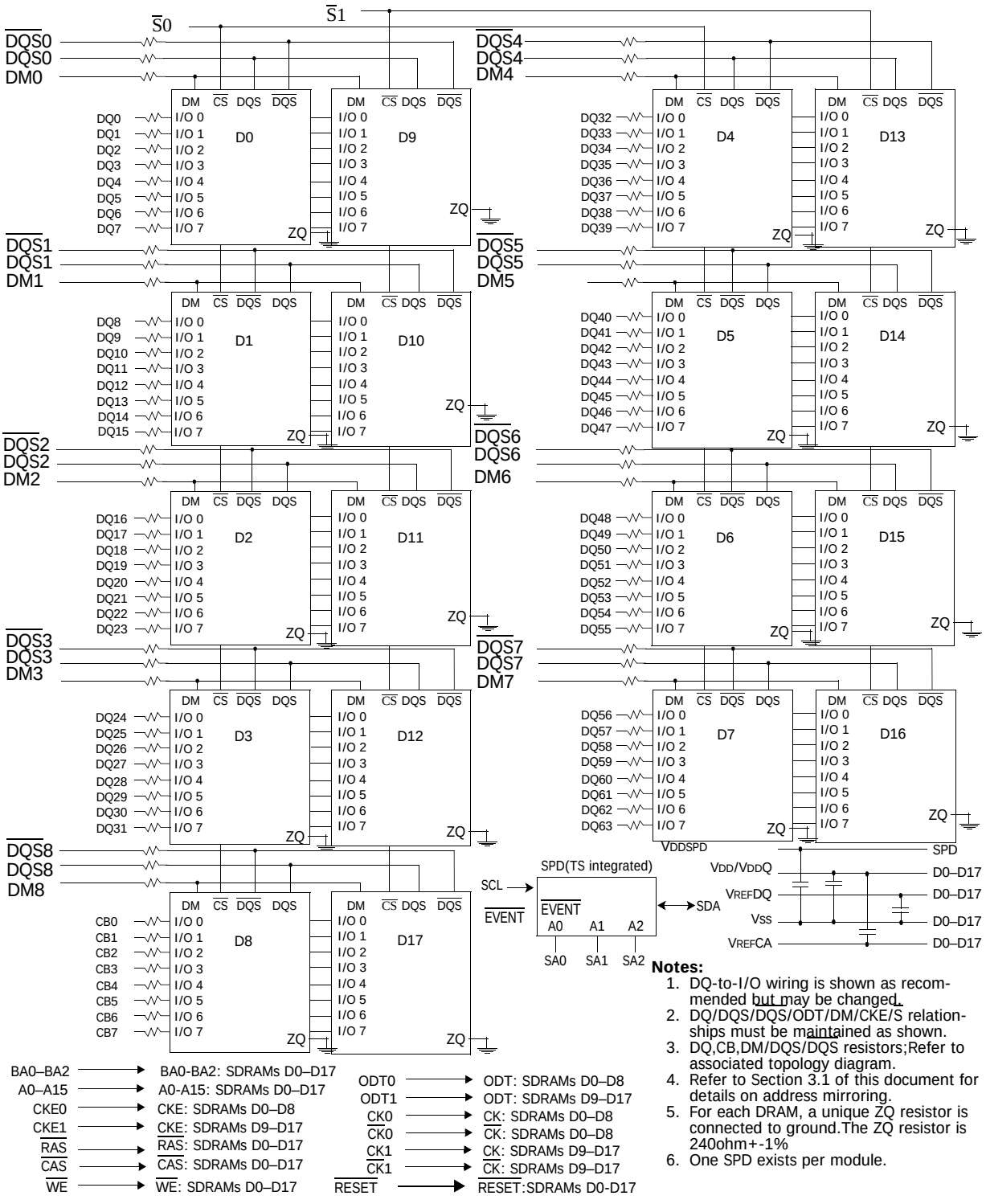
3.4 2GB, 256Mx64 Module(2Rank of x8)



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. DQ,DM,DQS,DQS resistors;Refer to associated topology diagram.
4. Refer to Section 3.1 of this document for details on address mirroring.
5. For each DRAM, a unique ZQ resistor is connected to ground.The ZQ resistor is 240ohm+-1%
6. One SPD exists per module.

3.5 2GB, 256Mx72 Module(2Rank of x8)



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. DQ,CB,DM/DQS/DQS resistors;Refer to associated topology diagram.
4. Refer to Section 3.1 of this document for details on address mirroring.
5. For each DRAM, a unique ZQ resistor is connected to ground.The ZQ resistor is 240ohm+-1%
6. One SPD exists per module.

4. Address Mirroring Feature

There is a via grid located under the SDRAMs for wiring the CA signals (address, bank address, command, and control lines) to the SDRAM pins. The length of the traces from the via to the SDRAMs places limitations on the bandwidth of the module. The shorter these traces, the higher the bandwidth. To extend the bandwidth of the CA bus for DDR3 modules, a scheme was defined to reduce the length of these traces.The pins on the SDRAM are defined in a manner that allows for these short trace lengths. The CA bus pins in Columns 2 and 8, ignoring the mechanical support pins, do not have any special functions (secondary functions). This allows the most flexibility with these pins. These are address pins A3, A4, A5, A6, A7, A8 and bank address pins BA0 and BA1. Refer to Table . Rank 0 SDRAM pins are wired straight, with no mismatch between the connector pin assignment and the SDRAM pin assignment. Some of the Rank 1 SDRAM pins are cross wired as defined in the table. Pins not listed in the table are wired straight.

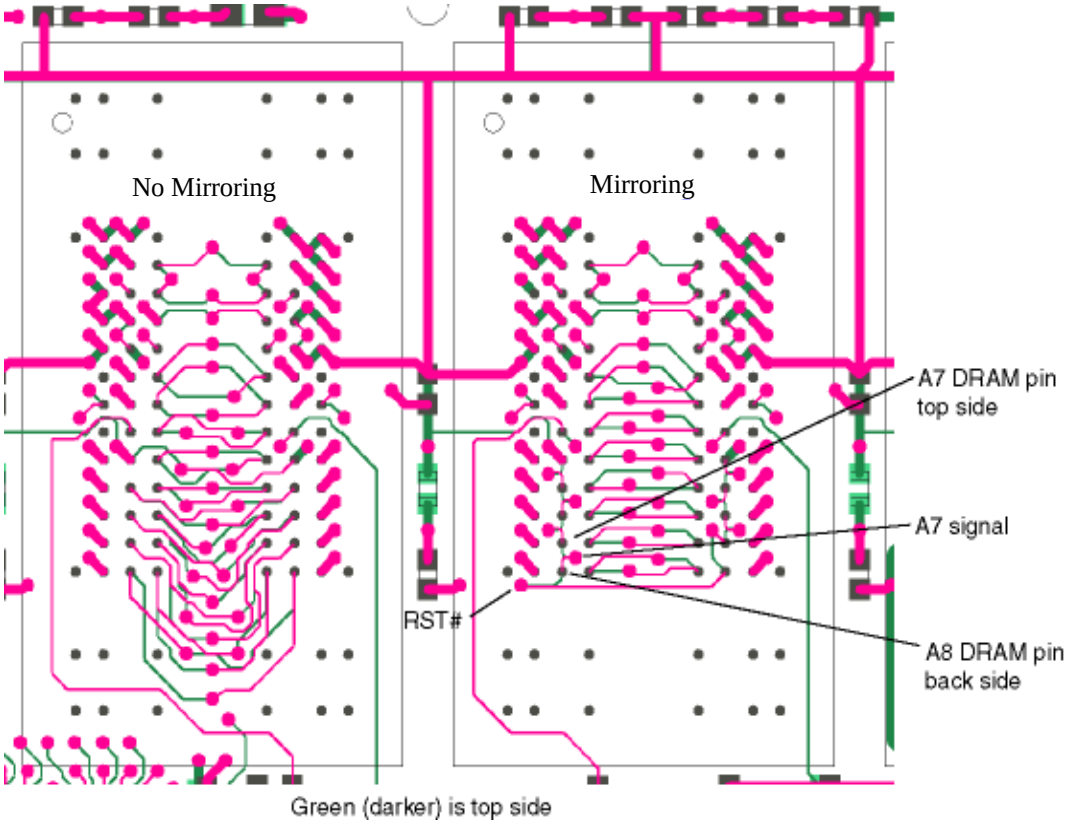
4.1 DRAM Pin Wiring for Mirroring

Connector Pin	SDRAM Pin	
	Rank 0	Rank 1
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
BA0	BA0	BA1
BA1	BA1	BA0

<Table 4.1: SDRAM Pin Wiring for Mirroring >

The table 4.1 illustrates the wiring in both the mirrored and non-mirrored case.

The lengths of the traces to the SDRAM pins, is obviously shorter. The via grid is smaller as well.



< Figure 4.1: Wiring Differences for Mirrored and Non-Mirrored Addresses >

Since the cross-wired pins have no secondary functions, there is no problem in normal operation. Any data written is read the same way. There are limitations however. When writing to the internal registers with a "load mode" operation, the specific address is required. This requires the controller to know if the rank is mirrored or not. This requires a few rules. Mirroring is done on 2 rank modules and can only be done on the second rank. There is not a requirement that the second rank be mirrored. There is a bit assignment in the SPD that indicates whether the module has been designed with the mirrored feature or not. See the DDR3 UDIMM SPD specification for these details. The controller must read the SPD and have the capability of de-mirroring the address when accessing the second rank.

5. ABSOLUTE MAXIMUM RATINGS

5.1 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.975 V	V	,3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.975 V	V	,3
VIN, VOUT	Voltage on any pin relative to Vss	- 0.4 V ~ 1.975 V	V	
TSTG	Storage Temperature	-55 to +100 ℃	℃	, 2

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times;and VREF must be not greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

5.2 DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
TOPER	Normal Temperature Range	0 to 85	℃	,2
	Extended Temperature Range	85 to 95	℃	1,3

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85oC under all operating conditions
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°... and 95°... case temperature.
   Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. (This double refresh requirement may not apply for some devices.) It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/ or the DIMM SPD for option avail ability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, than it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0band MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

6. AC & DC Operating Conditions

6.1 Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD abd VDDQ tied together.

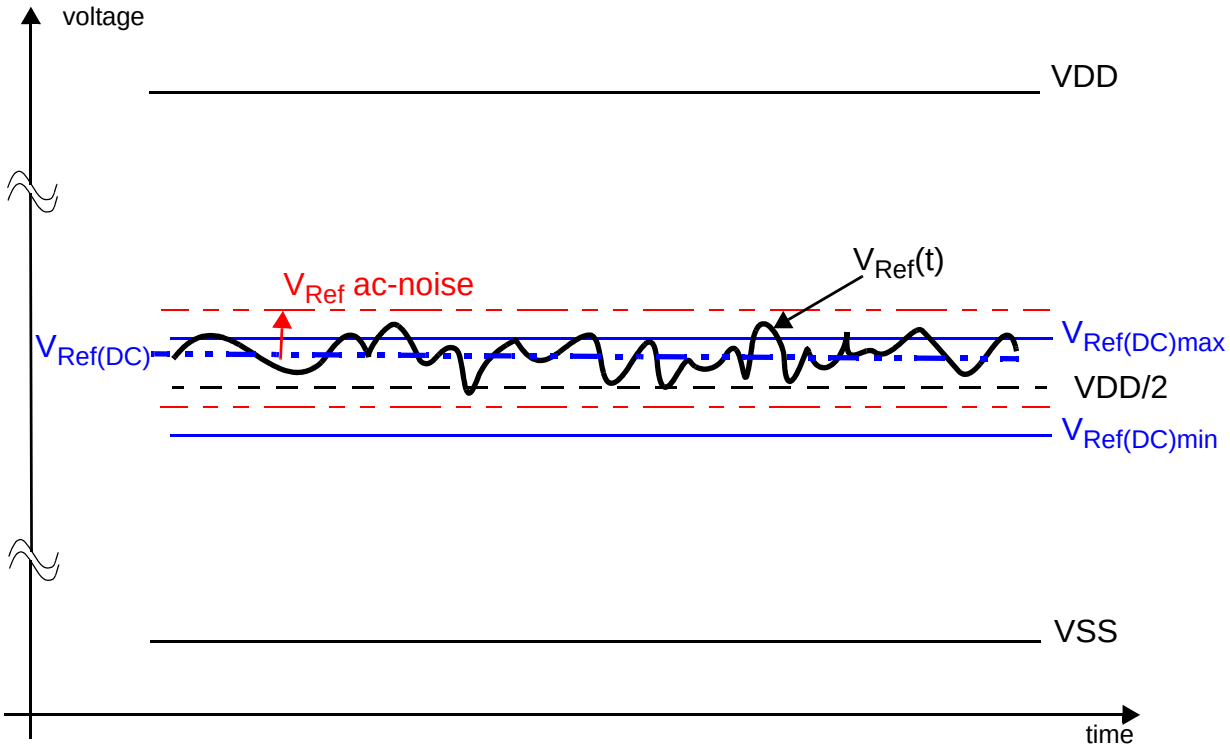
6.2 DC & AC Logic Input Levels

6.2.1 DC & AC Logic Input Levels for Single-Ended Signals

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Unit	Notes
		Min	Max		
VIH(DC)	DC input logic high	Vref + 0.100	-	V	1, 2
VIL(DC)	DC input logic low		Vref - 0.100	V	1, 2
VIH(AC)	AC input logic high	Vref + 0.175	-	V	1, 2
VIL(AC)	AC input logic low		Vref - 0.175	V	1, 2
VRefDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	3, 4
VRefCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4
VTT	Termination voltage for DQ, DQS outputs	VDDQ/2 - TBD	VDDQ/2 + TBD	V	

1. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.
2. The “t.b.d.” entries might change based on overshoot and undershoot specification.
3. The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
   For reference: approx. VDD/2 +/- 15 mV.

The dc-tolerance limits and ac-noise limits for the reference voltages VRefCA and VRefDQ are illustrated in figure 6.2.1. It shows a valid reference voltage VRef(t) as a function of time. (VRef stands for VRefCA and VRefDQ like-wise).VRef(DC) is the linear average of VRef(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table 1. Furthermore VRef(t) may temporarily deviate from VRef(DC) by no more than +/- 1% VDD.



< Figure 6.2.1: Illustration of Vref(DC) tolerance and Vref AC-noise limits >

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VRef. "VRef " shall be understood as VRef(DC), as defined in Figure 6.2.1
This clarifies, that dc-variations of VRef affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VRef(DC) deviations from the optimum position within the data-eye of the input signals.
This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VRef ac-noise. Timing and voltage effects due to ac-noise on VRef up to the specified limit (+/-1% of VDD) are included in DRAM timings and their associated deratings.

6.2.2 DC & AC Logic Input Levels for Differential Signals

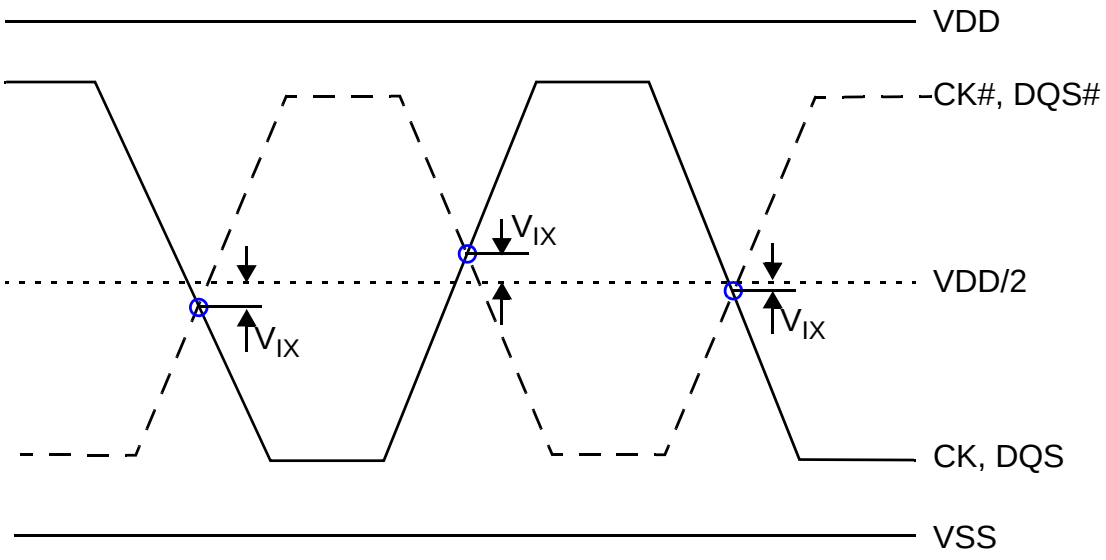
Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Unit	Notes
		Min	Max		
VIHdiff	Differential input logic high	+ 0.200	-	V	1
VILdiff	Differential input logic low		- 0.200	V	1

Note1:

Refer to “Overshoot and Undershoot Specification section 6.5 on 26 page

6.2.3 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) must meet the requirements in Table 6.2.3 The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the midlevel between of VDD and VSS.



< Figure 6.2.3 Vix Definition >

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Unit	Notes
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2	- 150	+ 150	mV	

< Table 6.2.3: Cross point voltage for differential input signals (CK, DQS) >

6.3 Slew Rate Definitions

6.3.1 For Single Ended Input Signals

- Input Slew Rate for Input Setup Time (tIS) and Data Setup Time (tDS)

Setup (tIS and tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIH(AC)min. Setup (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIL(AC)max.

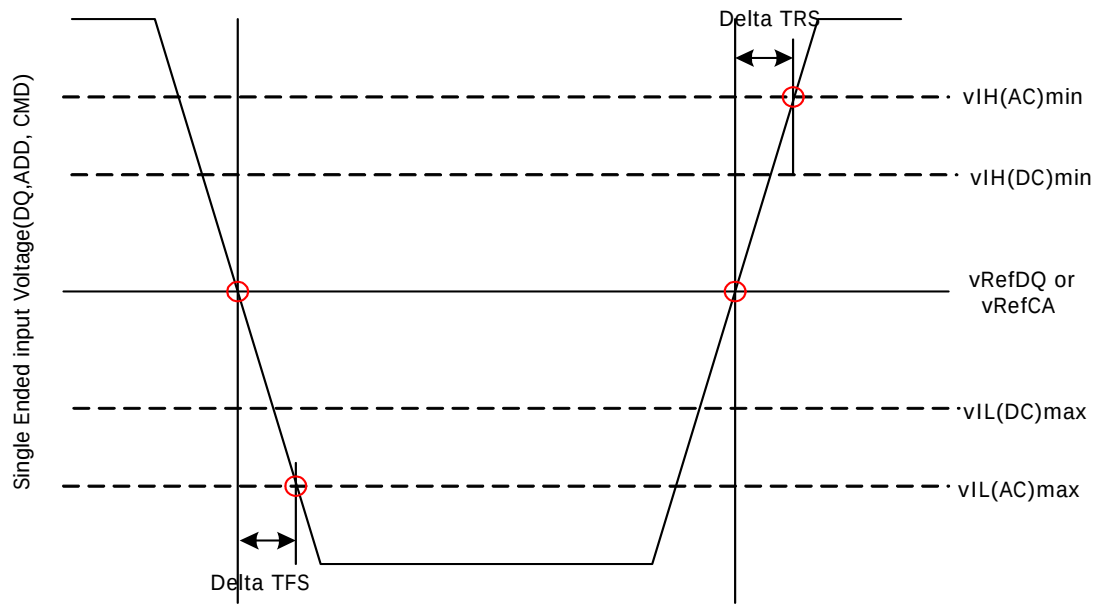
- Input Slew Rate for Input Hold Time (tIH) and Data Hold Time (tDH)

Hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VRef. Hold (tIH and tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VRef.

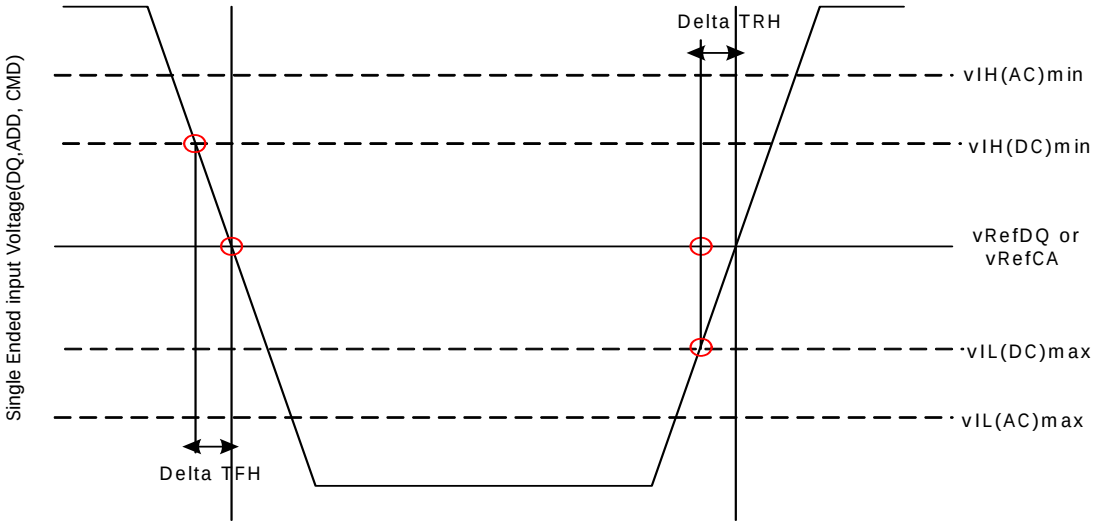
Description	Measured		Defined by	Applicable for
	Min	Max		
Input slew rate for rising edge	Vref	VIH(AC)min	$\frac{\text{VIH(AC)min-Vref}}{\text{Delta TRS}}$	Setup (tIS, tDS)
Input slew rate for falling edge	Vref	VIL(AC)max	$\frac{\text{Vref-VIL(AC)max}}{\text{Delta TFS}}$	
Input slew rate for rising edge	VIL(DC)max	Vref	$\frac{\text{Vref-VIL(DC)max}}{\text{Delta TFH}}$	Hold (tIH, tDH)
Input slew rate for falling edge	VIH(DC)min	Vref	$\frac{\text{VIH(DC)min-Vref}}{\text{Delta TRH}}$	

< Table 6.3.1: Single-Ended Input Slew Rate Definition >

Part A: Set up



Part B: Hold



< Figure 6.3.1: Input Nominal Slew Rate Definition for Single-Ended Signals >

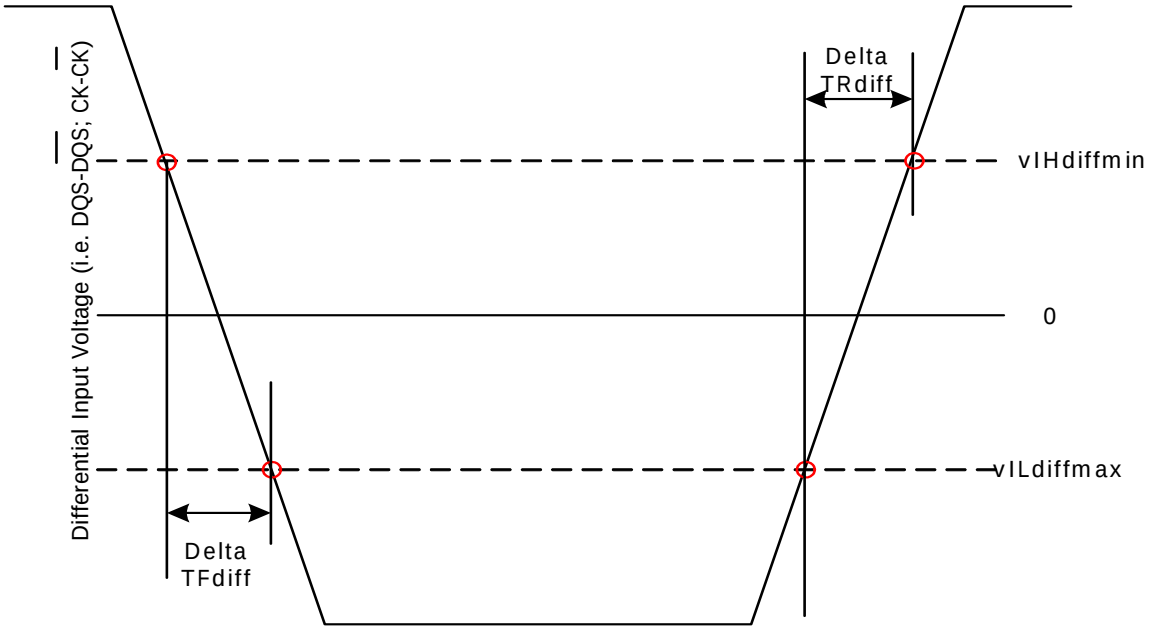
6.3.2 Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured as shown in below Table and Figure .

Description	Measured		Defined by
	Min	Max	
Differential input slew rate for rising edge (CK-CK and DQS-DQS)	VILdiffmax	VIHdiffmin	VIHdiffmin-VILdiffmax / $\overline{\text{DeltaTRdiff}}$
Differential input slew rate for falling edge (CK-CK and DQS-DQS)	VIHdiffmin	VILdiffmax	VIHdiffmin-VILdiffmax / $\overline{\text{DeltaTFdiff}}$

Note:

The differential signal (i.e. CK-CK and DQS-DQS) must be linear between these thresholds.



< Figure 6.3.2: Differential Input Slew Rate Definition for DQS,DQS# and CK,CK# >

6.4 DC & AC Output Buffer Levels

6.4.1 Single Ended DC & AC Output Levels

Below table shows the output levels used for measurements of single ended signals.

Symbol	Parameter	DDR3-800, 1066, 1333 and 1600	Unit	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.2 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT + 0.1 x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT - 0.1 x VDDQ	V	1

1. The swing of ± 0.1 x VDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ / 2.

6.4.2 Differential DC & AC Output Levels

Below table shows the output levels used for measurements of differential signals.

Symbol	Parameter	DDR3-800, 1066, 1333 and 1600	Unit	Notes
VOHdiff (AC)	AC differential output high measurement level (for output SR)	+ 0.2 x VDDQ	V	1
VOLdiff (AC)	AC differential output low measurement level (for output SR)	- 0.2 x VDDQ	V	1

1. The swing of °æ 0.2 x VDDQ is based on approximately 50% of the static differential output high or low swingwith a driver impedance of 40ßŸ and an effective test load of 25ßŸ to VTT = VDDQ/2 at each of the differential output

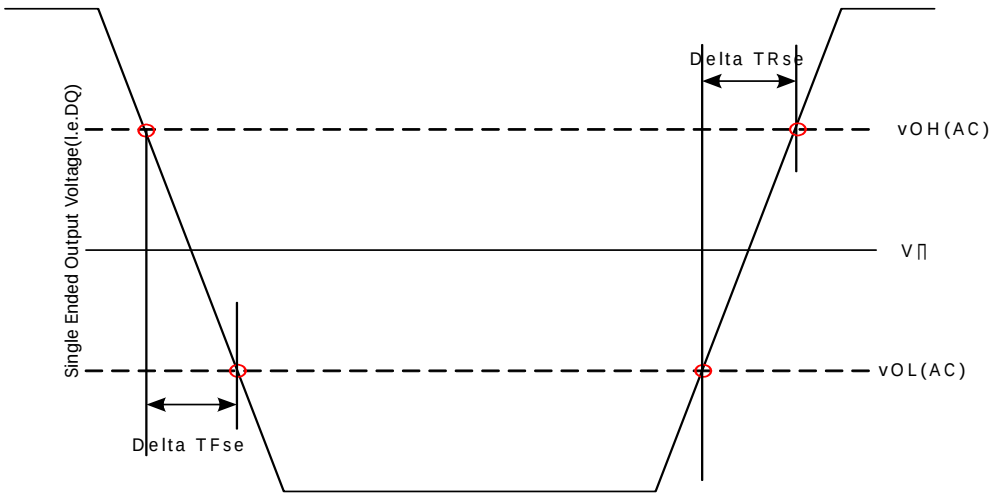
6.4.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in below Table and Figure 6.4.3.

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	$\frac{VOH(AC)-VOL(AC)}{\overline{DeltaTRse}}$
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	$\frac{VOH(AC)-VOL(AC)}{\overline{DeltaTFse}}$

Note:

Output slew rate is verified by design and characterization, and may not be subject to production test.



< Figure 6.4.3: Single Ended Output Slew Rate Definition >

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	2.5	5	TBD	5	V/ns

***** Description:**
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
For Ron = RZQ/7 setting

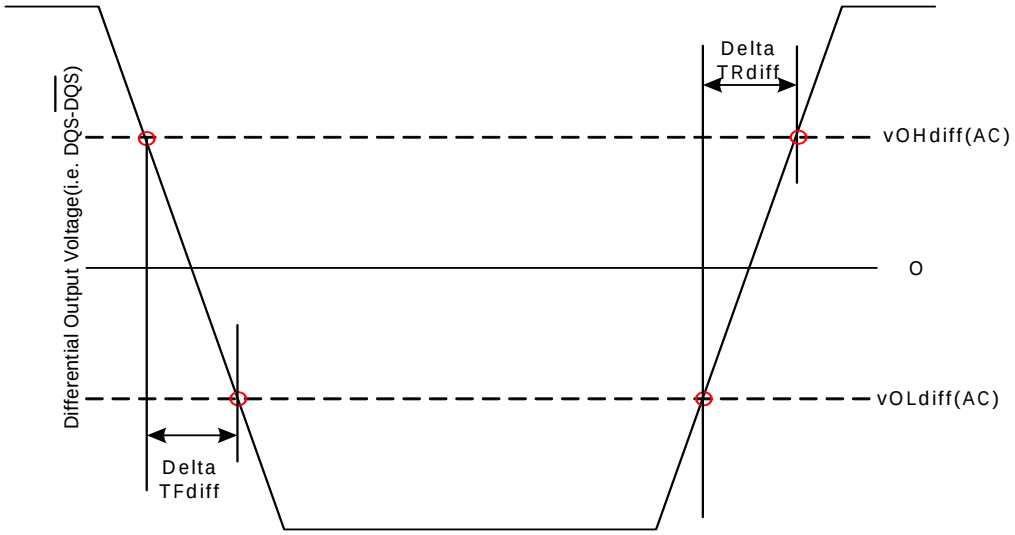
< Table 6.4.3: Output Slew Rate (single-ended) >

6.4.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in below Table and Figure 6.4.4

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	$\frac{\text{VOHdiff(AC)-VOLdiff(AC)}}{\overline{\text{DeltaTRdiff}}}$
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	$\frac{\text{VOHdiff(AC)-VOLdiff(AC)}}{\overline{\text{DeltaTFdiff}}}$

Note: Output slew rate is verified by design and characterization, and may not be subject to production test.



< Figure 6.4.4: Differential Output Slew Rate Definition >

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	5	10	5	10	5	10	TBD	10	V/ns

*****Description:**
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

< Table 6.6.4: Differential Output Slew Rate >

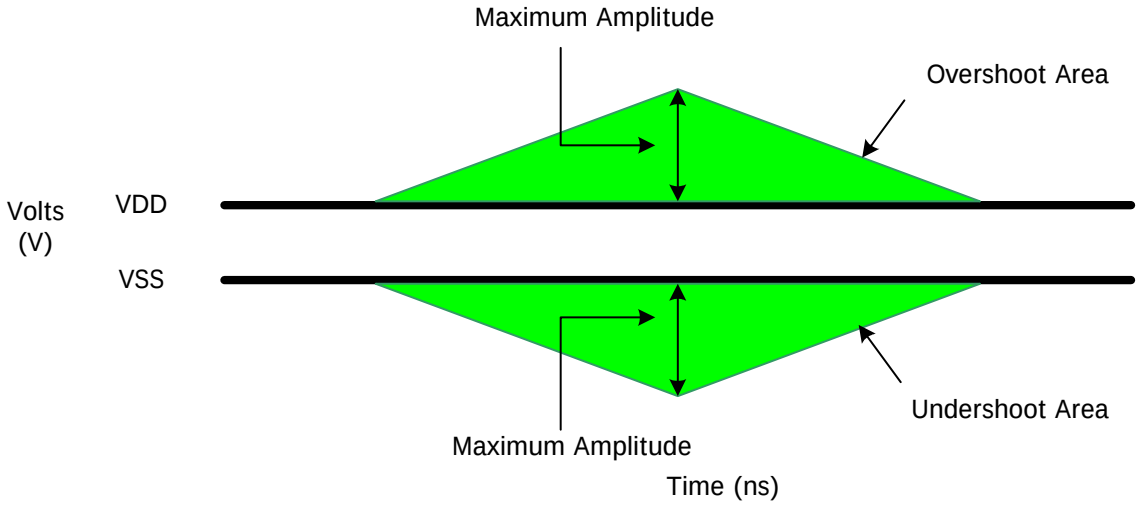
6.5 Overshoot and Undershoot Specifications

6.5.1 Address and Control Overshoot and Undershoot Specifications

Description	Specification			
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for overshoot area (see Figure)	0.4V	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure)	0.4V	0.4V	0.4V	0.4V
Maximum overshoot area above VDD (See Figure)	0.67 V-ns	0.5 V-ns	0.4 V-ns	0.33 V-ns
Maximum undershoot area below VSS (See Figure)	0.67 V-ns	0.5 V-ns	0.4 V-ns	0.33 V-ns

< Table 6.5.1: AC Overshoot/Undershoot Specification for Address and Control Pins >

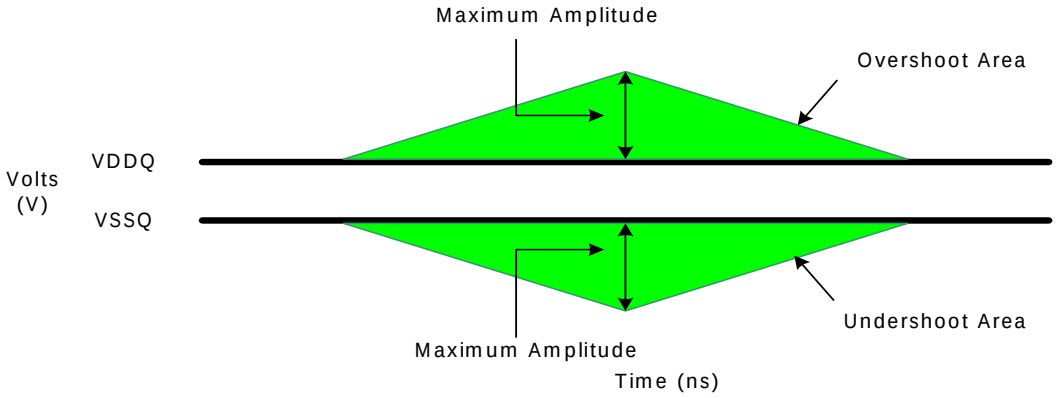
< Figure 6.5.1: Address and Control Overshoot and Undershoot Definition >



6.5.2 Clock,Data,Strobe and Mask Overshoot and Undershoot Specifications

Description	Specification			
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600
Maximum peak amplitude allowed for overshoot area (see Figure)	0.4V	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure)	0.4V	0.4V	0.4V	0.4V
Maximum overshoot area above VDDQ (See Figure)	0.25 V-ns	0.19 V-ns	0.15 V-ns	0.13 V-ns
Maximum undershoot area below VSSQ (See Figure)	0.25 V-ns	0.19 V-ns	0.15 V-ns	0.13 V-ns

< Table 6.5.2: AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask >



Clock, Data Strobe and Mask Overshoot and Undershoot Definition

< Figure 6.5.2: Clock, Data, Strobe and Mask Overshoot and Undershoot Definition >

6.6 Pin Capacitance

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, DQS#, TDQS, TDQS#)	C_{IO}	1.5	3.0	1.5	3.0	1.5	2.5	TBD	TBD	pF	1,2,3
Input capacitance, CK and CK#	C_{CK}	TBD	1.6	TBD	1.6	TBD	TBD	TBD	TBD	pF	2,3,5
Input capacitance delta CK and CK#	C_{DCK}	0	0.15	0	0.15	TBD	TBD	TBD	TBD	pF	2,3,4
Input capacitance (All other input-only pins)	C_{I}	TBD	1.5	TBD	1.5	TBD	TBD	TBD	TBD	pF	2,3,6
Input capacitance delta, DQS and DQS#	C_{DDQS}	0	0.20	0	0.20	TBD	TBD	TBD	TBD	pF	2,3,12
Input capacitance delta (All CTRL input-only pins)	C_{DI_CTRL}	-0.5	0.3	-0.5	0.3	TBD	TBD	TBD	TBD	pF	2,3,7,8
Input capacitance delta (All ADD/CMD input-only pins)	$C_{DI\_ADD\_CMD}$	-0.5	0.5	-0.5	0.5	TBD	TBD	TBD	TBD	pF	2,3,9, 10
Input/output capacitance delta (DQ, DM, DQS, DQS#)	C_{DIO}	-0.5	0.3	-0.5	0.3	TBD	TBD	TBD	TBD	pF	2,3,11

Notes:

1. TDQS/TDQS# are not necessarily input function but since TDQS is sharing DM pin and the parasitic characterization of TDQS/TDQS# should be close as much as possible, Cio&Cdio requirement is applied (recommend deleting note or changing to “Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS.”)
2. This parameter is not subject to production test. It is verified by design and characterization. Input capacitance is measured according to JEP147(“PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)”) with VDD, VDDQ, VSS,VSSQ applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of C_{CK}-C_{CK}#.
5. The minimum C_{CK} will be equal to the minimum C_{I}.
6. Input only pins include: ODT, CS, CKE, A0-A15, BA0-BA2, RAS#, CAS#, WE#.
7. CTRL pins defined as ODT, CS and CKE.
8. C_{DI_CTRL}=C_{I}(CNTL) - 0.5 * C_{I}(CLK) + C_{I}(CLK#))
9. ADD pins defined as A0-A15, BA0-BA2 and CMD pins are defined as RAS#, CAS# and WE#.
10. $C_{DI\_ADD\_CMD}$=C_{I}(ADD_CMD) - 0.5*(C_{I}(CLK)+C_{I}(CLK#))
11. C_{DIO}=C_{IO}(DQ) - 0.5*(C_{IO}(DQS)+C_{IO}(DQS#))
12. Absolute value of C_{IO}(DQS) - C_{IO}(DQS#)

6.7 IDD Specifications(T_{CASE}: 0 to 95°C)

512MB, 64M x 64 U-DIMM: HMT164U6AFP6C

Symbol	DDR3 800	DDR3 1066	DDR3 1333	Unit	note
IDD0	360	420	480	mA	
IDD1	480	540	580	mA	
IDD2P(F)	100	120	140	mA	
IDD2P(S)	40	40	40	mA	
IDD2Q	180	240	280	mA	
IDD2N	200	240	300	mA	
IDD3P	140	180	200	mA	
IDD3N	220	280	340	mA	
IDD4W	700	880	1060	mA	
IDD4R	700	860	1020	mA	
IDD5B	740	780	840	mA	
IDD6(D)	40	40	40	mA	1
IDD6(S)	24	24	24	mA	1
IDD7	1300	1420	1720	mA	

1GB, 128M x 64 U-DIMM: HMT112U6AFP8C

Symbol	DDR3 800	DDR3 1066	DDR3 1333	Unit	note
IDD0	640	760	840	mA	
IDD1	760	880	960	mA	
IDD2P(F)	200	240	280	mA	
IDD2P(S)	80	80	80	mA	
IDD2Q	360	480	560	mA	
IDD2N	400	480	600	mA	
IDD3P	280	360	400	mA	
IDD3N	440	560	680	mA	
IDD4W	1120	1440	1560	mA	
IDD4R	1040	1320	1680	mA	
IDD5B	1480	1560	1720	mA	
IDD6(D)	80	80	80	mA	1
IDD6(S)	48	48	48	mA	1
IDD7	1800	2000	2440	mA	

1GB, 128M x 72 U-DIMM: HMT112U7AFP8C

Symbol	DDR3 800	DDR3 1066	DDR3 1333	Unit	note
IDD0	720	855	945	mA	
IDD1	855	990	1080	mA	
IDD2P(F)	225	270	315	mA	
IDD2P(S)	90	90	90	mA	
IDD2Q	405	540	630	mA	
IDD2N	450	540	675	mA	
IDD3P	315	405	450	mA	
IDD3N	495	630	765	mA	
IDD4W	1260	1620	1755	mA	
IDD4R	1170	1485	1890	mA	
IDD5B	1665	1755	1935	mA	
IDD6(D)	90	90	90	mA	1
IDD6(S)	54	54	54	mA	1
IDD7	2025	2250	2745	mA	

2GB, 256M x 64 U-DIMM: HMT125U6AFP8C

Symbol	DDR3 800	DDR3 1066	DDR3 1333	Unit	note
IDD0	1040	1240	1440	mA	
IDD1	1160	1360	1560	mA	
IDD2P(F)	400	480	560	mA	
IDD2P(S)	160	160	160	mA	
IDD2Q	720	960	1120	mA	
IDD2N	800	960	1200	mA	
IDD3P	560	720	800	mA	
IDD3N	880	1120	1360	mA	
IDD4W	1520	1920	2160	mA	
IDD4R	1440	1800	2280	mA	
IDD5B	1880	2040	2320	mA	
IDD6(D)	160	160	160	mA	1
IDD6(S)	96	96	96	mA	1
IDD7	2200	2480	3040	mA	

2GB, 256M x 72 U-DIMM: HMT125U7AFP8C

Symbol	DDR3 800	DDR3 1066	DDR3 1333	Unit	note
IDD0	1170	1395	1620	mA	
IDD1	1305	1530	1755	mA	
IDD2P(F)	450	540	630	mA	
IDD2P(S)	180	180	180	mA	
IDD2Q	810	1080	1260	mA	
IDD2N	900	1080	1350	mA	
IDD3P	630	810	900	mA	
IDD3N	990	1260	1530	mA	
IDD4W	1710	2160	2430	mA	
IDD4R	1620	2025	2565	mA	
IDD5B	2115	2295	2610	mA	
IDD6(D)	180	180	180	mA	1
IDD6(S)	108	108	108	mA	1
IDD7	2475	2790	3420	mA	

6.7 IDD Measurement Conditions

Within the tables provided further down, an overview about the IDD measurement conditions is provided as follows:

Table 1 — Overview of Tables providing IDD Measurement Conditions and DRAM Behavior

Table number	Measurement Conditions
Table 5 on page 33	IDD0 and IDD1
Table 6 on page 36	IDD2N, IDD2Q, IDD2P(0), IDD2P(1)
Table 7 on page 38	IDD3N and IDD3P
Table 8 on page 39	IDD4R, IDD4W, IDD7
Table 9 on page 42	IDD7 for different Speed Grades and different tRRD, tFAW conditions
Table 10 on page 43	IDD5B
Table 11 on page 44	IDD6, IDD6ET

Within the tables about IDD measurement conditions, the following definitions are used:

- LOW is defined as VIN <= VILAC(max.); HIGH is defined as VIN >= VIHAC(min.).

- STABLE is defined as inputs are stable at a HIGH or LOW level.

- FLOATING is defined as inputs are VREF = VDDQ / 2.

- SWITCHING is defined as described in the following 2 tables.

Table 2 — Definition of SWITCHING for Address and Command Input Signals

SWITCHING for **Address (row, column) and Command Signals ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)** is defined as:	
Address (row, column):	If not otherwise mentioned the inputs are stable at HIGH or LOW during 4 clocks and change then to the opposite value (e.g. Ax Ax Ax Ax $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ Ax Ax Ax Ax..... please see each IDDx definition for details
Bank address:	If not otherwise mentioned the bank addresses should be switched like the row/column addresses - please see each IDDx definition for details
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$):	Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, LOW, LOW, LOW} Define $\overline{D}$ = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, HIGH,HIGH,HIGH} Define Command Background Pattern = D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$... If other commands are necessary (e.g. ACT for IDD0 or Read for IDD4R), the Background Pattern Command is substituted by the respective $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ levels of the necessary command. See each IDDx definition for details and figures 1,2,3 as examples.

Table 3 — Definition of SWITCHING for Data (DQ)

SWITCHING for **Data (DQ)** is defined as	
Data (DQ)	Data DQ is changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, which means that data DQ is stable during one clock; see each IDDx definition for exceptions from this rule and for further details. See figures 1,2,3 as examples.
Data Masking (DM)	NO Switching; DM must be driven LOW all the time

Timing parameters are listed in the following table:

Table 4 — For IDD testing the following parameters are utilized.

Parameter Bin		DDR3-800		DDR3-1066			DDR3-1333			DDR3-1600			Unit
		5-5-5	6-6-6	6-6-6	7-7-7	8-8-8	7-7-7	8-8-8	9-9-9	8-8-8	9-9-9	101010	
t_{CKmin}(IDD)		2.5		1.875			1.5			1.25			ns
CL(IDD)		5	6	6	7	8	7	8	9	8	9	10	clk
t_{RCDmin}(IDD)		12.5	15	11.25	13.13	15	10.5	12	13.5	10	11.25	12.5	ns
t_{RCmin}(IDD)		50	52.5	48.75	50.63	52.50	46.5	48	49.5	tbd	tbd	tbd	ns
t_{RASmin}(IDD)		37.5	37.5	37.5	37.5	37.5	36	36	36	tbd	tbd	tbd	ns
t_{RPmin}(IDD)		12.5	15	11.25	13.13	15	10.5	12	13.5	10	11.25	12.5	ns
t_{FAW}(IDD)	x4/ x8	40	40	37.5	37.5	37.5	30	30	30	30	30	30	ns
	x16	50	50	50	50	50	45	45	45	40	40	40	ns
t_{RRD}(IDD)	x4/ x8	10	10	7.5	7.5	7.5	6.0	6.0	6.0	6.0	6.0	6.0	ns
	x16	10	10	10	10	10	7.5	7.5	7.5	7.5	7.5	7.5	ns
t_{RFC}(IDD) - 512Mb		90	90	90	90	90	90	90	90	90	90	90	ns
t_{RFC}(IDD) - 1 Gb		110	110	110	110	110	110	110	110	110	110	110	ns
t_{RFC}(IDD) - 2 Gb		160	160	160	160	160	160	160	160	160	160	160	ns
t_{RFC}(IDD) - 4 Gb		tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	tbd	ns

The following conditions apply:

- IDD specifications are tested after the device is properly initialized.

- Input slew rate is specified by AC Parametric test conditions.

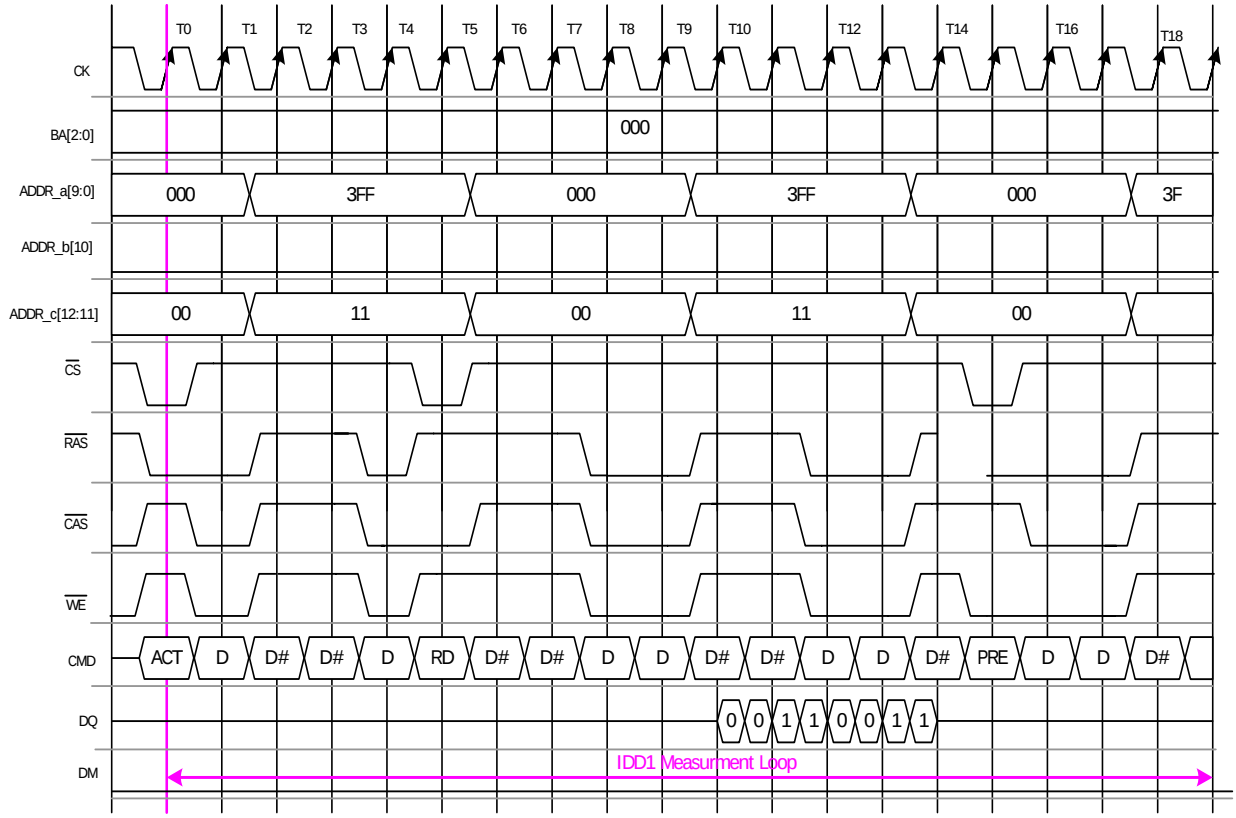
- IDD parameters are specified with ODT and output buffer disabled (MR1 Bit A12).

Table 5 — IDD Measurement Conditions for IDD0 and IDD1

Current	I_{DD0}	I_{DD1}
Name	**Operating Current 0** **-> One Bank Activate** **-> Precharge**	**Operating Current 1** **-> One Bank Activate** **-> Read** **-> Precharge**
Measurement Condition		
Timing Diagram Example		Figure 1
CKE	HIGH	HIGH
External Clock	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	t_{RCmin}(IDD)	t_{RCmin}(IDD)
t_{RAS}	t_{RASmin}(IDD)	t_{RASmin}(IDD)
t_{RCD}	n.a.	t_{RCDmin}(IDD)
t_{RRD}	n.a.	n.a.
CL	n.a.	CL(IDD)
AL	n.a.	0
$\overline{CS}$	HIGH between. Activate and Precharge Commands	HIGH between Activate, Read and Precharge
Command Inputs ($\overline{CS}$,$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	SWITCHING as described in Table 2 only exceptions are Activate and Precharge commands; example of IDD0 pattern: **A0**D$\overline{D}$D$\overline{D}$D$\overline{D}$D$\overline{D}$D$\overline{D}$D$\overline{D}$D$\overline{D}$D$\overline{D}$ **P0** (DDR3-800: t_{RAS} = 37.5ns between (A)ctivate and (P)recharge to bank 0; Definition of D and $\overline{D}$: see Table 2	SWITCHING as described in Table 2; only exceptions are Activate, Read and Precharge commands; example of IDD1 pattern: **A0**D$\overline{D}$D$\overline{D}$**R0**D$\overline{D}$D$\overline{D}$D$\overline{D}$D$\overline{D}$D$\overline{D}$ **P0** (DDR3-800 -555: t_{RCD} = 12.5ns between (A)ctivate and (R)ead to bank **0**; Definition of D and $\overline{D}$: see Table 2)

Table 5 — IDD Measurement Conditions for IDD0 and IDD1

Current	I_{DD0}	I_{DD1}
Name	**Operating Current 0** **-> One Bank Activate** **-> Precharge**	**Operating Current 1** **-> One Bank Activate** **-> Read** **-> Precharge**
Row, Column Addresses	Row addresses SWITCHING as described in Table 2; Address Input A10 must be LOW all the time!	Row addresses SWITCHING as described in Table 2; Address Input A10 must be LOW all the time!
Bank Addresses	bank address is fixed (bank 0)	bank address is fixed (bank 0)
Data I/O	SWITCHING as described in Table 3	Read Data: output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA, the output buffer should be switched off by MR1 Bit A12 set to “1”. When there is no read data burst from DRAM, the DQ I/O should be FLOATING.
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	8 fixed / MR0 Bits [A1, A0] = {0,0}
Active banks	one ACT-PRE loop	one ACT-RD-PRE loop
Idle banks	all other	all other
Precharge Power Down Mode / Mode Register Bit 12	n.a.	n.a.



< Figure 1. IDD1 Example > (DDR3-800-555, 512Mb x8): Data DQ is shown but the output buffer should be switched off (per MR1 Bit A12 ="1") to achieve Iout = 0mA. Address inputs are split into 3 parts.

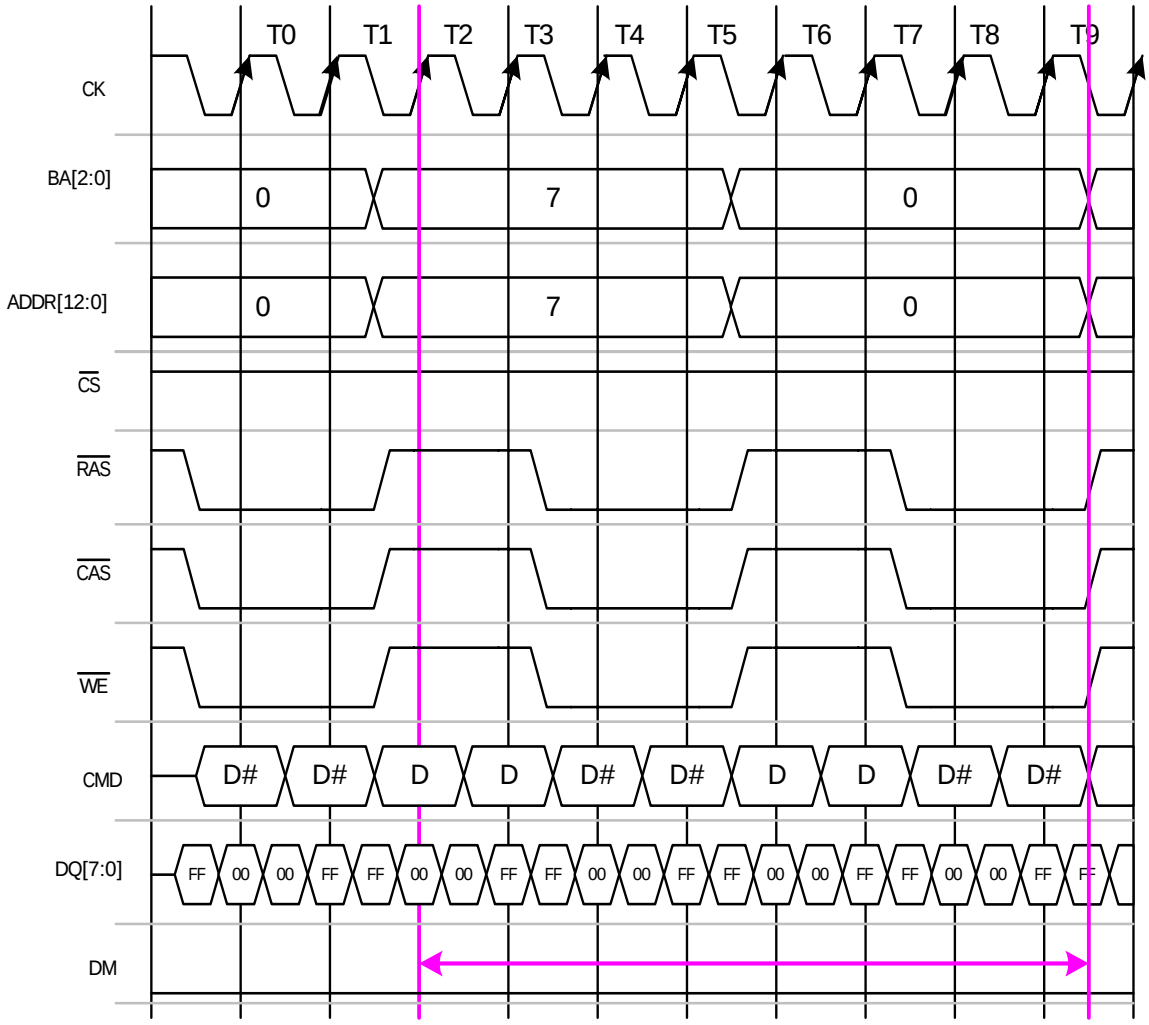
a. In DDR3, the MRS Bit 12 defines DLL on/off behaviour ONLY for precharge power down. There are 2 different Precharge Power Down states possible: one with DLL on (fast exit, bit 12 = 1) and one with DLL off (slow exit, bit 12 = 0).

b. Because it is an exit after precharge power down, the valid commands are: Activate, Refresh, Mode-Register Set, Enter - Self Refresh

Table 6 — IDD Measurement Conditions for IDD2N, IDD2P(1), IDD2P(0) and IDD2Q

Current	I_{DD2N}	$I_{DD2P}(1)$ [a]	$I_{DD2P}(0)$	I_{DD2Q}
Name	**Precharge Standby Current**	**Precharge Power Down Current Fast Exit - MRS A12 Bit = 1**	**Precharge Power Down Current Slow Exit - MRS A12 Bit = 0**	**Precharge Quiet Standby Current**
Measurement Condition				
Timing Diagram Example	Figure 2			
CKE	HIGH	LOW	LOW	HIGH
External Clock	on	on	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.	n.a.	n.a.
t_{RAS}	n.a.	n.a.	n.a.	n.a.
t_{RCD}	n.a.	n.a.	n.a.	n.a.
t_{RRD}	n.a.	n.a.	n.a.	n.a.
CL	n.a.	n.a.	n.a.	n.a.
AL	n.a.	n.a.	n.a.	n.a.
$\overline{CS}$	HIGH	STABLE	STABLE	HIGH
Bank Address, Row Addr. and Command Inputs	SWITCHING as described in Table 2	STABLE	STABLE	STABLE
Data inputs	SWITCHING	FLOATING	FLOATING	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	n.a.	n.a.	n.a.
Active banks	none	none	none	none
Idle banks	all	all	all	all
Precharge Power Down Mode / Mode Register Bit [a]	n.a.	Fast Exit / 1 (any valid command after tXP[b])	Slow Exit / 0 Slow exit (RD and ODT commands must satisfy tXPDLL-AL)	n.a.

a.
b.



<Figure 2. IDD2N / IDD3N Example > (DDR3-800-555, 512Mb x8)

Table 7 — IDD Measurement Conditions for IDD3N and IDD3P(fast exit)

Current	I_{DD3N}	I_{DD3P}
Name	**Active Standby Current**	**Active Power-Down Current[a] Always Fast Exit**
Measurement Condition		
Timing Diagram Example	Figure 2	
CKE	HIGH	LOW
External Clock	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.
t_{RAS}	n.a.	n.a.
t_{RCD}	n.a.	n.a.
t_{RRD}	n.a.	n.a.
CL	n.a.	n.a.
AL	n.a.	n.a.
$\overline{CS}$	HIGH	STABLE
Addr. and cmd Inputs	SWITCHING as described in Table 2	STABLE
Data inputs	SWITCHING as described in Table 3	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	n.a.
Active banks	all	all
Idle banks	none	none
Precharge Power Down Mode / Mode Register Bit [a]	n.a.	n.a. (Active Power Down Mode is always "Fast Exit" with DLL on

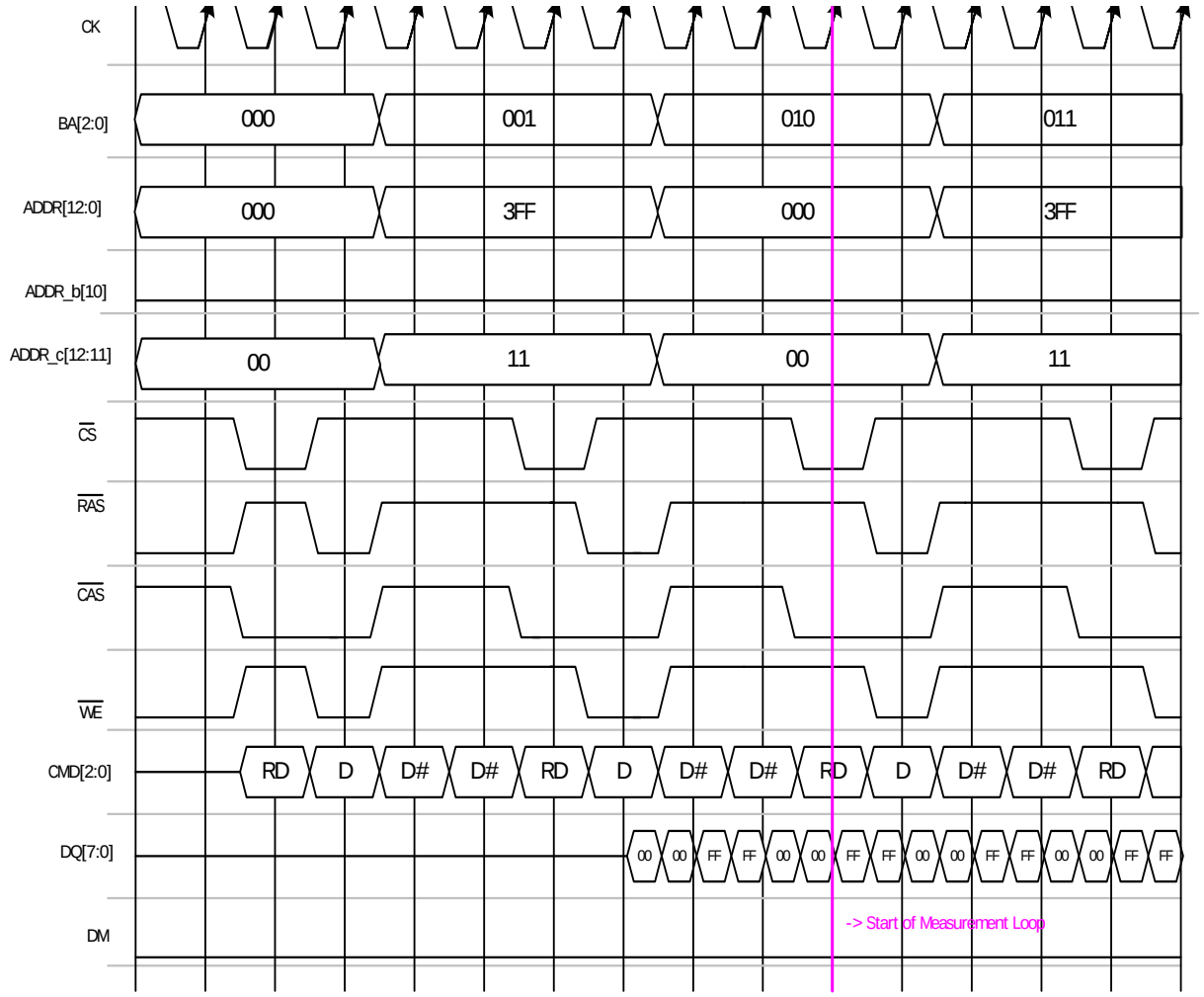
a. DDR3 will offer only ONE active power down mode with DLL on (-> fast exit). MRS bit 12 will not be used for active power down. Instead bit 12 will be used to switch between two different precharge power down modes.

Table 8 — IDD Measurement Conditions for IDD4R, IDD4W and IDD7

Current	I_{DD4R}	I_{DD4W}	I_{DD7}
Name	**Operating Current Burst Read**	**Operating Current Burst Write**	**All Bank Interleave Read Current**
Measurement Condition			
Timing Diagram Example	Figure 3		
CKE	HIGH	HIGH	HIGH
External Clock	on	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.	t_{RCmin}(IDD)
t_{RAS}	n.a.	n.a.	t_{RASmin}(IDD)
t_{RCD}	n.a.	n.a.	t_{RCDmin}(IDD)
t_{RRD}	n.a.	n.a.	t_{RRDmin}(IDD)
CL	CL(IDD)	CL(IDD)	CL(IDD)
AL	0	0	t_{RCDmin} - 1 t_{CK}
$\overline{CS}$	HIGH btw. valid cmds	HIGH btw. valid cmds	HIGH btw. valid cmds
Command Inputs ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	SWITCHING as described in Table 2; exceptions are Read commands => IDD4R Pattern: **R0**DDD**R1**D$\overline{D}$D**R2**DDD**R3**.DD $\overline{D}$ D **R4**..... Rx = Read from bank x; Definition of D and $\overline{D}$: see Table 2	SWITCHING as described in Table 2; exceptions are Write commands => IDD4W Pattern: **W0**DDD**W1**D$\overline{D}$D**W2**DDD**W3** DDD **W4**... Wx = Write to bank x; Definition of D and $\overline{D}$: see Table 2	For patterns see Table 9

Table 8 — IDD Measurement Conditions for IDD4R, IDD4W and IDD7

Current	I_{DD4R}	I_{DD4W}	I_{DD7}
Name	**Operating Current Burst Read**	**Operating Current Burst Write**	**All Bank Interleave Read Current**
Row, Column Addresses	column addresses SWITCHING as described in Table 2; Address Input A10 must be LOW all the time!	column addresses SWITCHING as described in Table 2; Address Input A10 must be LOW all the time!	STABLE during DESELECTs
Bank Addresses	bank address cycling (0 -> 1 -> 2 -> 3...)	bank address cycling (0 -> 1 -> 2 -> 3...)	bank address cycling (0 -> 1 -> 2 -> 3...), see pattern in Table 9
DQ I/O	Seamless Read Data Burst (BL8): output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA the output buffer should be switched off by MR1 Bit A12 set to “1”.	Seamless Write Data Burst (BL8): input data switches every clock, which means that Write data is stable during one clock cycle. DM is low all the time.	Read Data (BL8): output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA the output buffer should be switched off by MR1 Bit A12 set to “1”.
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]	disabled / [0,0]
Burst length	8 fixed / MR0 Bits [A1, A0] = {0,0}	8 fixed / MR0 Bits [A1, A0] = {0,0}	8 fixed / MR0 Bits [A1, A0] = {0,0}
Active banks	all	all	all, rotational
Idle banks	none	none	none
Precharge Power Down Mode / Mode Register Bit	n.a.	n.a.	n.a.



< Figure 3. IDD4R Example > (DDR3-800-555, 512Mb x8): data DQ is shown but the output buffer should be switched off (per MR1 Bit A12="1") to achieve Iout = 0mA. Address inputs are split into 3 parts.

Table 9 — IDD7 Pattern for different Speed Grades and different tRRD, tFAW conditions

Speed	Bin	Org.	tFAW	tFAW	tRRD	tRRD	IDD7 Pattern[a]
Mb/s			[ns]	[CLK]	[ns]	[CLK]	(Note this entire sequence is repeated.)
800	all	x4/x8	40	16	10	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D
	all	x16	50	20	10	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D
1066	all	x4/x8	37.5	20	7.5	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D
	all	x16	50	27	10	6	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D A4 RA4 D D D D A5 RA5 D D D D A6 RA6 D D D D A7 RA7 D D D D D D D
1333	all	x4/x8	30	20	6	4	A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D D D
	all	x16	45	30	7.5	5	A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D D D D D D D A4 RA4 D D D A5 RA5 D D D A6 RA6 D D D A7 RA7 D D D D D D D D D D D D
1600	all	x4/x8	30	24	6	5	A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D A4 RA4 D D D A5 RA5 D D D A6 RA6 D D D A7 RA7 D D D D D D D
	all	x16	40	32	7.5	6	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D D D D A3 RA3 D D D D D D D D D D A4 RA4 D D D D A5 RA5 D D D D A6 RA6 D D D D A7 RA7 D D D D D D D D D D D

a. A0 = Activation of Bank 0; RA0 = Read with Auto-Precharge of Bank 0; D = Deselect

Table 10 — IDD Measurement Conditions for IDD5B

Current	I_{DD5B}
Name	**Burst Refresh Current**
Measurement Condition	
CKE	HIGH
External Clock	on
t_{CK}	t_{CKmin}(IDD)
t_{RC}	n.a.
t_{RAS}	n.a.
t_{RCD}	n.a.
t_{RRD}	n.a.
t_{RFC}	t_{RFCmin}(IDD)
CL	n.a.
AL	n.a.
$\overline{CS}$	HIGH btw. valid cmds
Addr. and cmd Inputs	SWITCHING
Data inputs	SWITCHING
Output Buffer DQ,DQS / MR1 bit A12	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]
Burst length	n.a.
Active banks	Refresh command every tRFC=tRFCmin
Idle banks	none
Precharge Power Down Mode / Mode Register Bit	n.a.

Table 11 — IDD Measurement Conditions for IDD6 and IDD6ET

Current	I_{DD6}	I_{DD6ET}
Name	**Self-Refresh Current Normal Temperature Range** T_{CASE} = 0. 85 °C	**Self-Refresh Current Extended Temperature Range** [a] T_{CASE} = 0. 95 °C
Measurement Condition		
Temperature	T_{CASE} = 85 °C	T_{CASE} = 95 °C
Auto Self Refresh (ASR) / MR2 Bit A6	Disabled / “0”	Disabled / “0”
Self Refresh Temperature Range (SRT) / MR2 Bit A7	Normal / “0”	Extended / “1”
CKE	LOW	LOW
External Clock	OFF; CK and $\overline{CK}$ at LOW	OFF; CK and $\overline{CK}$ at LOW
t_{CK}	n.a.	n.a.
t_{RC}	n.a.	n.a.
t_{RAS}	n.a.	n.a.
t_{RCD}	n.a.	n.a.
t_{RRD}	n.a.	n.a.
CL	n.a.	n.a.
AL	n.a.	n.a.
$\overline{CS}$	FLOATING	FLOATING
Command Inputs ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	FLOATING	FLOATING
Row, Column Addresses	FLOATING	FLOATING
Bank Addresses	FLOATING	FLOATING
Data I/O	FLOATING	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1
ODT / MR1 bits [A6, A2]	disabled / [0,0]	disabled / [0,0]
Burst length	n.a.	n.a.
Active banks	all during self-refresh actions	all during self-refresh actions
Idle banks	all btw. Self-Refresh actions	all btw. Self-Refresh actions
Precharge Power Down Mode / MR0 bit A12	n.a.	n.a.

a. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

7. Electrical Characteristics and AC Timing

7.1 Refresh Parameters by Device Density

Parameter	Symbol		512Mb	1Gb	2Gb	4Gb	8Gb	Units
REF command to ACT or REF command time	tRFC		90	110	160	300	350	ns
Average periodic refresh interval	tREFI	0 ×C < T_{CASE} < 85 ×C	7.8	7.8	7.8	7.8	7.8	ms
		85 ×C < T_{CASE} < 95 ×C	3.9	3.9	3.9	3.9	3.9	ms

7.2 DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin

DDR3 800 Speed Bin			DDR3-800D		DDR3-800E		Unit	Notes
CL - nRCD - nRP			5-5-5		6-6-6			
Parameter		Symbol	min	max	min	max		
Internal read command to first data		t_{AA}	12.5	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	12.5	—	15	—	ns	
PRE command period		t_{RP}	12.5	—	15	—	ns	
ACT to ACT or REF command period		t_{RC}	50	—	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	Reserved		ns	1)2)3)4)
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	ns	1)2)3)
Supported CL Settings			5, 6		6		n_{CK}	
Supported CWL Settings			5		5		n_{CK}	

DDR3 1066 Speed Bin			DDR3-1066E		DDR3-1066F		DDR3-1066G		Unit	Note
CL - nRCD - nRP			6-6-6		7-7-7		8-8-8			
Parameter		Symbol	min	max	min	max	min	max		
Internal read command to first data		t_{AA}	11.25	20	13.125	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	11.25	—	13.125	—	15	—	ns	
PRE command period		t_{RP}	11.25	—	13.125	—	15	—	ns	
ACT to ACT or REF command period		t_{RC}	48.75	—	50.625	—	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	37.5	9 * tREFI	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	Reserved		Reserved		ns	1)2)3)4)6)
	CWL = 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4)
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	ns	1)2)3)6)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	Reserved		Reserved		ns	1)2)3)4)
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		ns	1)2)3)4)
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1)2)3)
Supported CL Settings			5, 6, 7, 8		6, 7, 8		6, 8		n_{CK}	
Supported CWL Settings			5, 6		5, 6		5, 6		n_{CK}	

DDR3 1333 Speed Bin			DDR3-1333F (optional)		DDR3-1333G		DDR3-1333H		DDR3-1333J (optional)		Unit	Note
CL - nRCD - nRP			7-7-7		8-8-8		9-9-9		10-10-10			
Parameter		Symbol	min	max	min	max	min	max	min	max		
Internal read command to first		t_{AA}	10.5	20	12	20	13.5	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	10.5	—	12	—	13.5	—	15	—	ns	
PRE command period		t_{RP}	10.5	—	12	—	13.5	—	15	—	ns	
ACT to ACT or REF command period		t_{RC}	46.5	—	48	—	49.5	—	51	—	ns	
ACT to PRE command period		t_{RAS}	36	9 * tREFI	36	9 * tREFI	36	9 * tREFI	36	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	Reserved		Reserved		ns	1,2,3,4,7
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,7
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	Reserved		Reserved		Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	Reserved		Reserved		Reserved		ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,7
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	Reserved		Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	Reserved		ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	1,2,3
			(Optional)		(Optional)		(Optional)				ns	5
Supported CL Settings			5, 6, 7, 8, 9		5, 6, 7, 8, 9		6, 8, 9		6, 8, 10		n_{CK}	
Supported CWL Settings			5, 6, 7		5, 6, 7		5, 6, 7		5, 6, 7		n_{CK}	

DDR3 1600 Speed Bin			DDR3-1600G (optional)		DDR3-1600H		DDR3-1600J		DDR3-1600K (optional)		Unit	Note
CL - nRCD - nRP			8-8-8		9-9-9		10-10-10		11-11-11			
Parameter		Symbol	min	max	min	max	min	max	min	max		
Internal read command to first data		t_{AA}	10	20	11.25	20	12.5	20	13.75	20	ns	
ACT to internal read or write delay time		t_{RCD}	10	—	11.25	—	12.5	—	13.75	—	ns	
PRE command period		t_{RP}	10	—	11.25	—	12.5	—	13.75	—	ns	
ACT to ACT or REF command period		t_{RC}	45	—	46.25	—	47.5	—	48.75	—	ns	
ACT to PRE command period		t_{RAS}	35	9 * tREFI	35	9 * tREFI	35	9 * tREFI	35	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	Reserved		ns	1,2,3,4,8
	CWL = 6, 7, 8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,8
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		Reserved		ns	1,2,3,4,8
	CWL = 7, 8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	Reserved		ns	1,2,3,4,8
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	Reserved		Reserved		Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,8
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	Reserved		Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	Reserved		Reserved		Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	Reserved		Reserved		ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	1,2,3,8
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	Reserved		ns	1,2,3,4

CL = 11	CWL = 5, 6, 7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	ns	1,2,3
			(Optional)		(Optional)		(Optional)				ns	5
Supported CL Settings			5, 6, 7, 8, 9, 10		5, 6, 7, 8, 9, 10		5, 6, 7, 8, 9, 10		6, 8, 10, 11		n_{CK}	
Supported CWL Settings			5, 6, 7, 8		5, 6, 7, 8		5, 6, 7, 8		5, 6, 7, 8		n_{CK}	

Speed Bin Table Notes

Absolute Specification (T_{OPER}; V_{DDQ} = V_{DD} = 1.5V +/- 0.075 V);

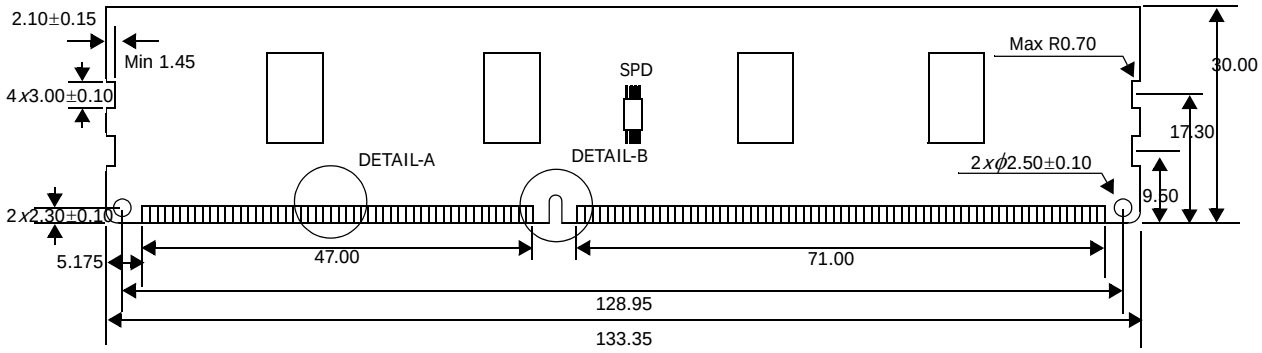
Notes:

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL'.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CLSELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CLSELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

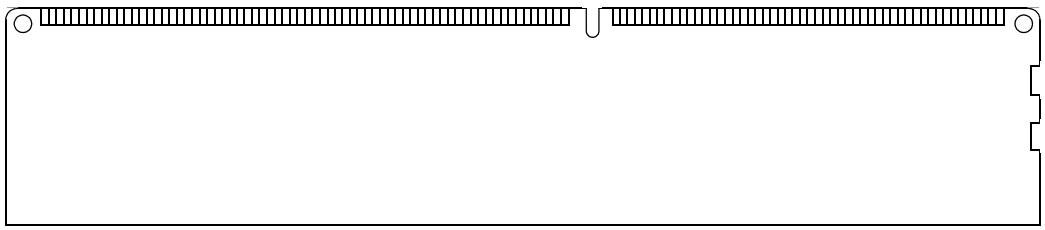
8. Dimm Outline Diagram

8.1 164Mx64 - HMT164U6AFP(R)6C

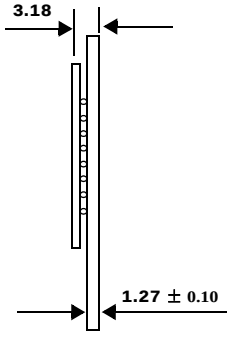
Front



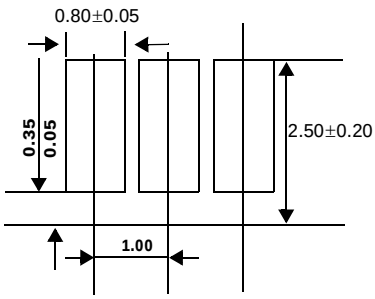
Back



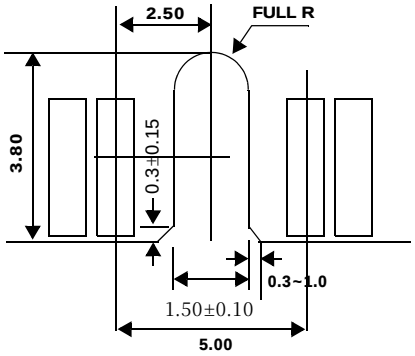
Side



Detail - A

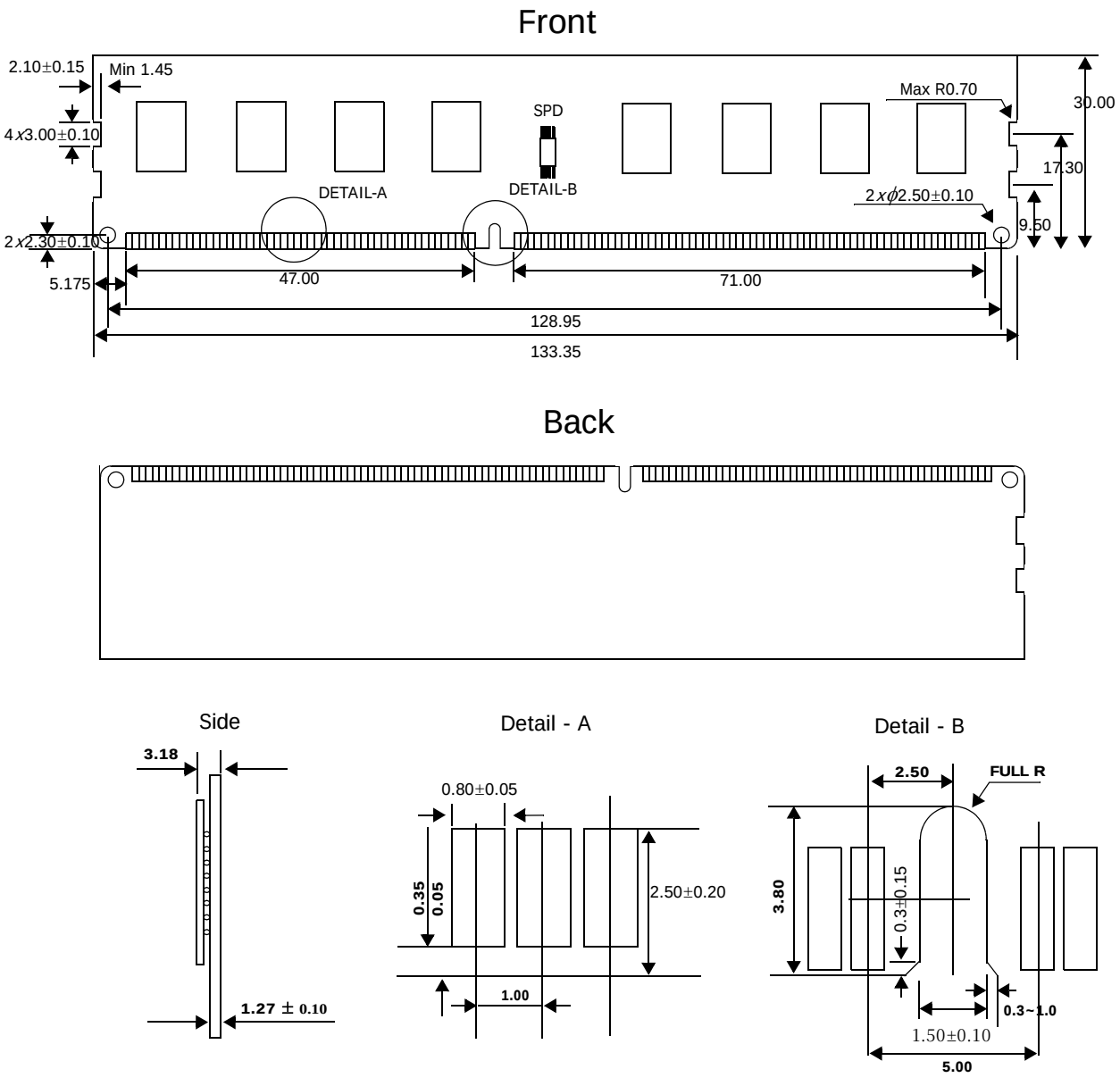


Detail - B



Note) All dimensions are in millimeters unless otherwise stated.

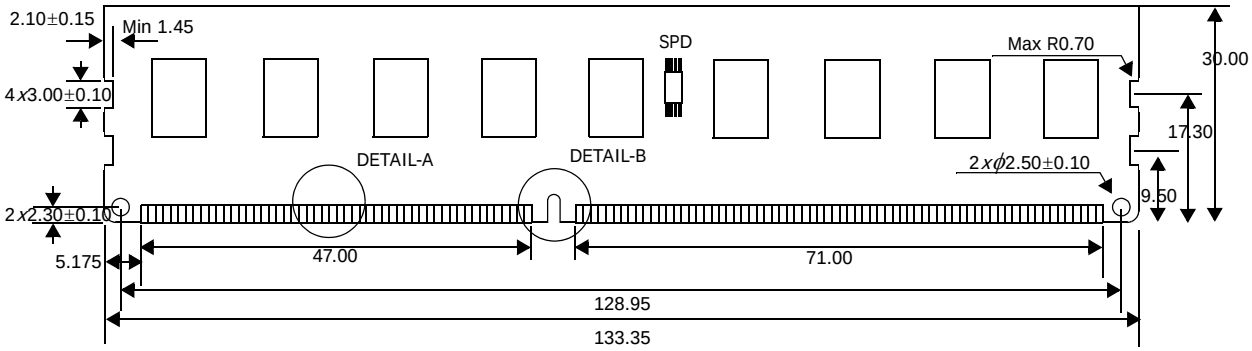
8.2 128Mx64 - HMT112U6AFP(R)8C



Note) All dimensions are in millimeters unless otherwise stated.

8.3 128Mx72 - HMT112U7AFP(R)8C

Front



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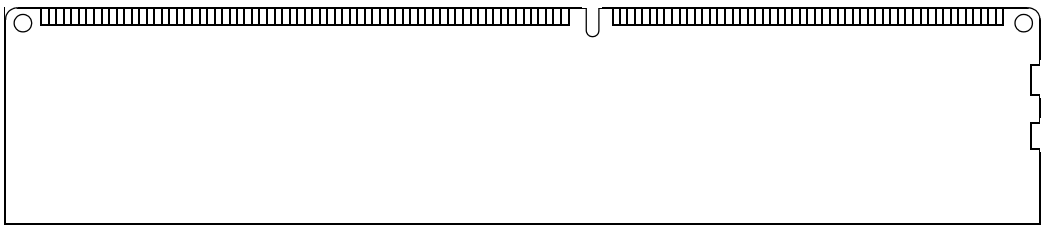
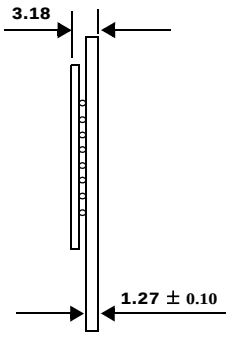
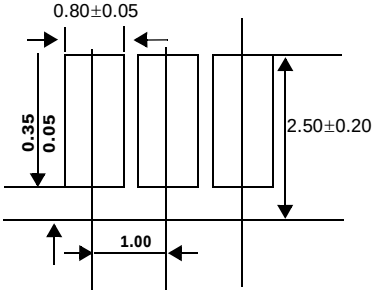


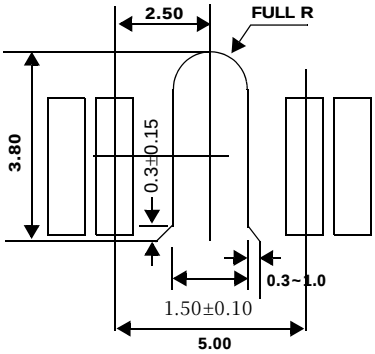
Side



Detail - A



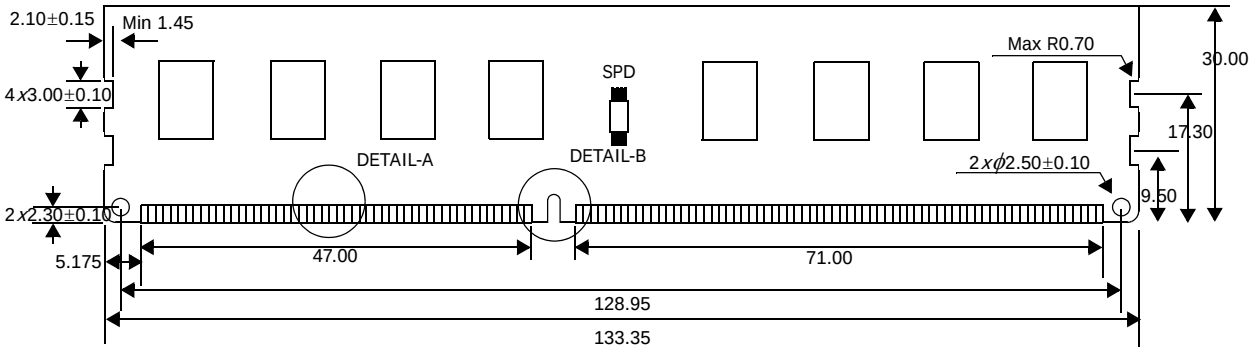
Detail - B



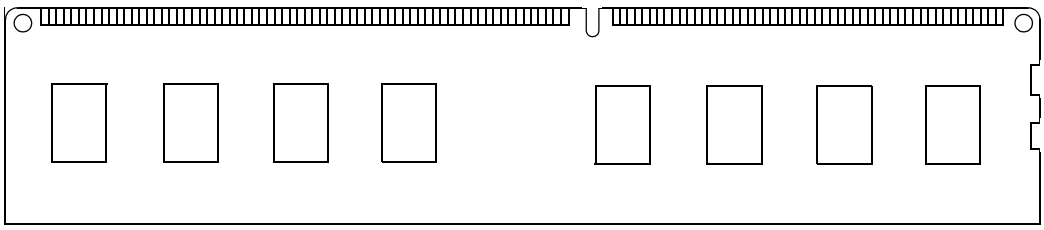
Note) All dimensions are in millimeters unless otherwise stated.

8.4 256Mx64 - HMT125U6AFP(R)8C

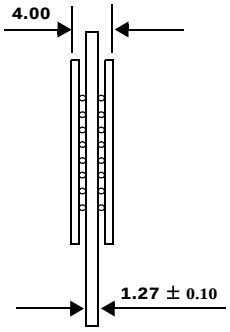
Front



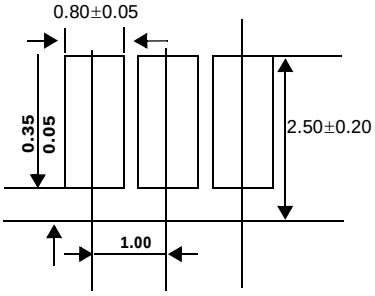
Back



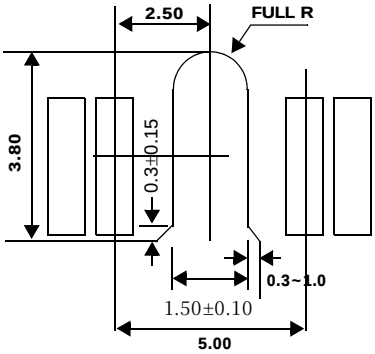
Side



Detail - A



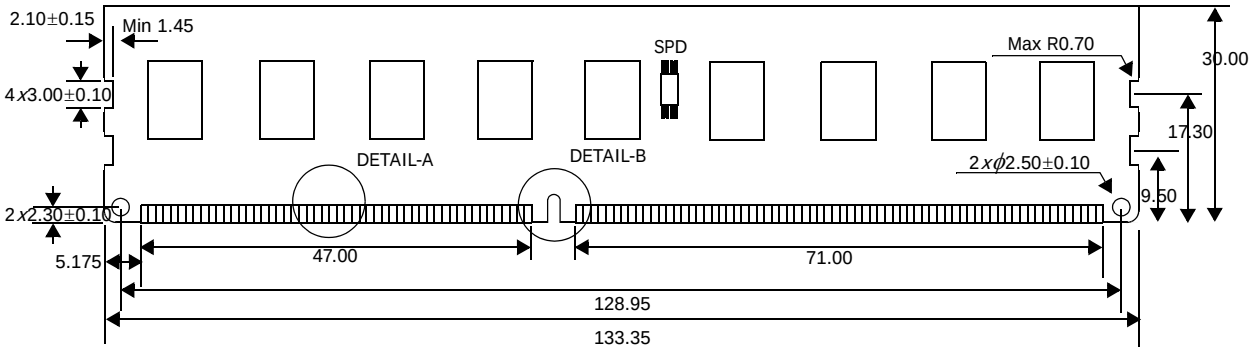
Detail - B



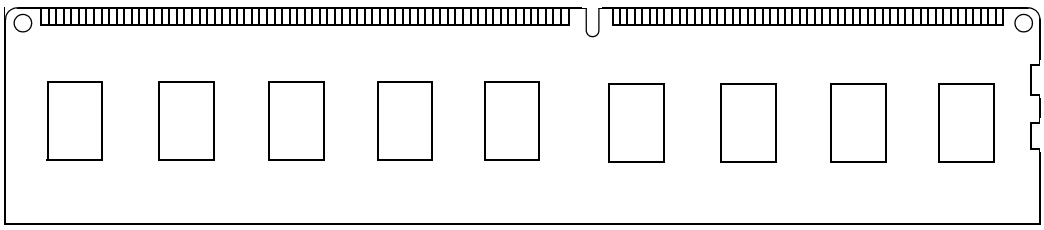
Note) All dimensions are in millimeters unless otherwise stated.

8.5 256Mx72 - HMT125U7AFP(R)8C

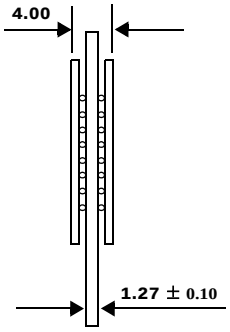
Front



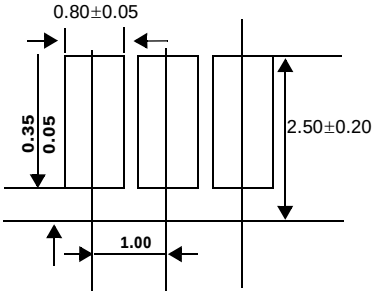
Back



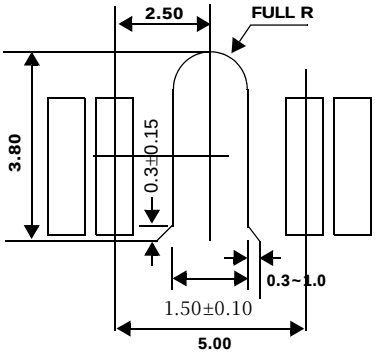
Side



Detail - A



Detail - B



Note) All dimensions are in millimeters unless otherwise stated.