DDR3L SDRAM Unbuffered DIMMs Based on 4Gb C-Die

HMT425U6CFR6A

*SK hynix reserves the right to change products or specifications without notice.

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Release	Aug. 2014	
1.0	IDD Specification update	Nov. 2014	

Description

SK hynix Unbuffered DDR3L SDRAM DIMMs (Unbuffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules) are low power, high-speed operation memory modules that use DDR3L SDRAM devices. These Unbuffered SDRAM DIMMs are intended for use as main memory when installed in systems such as PCs and workstations.

Feature

- Power Supply: VDD=1.35V (1.283V to 1.45V)
- VDDQ=1.35V (1.283 to 1.45V)
- VDDSPD=3.0V to 3.6V
- Backward Compatible with 1.5V DDR3 Memory module
- 8 internal banks
- Data transfer rates: PC3-14900. PC3-12800, PC3-10600, PC3-8500
- Bi-directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly: BL 8 or BC (Burst Chop) 4
- Supports ECC error correction and detection
- On Die Termination (ODT) supported
- Temperature sensor with integrated SPD (Serial Presence Detect) EEPROM
- This product is in Compliance with the RoHS directive

Ordering Information

Part Number	Density	Organization	Component Composition	# of ranks	FDHS
HMT425U6CFR6A-G7/H9/PB	2GB	256Mx64	256Mx16(H5TC4G63CFR)*4	1	X

Key Parameters

MT/s	Grade	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
DDR3L-1066	-G7	1.875	7	13.125	13.125	37.5	50.625	7-7-7
DDR3L-1333	-H9	1.5	9	13.5 (13.125)*	13.5 (13.125)*	36	49.5 (49.125)*	9-9-9
DDR3L-1600	-PB	1.25	11	13.75 (13.125)*	13.75 (13.125)*	35	48.75 (48.125)*	11-11-11
DDR3L-1866	-Rd	1.07	13	13.91 (13.125)*	13.91 (13.125)*	34	47.91 (48.125)*	13-13-13

*SK hynix DRAM devices support optional downbinning to CL11, CL9 and CL7. SPD setting is programmed to match.

Speed Grade

Grade	Frequency [Mbps]								Remark
	CL6	CL7	CL8	CL9	CL10	CL11	CL12	CL13	
-G7	800	1066	1066						
-H9	800	1066	1066	1333	1333				
-PB	800	1066	1066	1333	1333	1600			
-RD	800	1066	1066	1333	1333	1600		1866	

Address Table

	2GB(1Rx16)
Refresh Method	8K/64ms
Row Address	A0-A14
Column Address	A0-A9
Bank Address	BA0-BA2
Page Size	2KB

Pin Descriptions

Pin Name	Description	Pin Name	Description
A0–A15	SDRAM address bus	SCL	I^2C serial bus clock for EEPROM
BA0–BA2	SDRAM bank select	SDA	I^2C serial bus data line for EEPROM
$\overline{RAS}$	SDRAM row address strobe	SA0–SA2	I^2C slave address select for EEPROM
$\overline{CAS}$	SDRAM column address strobe	V_{DD}*	SDRAM core power supply
$\overline{WE}$	SDRAM write enable	$V_{DD}Q$*	SDRAM I/O Driver power supply
$\overline{S0}$–$\overline{S1}$	DIMM Rank Select Lines	$V_{REF}DQ$	SDRAM I/O reference supply
CKE0–CKE1	SDRAM clock enable lines	$V_{REF}CA$	SDRAM command/address reference supply
ODT0–ODT1	On-die termination control lines	V_{SS}	Power supply return (ground)
DQ0–DQ63	DIMM memory data bus	V_{DDSPD}	Serial EEPROM positive power supply
CB0–CB7	DIMM ECC check bits	NC	Spare pins (no connect)
DQS0–DQS8	SDRAM data strobes (positive line of differential pair)	TEST	Memory bus analysis tools (unused on memory DIMMS)
$\overline{DQS0}$–$\overline{DQS8}$	SDRAM data strobes (negative line of differential pair)	RESET	Set DRAMs to Known State
DM0–DM8	SDRAM data masks/high data strobes (x8-based x72 DIMMs)	V_{TT}	SDRAM I/O termination supply
CK0–CK1	SDRAM clocks (positive line of differential pair)	RSVD	Reserved for future use
$\overline{CK0}$–$\overline{CK1}$	SDRAM clocks (negative line of differential pair)	-	-
***The V_{DD} and $V_{DD}Q$ pins are tied common to a single power-plane on these designs**			

Input/Output Functional Descriptions

Symbol	Type	Polarity	Function
CK0–CK1 $\overline{CK0}$–$\overline{CK1}$	SSTL	Differential crossing	CK and $\overline{CK}$ are differential clock inputs. All the DDR3 SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is reference to the crossing of CK and $\overline{CK}$ (Both directions of crossing).
CKE0–CKE1	SSTL	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{S0}$–$\overline{S1}$	SSTL	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	SSTL	Active Low	$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (ALONG WITH $\overline{S}$) define the command being entered.
ODT0–ODT1	SSTL	Active High	When high, termination resistance is enabled for all DQ, DQS, $\overline{DQS}$ and DM pins, assuming this function is enabled in the Mode Register 1 (MR1).
V_{REF}DQ	Supply		Reference voltage for SSTL15 I/O inputs.
V_{REF}CA	Supply		Reference voltage for SSTL 15 command/address inputs.
V_{DD}Q	Supply		Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For all current DDR3 unbuffered DIMM designs, V_{DD}Q shares the same power plane as V_{DD} pins.
BA0–BA2	SSTL	—	Selects which SDRAM bank of eight is activated.
A0–A15	SSTL	—	During a Bank Activate command cycle, Address input defines the row address (RA0–RA15). During a Read or Write command cycle, Address input defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12($\overline{BC}$) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped).
DQ0–DQ63, CB0–CB7	SSTL	—	Data and Check Bit Input/Output pins.
DM0–DM8	SSTL	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR3 SDRAM input buffers, and core logic. V_{DD} and V_{DD}Q pins are tied to V_{DD}/V_{DD}Q planes on these modules.

Symbol	Type	Polarity	Function
$\overline{DQS0}$–$\overline{DQS8}$ DQS0–DQS8	SSTL	Differential crossing	Data strobe for input and output data.
SA0–SA2		—	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA		—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to V_{DDSPD} to act as a pullup on the system board.
SCL		—	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to V_{DDSPD} to act as a pullup on the system board.
V_{DDSPD}	Supply		Power supply for SPD EEPROM. This supply is separate from the V_{DD}/V_{DD}Q power plane. EEPROM supply is operable from 3.0V to 3.6V.

Pin Assignments

Front Side(left 1–60)			Back Side(right 121–180)			Front Side(left 61–120)			Back Side(right 181–240)		
Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC
1	$V_{REF}DQ$	$V_{REF}DQ$	121	V_{SS}	V_{SS}	61	A2	A2	181	A1	A1
2	V_{SS}	V_{SS}	122	DQ4	DQ4	62	V_{DD}	V_{DD}	182	V_{DD}	V_{DD}
3	DQ0	DQ0	123	DQ5	DQ5	63	CK1	CK1	183	V_{DD}	V_{DD}
4	DQ1	DQ1	124	V_{SS}	V_{SS}	64	$\overline{CK}1$	$\overline{CK}1$	184	CK0	CK0
5	V_{SS}	V_{SS}	125	DM0	DM0	65	V_{DD}	V_{DD}	185	$\overline{CK}0$	$\overline{CK}0$
6	$\overline{DQS}0$	$\overline{DQS}0$	126	NC	NC	66	V_{DD}	V_{DD}	186	V_{DD}	V_{DD}
7	DQS0	DQS0	127	V_{SS}	V_{SS}	67	$V_{REF}CA$	$V_{REF}CA$	187	NC	$\overline{EVENT}$
8	V_{SS}	V_{SS}	128	DQ6	DQ6	68	NC	NC	188	A0	A0
9	DQ2	DQ2	129	DQ7	DQ7	69	V_{DD}	V_{DD}	189	V_{DD}	V_{DD}
10	DQ3	DQ3	130	V_{SS}	V_{SS}	70	A10	A10	190	$BA1^2$	$BA1^2$
11	V_{SS}	V_{SS}	131	DQ12	DQ12	71	$BA0^2$	$BA0^2$	191	V_{DD}	V_{DD}
12	DQ8	DQ8	132	DQ13	DQ13	72	V_{DD}	V_{DD}	192	$\overline{RAS}$	$\overline{RAS}$
13	DQ9	DQ9	133	V_{SS}	V_{SS}	73	$\overline{WE}$	$\overline{WE}$	193	$\overline{S}0$	$\overline{S}0$
14	V_{SS}	V_{SS}	134	DM1	DM1	74	$\overline{CAS}$	$\overline{CAS}$	194	V_{DD}	V_{DD}
15	$\overline{DQS}1$	$\overline{DQS}1$	135	NC	NC	75	V_{DD}	V_{DD}	195	ODT0	ODT0
16	DQS1	DQS1	136	V_{SS}	V_{SS}	76	S1	S1	196	A13	A13
17	V_{SS}	V_{SS}	137	DQ14	DQ14	77	ODT1	ODT1	197	V_{DD}	V_{DD}
18	DQ10	DQ10	138	DQ15	DQ15	78	V_{DD}	V_{DD}	198	NC	NC
19	DQ11	DQ11	139	V_{SS}	V_{SS}	79	NC	NC	199	V_{SS}	V_{SS}
20	V_{SS}	V_{SS}	140	DQ20	DQ20	80	V_{SS}	V_{SS}	200	DQ36	DQ36
21	DQ16	DQ16	141	DQ21	DQ21	81	DQ32	DQ32	201	DQ37	DQ37
22	DQ17	DQ17	142	V_{SS}	V_{SS}	82	DQ33	DQ33	202	V_{SS}	V_{SS}
23	V_{SS}	V_{SS}	143	DM2	DM2	83	V_{SS}	V_{SS}	203	DM4	DM4
24	$\overline{DQS}2$	$\overline{DQS}2$	144	$\overline{NC}$	$\overline{NC}$	84	$\overline{DQS}4$	$\overline{DQS}4$	204	NC	NC
25	DQS2	DQS2	145	V_{SS}	V_{SS}	85	DQS4	DQS4	205	V_{SS}	V_{SS}
26	V_{SS}	V_{SS}	146	DQ22	DQ22	86	V_{SS}	V_{SS}	206	DQ38	DQ38
27	DQ18	DQ18	147	DQ23	DQ23	87	DQ34	DQ34	207	DQ39	DQ39
28	DQ19	DQ19	148	V_{SS}	V_{SS}	88	DQ35	DQ35	208	V_{SS}	V_{SS}
29	V_{SS}	V_{SS}	149	DQ28	DQ28	89	V_{SS}	V_{SS}	209	DQ44	DQ44
30	DQ24	DQ24	150	DQ29	DQ29	90	DQ40	DQ40	210	DQ45	DQ45

NC = No Connect; RFU = Reserved Future Use

1. NC pins should not be connected to anything on the DIMM, including bussing within the NC group.
2. Address pins A3–A8 and BA0 and BA1 can be mirrored or not mirrored.

Front Side(left 1–60)			Back Side(right 121–180)			Front Side(left 61–120)			Back Side(right 181–240)		
Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC	Pin #	x64 Non-ECC	x72 ECC
31	DQ25	DQ25	151	VSS	VSS	91	DQ41	DQ41	211	VSS	VSS
32	VSS	VSS	152	DM3	DM3	92	VSS	VSS	212	DM5	DM5
33	$\overline{DQS3}$	$\overline{DQS3}$	153	NC	NC	93	$\overline{DQS5}$	$\overline{DQS5}$	213	NC	NC
34	DQS3	DQS3	154	VSS	VSS	94	DQS5	DQS5	214	VSS	VSS
35	VSS	VSS	155	DQ30	DQ30	95	VSS	VSS	215	DQ46	DQ46
36	DQ26	DQ26	156	DQ31	DQ31	96	DQ42	DQ42	216	DQ47	DQ47
37	DQ27	DQ27	157	VSS	VSS	97	DQ43	DQ43	217	VSS	VSS
38	VSS	VSS	158	NC	CB4	98	VSS	VSS	218	DQ52	DQ52
39	NC	CB0	159	NC	CB5	99	DQ48	DQ48	219	DQ53	DQ53
40	NC	CB1	160	VSS	VSS	100	DQ49	DQ49	220	VSS	VSS
41	VSS	VSS	161	DM8	DM8	101	VSS	VSS	221	DM6	DM6
42	NC	$\overline{DQS8}$	162	NC	NC	102	$\overline{DQS6}$	$\overline{DQS6}$	222	NC	NC
43	NC	DQS8	163	VSS	VSS	103	DQS6	DQS6	223	VSS	VSS
44	VSS	VSS	164	NC	CB6	104	VSS	VSS	224	DQ54	DQ54
45	NC	CB2	165	NC	CB7	105	DQ50	DQ50	225	DQ55	DQ55
46	NC	CB3	166	VSS	VSS	106	DQ51	DQ51	226	VSS	VSS
47	VSS	VSS	167	NC	NC	107	VSS	VSS	227	DQ60	DQ60
48	NC	NC	168	Reset	Reset	108	DQ56	DQ56	228	DQ61	DQ61
KEY			KEY			109	DQ57	DQ57	229	VSS	VSS
49	NC	NC	169	CKE1/NC	CKE1/NC	110	VSS	VSS	230	DM7	DM7
50	CKE0	CKE0	170	VDD	VDD	111	$\overline{DQS7}$	$\overline{DQS7}$	231	NC	NC
51	VDD	VDD	171	NC	NC	112	DQS7	DQS7	232	VSS	VSS
52	BA2	BA2	172	A14	A14	113	VSS	VSS	233	DQ62	DQ62
53	NC	NC	173	VDD	VDD	114	DQ58	DQ58	234	DQ63	DQ63
54	VDD	VDD	174	A12	A12	115	DQ59	DQ59	235	VSS	VSS
55	All	All	175	A9	A9	116	VSS	VSS	236	VDDSPD	VDDSPD
56	A7[2]	A7[2]	176	VDD	VDD	117	SA0	SA0	237	SA1	SA1
57	VDD	VDD	177	A8[2]	A8[2]	118	SCL	SCL	238	SDA	SDA
58	A5[2]	A5[2]	178	A6[2]	A6[2]	119	SA2	SA2	239	VSS	VSS
59	A4[2]	A4[2]	179	VDD	VDD	120	VTT	VTT	240	VTT	VTT
60	VDD	VDD	180	A3[2]	A3[2]						

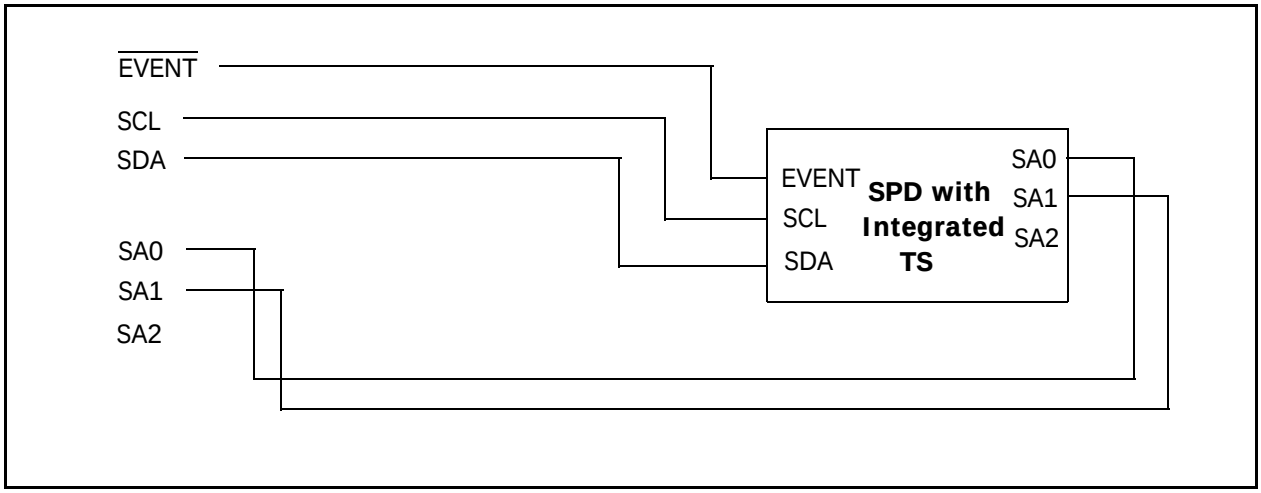
NC = No Connect; RFU = Reserved Future Use

1. NC pins should not be connected to anything on the DIMM, including bussing within the NC group.
2. Address pins A3–A8 and BA0 and BA1 can be mirrored or not mirrored.

On DIMM Thermal Sensor

The DDRL3 SDRAM DIMM temperature is monitored by integrated thermal sensor. The integrated thermal sensor comply with JEDEC “TSE2002av, Serial Presence Detect with Temperature Sensor”.

Connection of Thermal Sensor

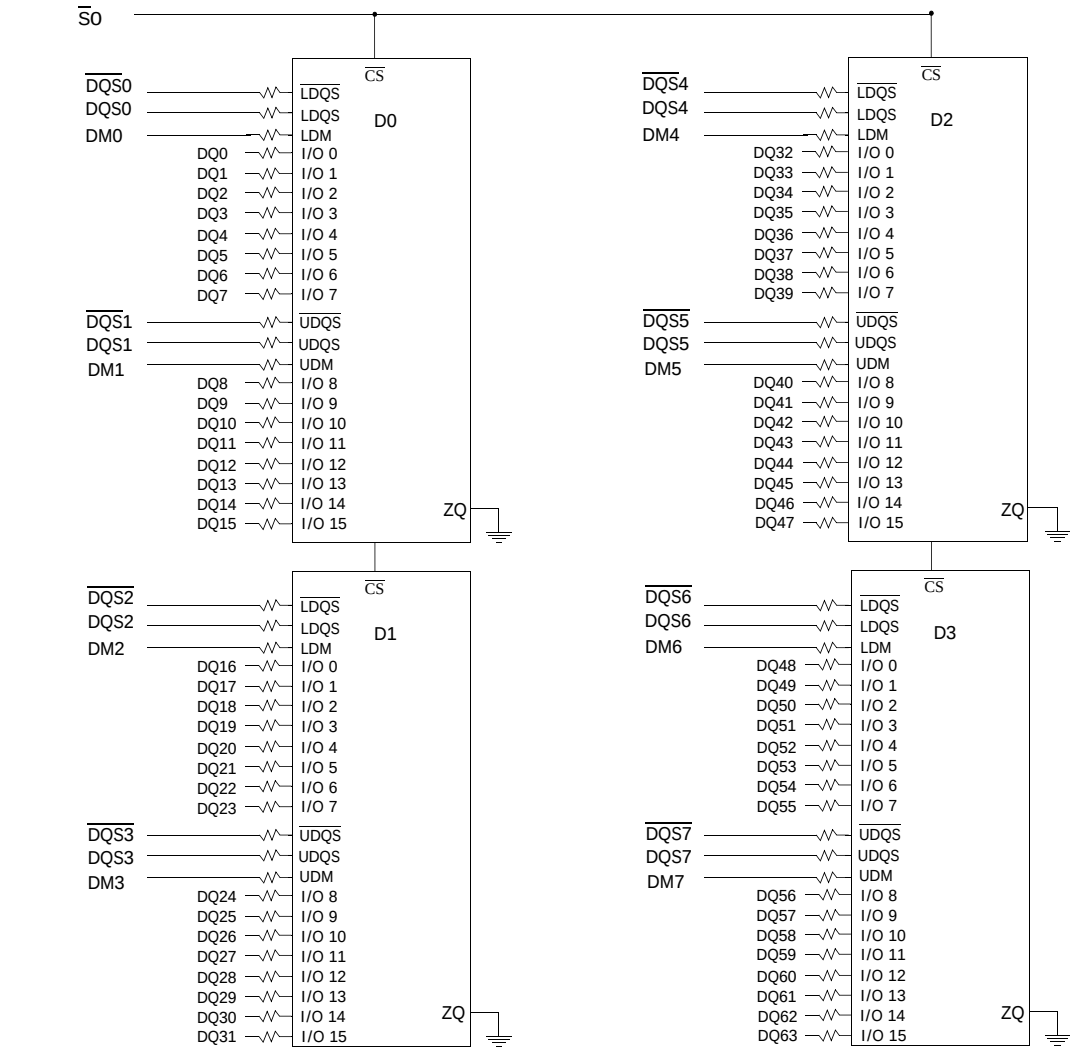


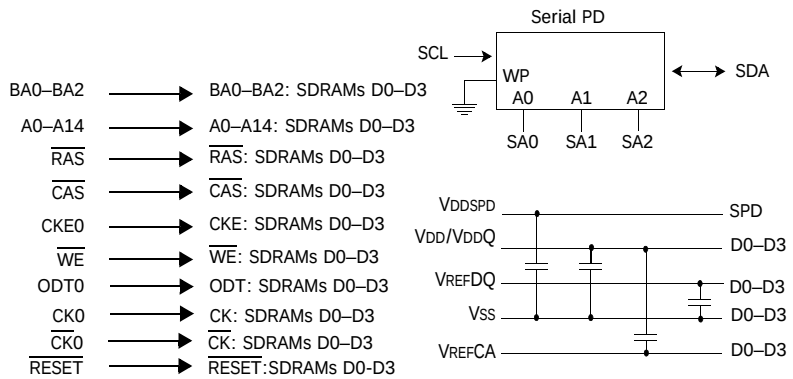
Temperature-to-Digital Conversion Performance

Parameter	Condition	Min	Typ	Max	Unit
Temperature Sensor Accuracy (Grade B)	Active Range, 75°C < T_A < 95°C	-	± 0.5	± 1.0	°C
	Monitor Range, 40°C < T_A < 125°C	-	± 1.0	± 2.0	°C
	-20°C < T_A < 125°C	-	± 2.0	± 3.0	°C
Resolution			0.25		°C

Functional Block Diagram

2GB, 256Mx64 Module(1Rank of x16)





Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. DQ,DM,DQS,DQS resistors;Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of this document.
5. The pair CK1 and CK1# is terminated in 75ohm but is not used on the module.
6. A15 is not routed on the module.
7. For each DRAM, a unique ZQ resistor is connected to ground.The ZQ resistor is 240ohm+-1%
8. One SPD exists per module.

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.8 V	V	1, 3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.8 V	V	1, 3
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.4 V ~ 1.8 V	V	1
T_{STG}	Storage Temperature	-55 to +100	^{o}C	1, 2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

DRAM Component Operating Temperature Range

Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	^{o}C	1,2
	Extended Temperature Range	85 to 95	^{o}C	1,3

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85^{o}C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85^{o}C and 95^{o}C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
   b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b). DDR3 SDRAMs support Extended Temperature Range and please refer to component datasheet and/or the DIMM SPD for tFEFI requirements in the Extended Temperature Range.

AC & DC Operating Conditions

Recommended DC Operating Conditions

Recommended DC Operating Conditions - DDR3L (1.35V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.283	1.35	1.45	V	1,2,3,4
VDDQ	Supply Voltage for Output	1.283	1.35	1.45	V	1,2,3,4

Notes:

1. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDDQ (t) over a very long period of time (e.g., 1 sec).
2. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
3. Under these supply voltages, the device operates to this DDR3L specification.
4. Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3 operation (see Figure 0).

Recommended DC Operating Conditions - - DDR3 (1.5V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2,3
VDDQ	Supply Voltage for Output	1.425	1.5	1.575	V	1,2,3

Notes:

1. If minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
2. Under 1.5V operation, this DDR3L device operates to the DDR3 specifications under the same speed timings as defined for this device.
3. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation (see Figure 0).

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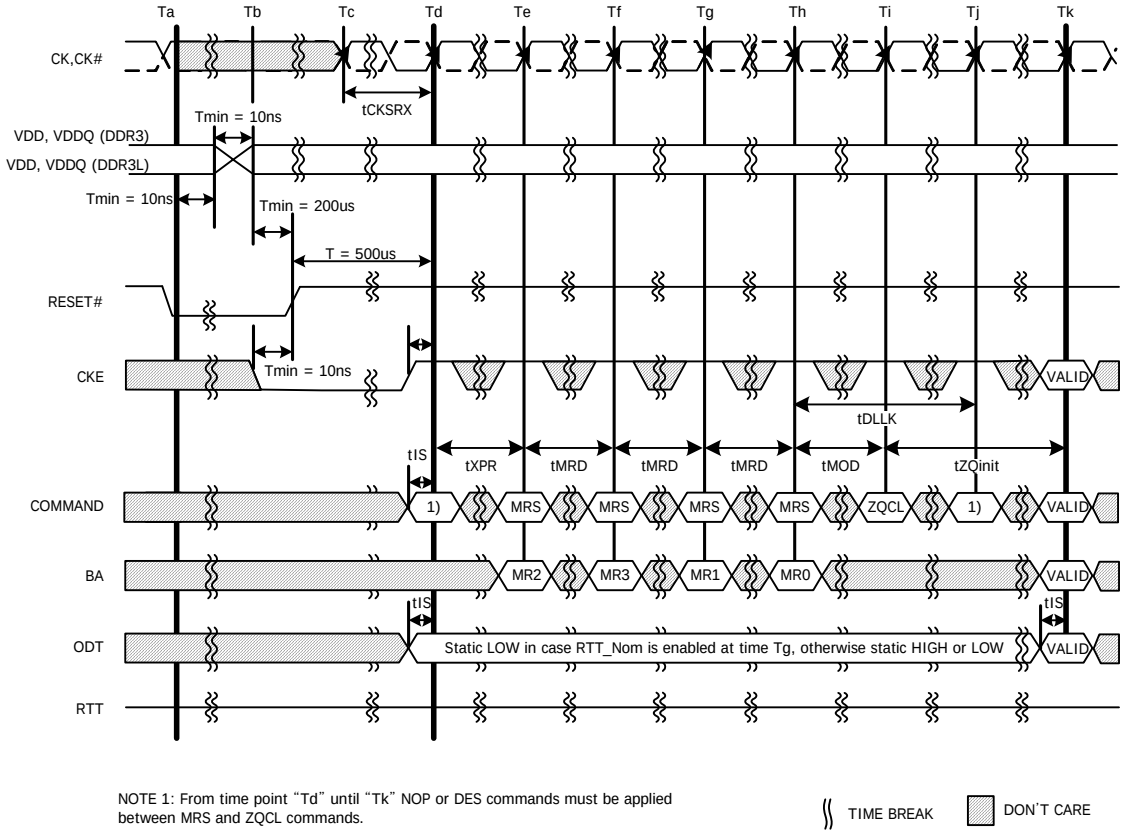


NOTE 1: From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK DON'T CARE

Figure 0 - VDD/VDDQ Voltage Switch Between DDR3L and DDR3

AC & DC Input Measurement Levels

AC and DC Logic Input Levels for Single-Ended Signals

AC and DC Input Levels for Single-Ended Command and Address Signals

Single Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		DDR3L-1866		Unit	Notes
		Min	Max	Min	Max	Min	Max		
VIH.CA(DC90)	DC input logic high	Vref + 0.09	VDD	Vref + 0.09	VDD	Vref + 0.09	VDD	V	1
VIL.CA(DC90)	DC input logic low	VSS	Vref - 0.09	VSS	Vref - 0.09	VSS	Vref - 0.09	V	1
VIH.CA(AC160)	AC input logic high	Vref + 0.160	Note2	Vref + 0.160	Note2	-	-	V	1,2,5
VIL.CA(AC160)	AC input logic low	Note2	Vref - 0.160	Note2	Vref - 0.160	-	-	V	1,2,5
VIH.CA(AC135)	AC Input logic high	Vref + 0.135	Note2	Vref + 0.135	Note2	Vref + 0.135	Note2	V	1,2,5
VIL.CA(AC135)	AC input logic low	Note2	Vref - 0.135	Note2	Vref - 0.135	Note2	Vref - 0.135	V	1,2,5
VIH.CA(AC125)	AC Input logic high	-	-	-	-	Vref + 0.125	Note2	V	1,2,5
VIL.CA(AC125)	AC input logic low	-	-	-	-	Note2	Vref - 0.125	V	1,2,5
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3,4

Notes:

1. For input only pins except $\overline{\text{RESET}}$, Vref = VrefCA (DC).
2. Refer to "Overshoot and Undershoot Specifications" on page 28.
3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefCA(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 13.5 mV).
4. For reference: approx. VDD/2 +/- 13.5 mV
5. These levels apply for 1.35 volt (see table above) operation only. If the device is operated at 1.5V (table "Single Ended AC and DC Input Levels for DQ and DM" on page 16), the respective levels in JESD79-3 (VIH/L.CA(DC100), VIH/L.CA(AC175), VIH/L.CA(AC150), VIH/L.CA(AC135), VIH/L.CA(AC125) etc.) apply. The 1.5V levels (VIH/L.CA(DC100), VIH/L.CA(AC175), VIH/L.CA(AC150), VIH/L.CA(AC135), VIH/L.CA(AC125) etc.) do not apply when the device is operated in the 1.35 voltage range.

AC and DC Input Levels for Single-Ended Signals

DDR3 SDRAM will support two Vih/Vil AC levels for DDR3-800 and DDR3-1066s specified in table below. DDR3 SDRAM will also support corresponding tDS values (Table 43 and Table 50 in “DDR3L Device Operation”) as well as derating tables Table 46 in “DDR3L Device Operation” depending on Vih/Vil AC levels.

Single Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		DDR3L-1866		Unit	Notes
		Min	Max	Min	Max	Min	Max		
VIH.DQ(DC90)	DC input logic high	Vref + 0.09	VDD	Vref + 0.09	VDD	Vref + 0.09	VDD	V	1
VIL.DQ(DC90)	DC input logic low	VSS	Vref - 0.09	VSS	Vref - 0.09	VSS	Vref - 0.09	V	1
VIH.DQ(AC160)	AC input logic high	Vref + 0.160	Note2	-	-	-	-	V	1, 2, 5
VIL.DQ(AC160)	AC input logic low	Note2	Vref - 0.160	-	-	-	-	V	1, 2, 5
VIH.DQ(AC135)	AC Input logic high	Vref + 0.135	Note2	Vref + 0.135	Note2	-	-	V	1, 2, 5
VIL.DQ(AC135)	AC input logic low	Note2	Vref - 0.135	Note2	Vref - 0.135	-	-	V	1, 2, 5
VIH.DQ(AC130)	AC Input logic high	-	-	-	-	Vref + 0.130	Note2	V	1, 2, 5
VIL.DQ(AC130)	AC input logic low	-	-	-	-	Note2	Vref - 0.130	V	1, 2, 5
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3, 4

Notes:

1. Vref = VrefDQ (DC).
2. Refer to "Overshoot and Undershoot Specifications" on page 28.
3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 13.5 mV). 4. For reference: approx. VDD/2 +/- 13.5 mV
4. For reference: approx. VDD/2 +/- 13.5 mV
5. These levels apply for 1.35 volt (table "Single Ended AC and DC Input Levels for Command and Address" on page 15) operation only. If the device is operated at 1.5V (table above), the respective levels in JESD79-3 (VIH/L.DQ(DC100), VIH/L.DQ(AC175), VIH/L.DQ(AC150), VIH/L.DQ(AC135) etc.) apply. The 1.5V levels (VIH/L.DQ(DC100), VIH/L.DQ(AC175), VIH/L.DQ(AC150), VIH/L.DQ(AC135) etc.) do not apply when the device is operated in the 1.35 voltage range.

Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages $_{VRefCA}$ and V_{RefDQ} are illustrated in figure below. It shows a valid reference voltage V_{Ref} (t) as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise).

V_{Ref} (DC) is the linear average of V_{Ref} (t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in the table "Differential AC and DC Input Levels" on page 19. Furthermore V_{Ref} (t) may temporarily deviate from $V_{Ref\ (DC)}$ by no more than +/- 1% VDD.

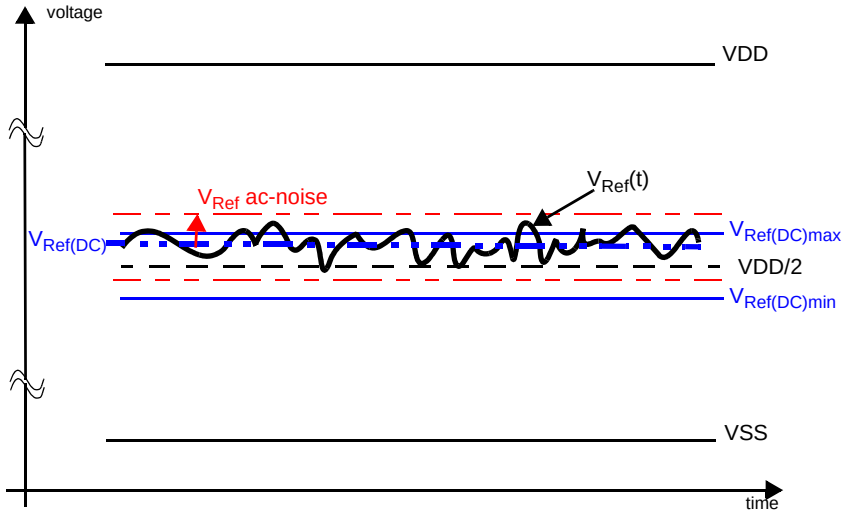


Illustration of $V_{Ref(DC)}$ tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$, and $V_{IL(DC)}$ are dependent on V_{Ref}.

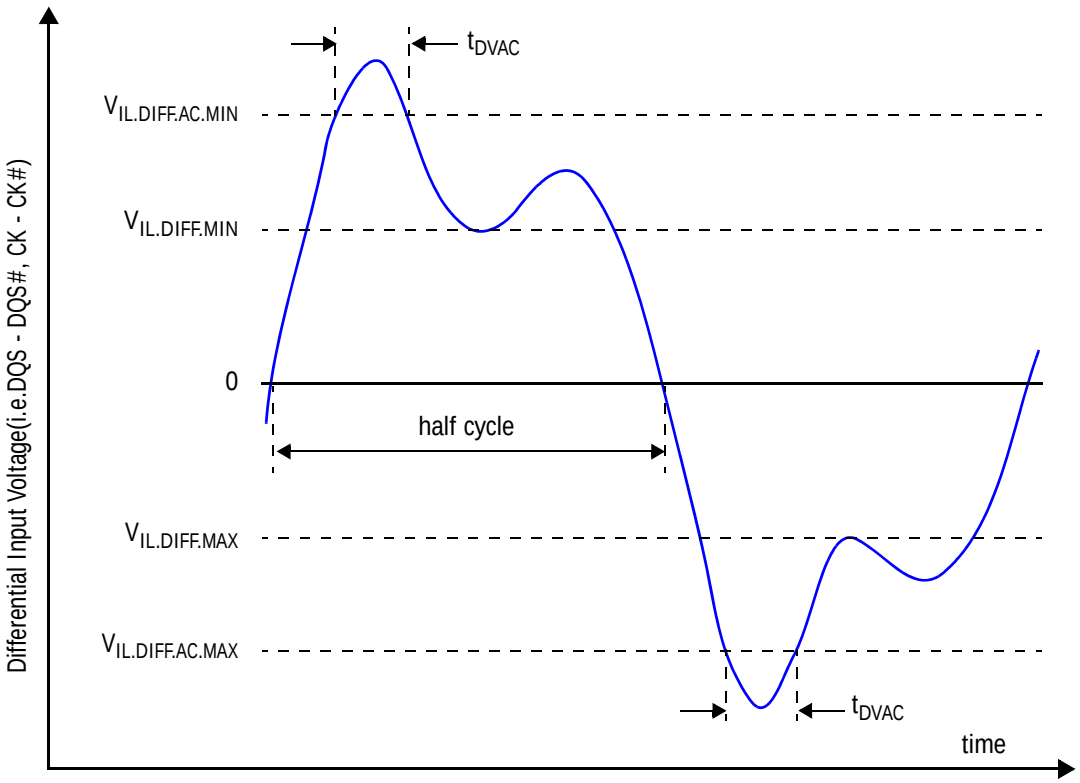
"V_{Ref}" shall be understood as $V_{Ref(DC)}$, as defined in figure above.

This clarifies that dc-variations of V_{Ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{Ref(DC)}$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{Ref}ac-noise. Timing and voltage effects due to ac-noise on V_{Ref} up to the specified limit (+/- 1% of VDD) are included in DRAM timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals

Differential signal definition



Definition of differential ac-swing and "time above ac-level" t_{DVAC}

Differential swing requirements for clock (CK - $\overline{CK}$) and strobe (DQS-$\overline{DQS}$)

Differential AC and DC Input Levels

Symbol	Parameter	DDR3L-800, 1066, 1333, 1600		Unit	Notes
		Min	Max		
VIHdiff	Differential input high	+ 0.180	Note 3	V	1
VILdiff	Differential input logic low	Note 3	- 0.180	V	1
VIHdiff (ac)	Differential input high ac	2 x (VIH (ac) - Vref)	Note 3	V	2
VILdiff (ac)	Differential input low ac	Note 3	2 x (VIL (ac) - Vref)	V	2

Notes:

1. Used to define a differential signal slew-rate.
2. For CK - $\overline{CK}$ use VIH/VIL (ac) of AADD/CMD and VREFCA; for DQS - $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ use VIH/VIL (ac) of DQs and VREFDQ; if a reduced ac-high or ac-low levels is used for a signal group, then the reduced level applies also here.
3. These values are not defined; however, the single-ended signals Ck, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits (VIH (dc) max, VIL (dc) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 28.

Allowed time before ringback (tDVAC) for CK - $\overline{CK}$ and DQS - $\overline{DQS}$

Slew Rate [V/ns]	DDR3L-800/1066/1333/1600				DDR3L-1866					
	tDVAC [ps] @ |VIH/Ldiff (ac)| = 320mV		tDVAC [ps] @ |VIH/Ldiff (ac)| = 270mV		tDVAC [ps] @ |VIH/Ldiff (ac)| = 270mV		tDVAC [ps] @ |VIH/Ldiff (ac)| = 250mV		tDVAC [ps] @ |VIH/Ldiff (ac)| = 260mV	
	min	max	min	max	min	max	min	max	min	max
> 4.0	189	-	201	-	163	-	168	-	176	-
4.0	189	-	201	-	163	-	168	-	176	-
3.0	162	-	179	-	140	-	147	-	154	-
2.0	109	-	134		95		105		111	
1.8	91	-	119	-	80	-	91	-	97	-
1.6	69	-	100	-	62	-	74	-	78	-
1.4	40	-	76	-	37	-	52	-	56	-
1.2	note	-	44	-	5	-	22	-	24	-
1.0	note	-	note	-	note	-	note	-	note	-
< 1.0	note	-	note	-	note	-	note	-	note	-

note : Rising input signal shall become equal to or greater than VIH(ac) level and Falling input signal shall become equal to or less than VIL(ac) level.

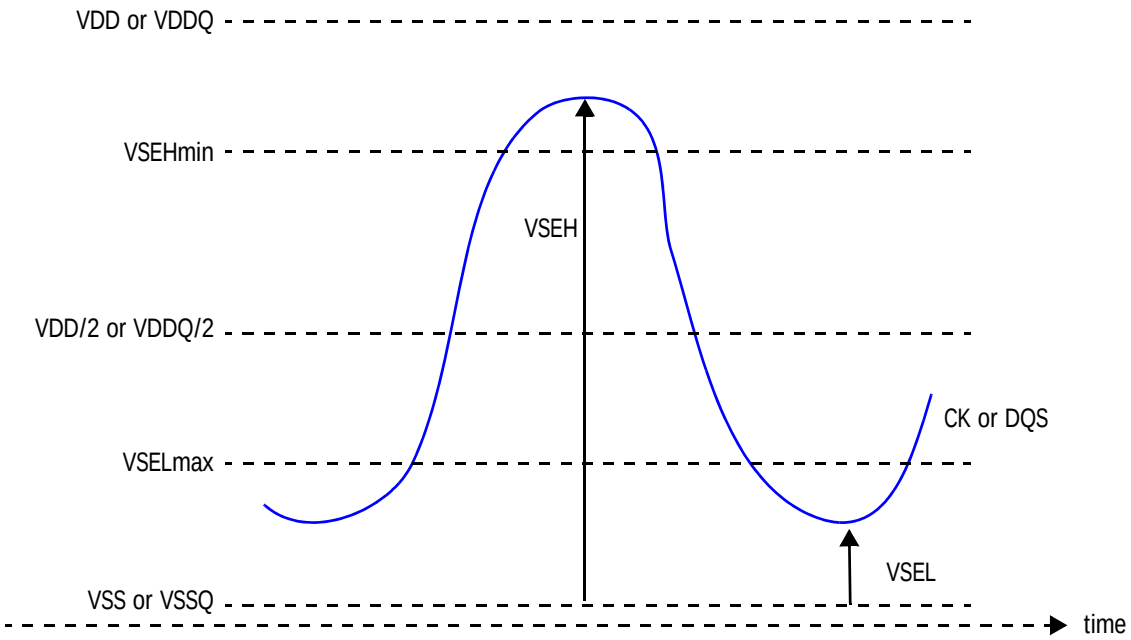
Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$, of $\overline{DQSU}$) also has to comply with certain requirements for single-ended signals.

CK and CK have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH (ac) / VIL (ac)) for ADD/CMD signals) in every half-cycle.

DQS, DQSL, DQSU, $\overline{DQS}$, $\overline{DQSL}$ have to reach VSEHmin / VSELmax (approximately the ac-levels (VIH (ac) / VIL (ac)) for DQ signals) in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g., if VIH.CA(AC150)/VIL.CA(AC150) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and $\overline{CK}$.



Single-ended requirements for differential signals.

Note that, while ADD/CMD and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. the transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended levels for CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$ or $\overline{DQSU}$

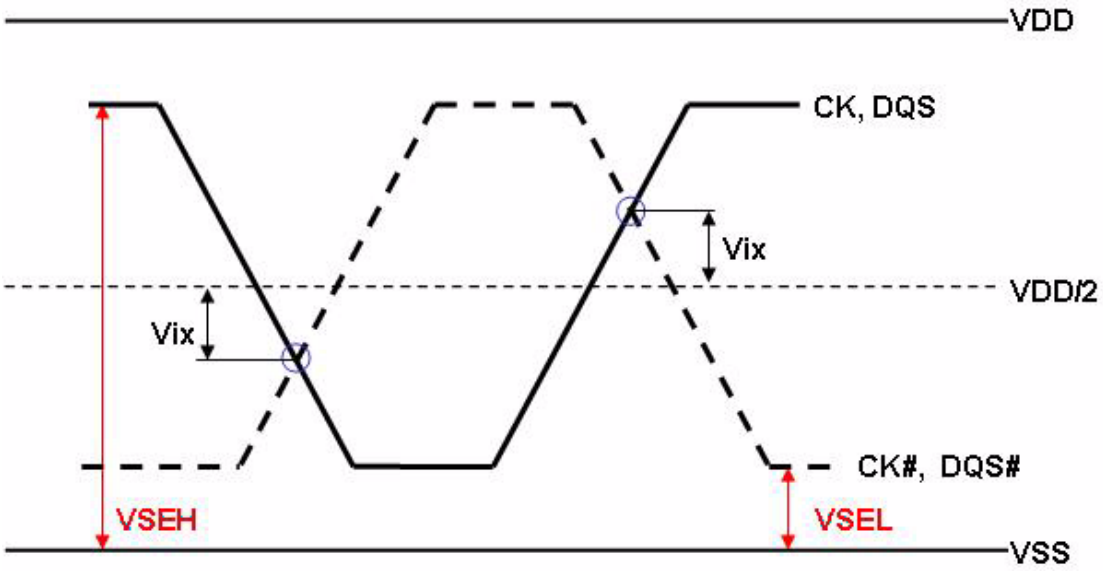
Symbol	Parameter	DDR3L-800, 1066, 1333, 1600, 1866		Unit	Notes
		Min	Max		
VSEH	Single-ended high level for strobes	(VDD / 2) + 0.175	Note 3	V	1,2
	Single-ended high level for Ck, $\overline{CK}$	(VDD /2) + 0.175	Note 3	V	1,2
VSEL	Single-ended low level for strobes	Note 3	(VDD / 2) - 0.175	V	1,2
	Single-ended low level for CK, $\overline{CK}$	Note 3	(VDD / 2) - 0.175	V	1,2

Notes:

1. For CK, $\overline{CK}$ use VIH/VIL (ac) of ADD/CMD; for strobes (DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$) use VIH/VIL (ac) of DQs.
2. VIH (ac)/VIL (ac) for DQs is based on VREFDQ; VIH (ac)/VIL (ac) for ADD/CMD is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined; however, the single-ended signals Ck, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits (VIH (dc) max, VIL (dc) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 28.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in table below. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS



Vix Definition

Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	DDR3L-800, 1066, 1333, 1600, 1866		Unit	Notes
		Min	Max		
V_{IX}(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK, $\overline{CK}$	-150	150	mV	2
		-175	175	mV	1
V_{IX}(DQS)	Differential Input Cross Point Voltage relative to VDD/2 for DQS, $\overline{DQS}$	-150	150	mV	2

Notes:

1. Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-250 mV, and when the differential slew rate of CK - $\overline{CK}$ is larger than 3 V/ns.
2. The relation between Vix Min/Max and VSEL/VSEH should satisfy following.
   (VDD/2) + Vix (Min) - VSEL $\geq$ 25mV
   VSEH - ((VDD/2) + Vix (Max)) $\geq$ 25mV

Slew Rate Definitions for Single-Ended Input Signals

See 7.5 “Address / Command Setup, Hold and Derating” in “DDR3L Device Operation” for single-ended slew rate definitions for address and command signals.

See 7.6 “Data Setup, Hold and Slew Rate Derating” in “DDR3L Device Operation” for single-ended slew rate definition for data signals.

Slew Rate Definitions for Differential Input Signals

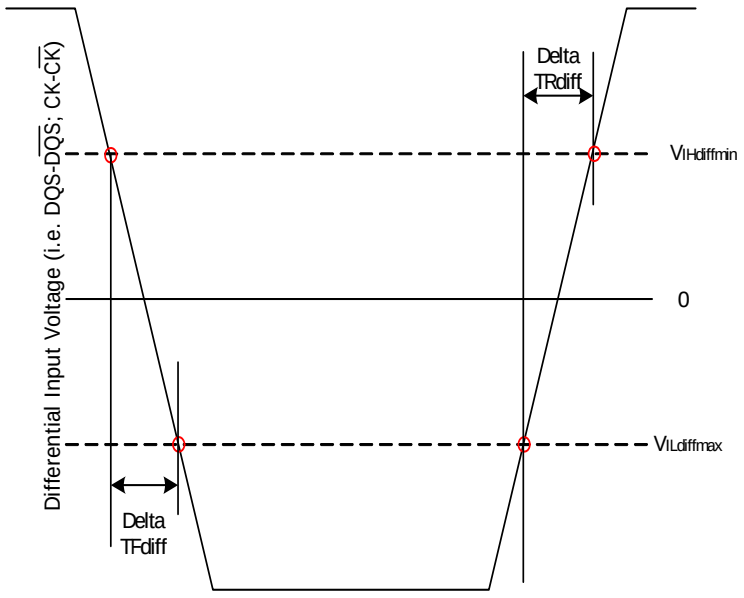
Input slew rate for differential signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) are defined and measured as shown in table and figure below.

Differential Input Slew Rate Definition

Description	Measured		Defined by
	Min	Max	
Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin}-V_{ILdiffmax}]$ / DeltaTRdiff
Differential input slew rate for falling edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin}-V_{ILdiffmax}]$ / DeltaTFdiff

Notes:

The differential signal (i.e. CK-$\overline{CK}$ and DQS-$\overline{DQS}$) must be linear between these thresholds.



Differential Input Slew Rate Definition for DQS, $\overline{DQS}$ and CK, $\overline{CK}$

AC & DC Output Measurement Levels

Single Ended AC and DC Output Levels

Table below shows the output levels used for measurements of single ended signals.

Single-ended AC and DC Output Levels

Symbol	Parameter	DDR3L-800, 1066, 1333, 1600, 1866	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	V_{TT} + 0.1 x V_{DDQ}	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	V_{TT} - 0.1 x V_{DDQ}	V	1

Notes:

1. The swing of ± 0.1 x V_{DDQ} is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT} = V_{DDQ} / 2.

Differential AC and DC Output Levels

Table below shows the output levels used for measurements of single ended signals.

Differential AC and DC Output Levels

Symbol	Parameter	DDR3L-800, 1066, 1333, 1600, 1866	Unit	Notes
$V_{OHdiff\ (AC)}$	AC differential output high measurement level (for output SR)	+ 0.2 x V_{DDQ}	V	1
$V_{OLdiff\ (AC)}$	AC differential output low measurement level (for output SR)	- 0.2 x V_{DDQ}	V	1

Notes:

1. The swing of ± 0.2 x V_{DDQ} is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

Single Ended Output Slew Rate

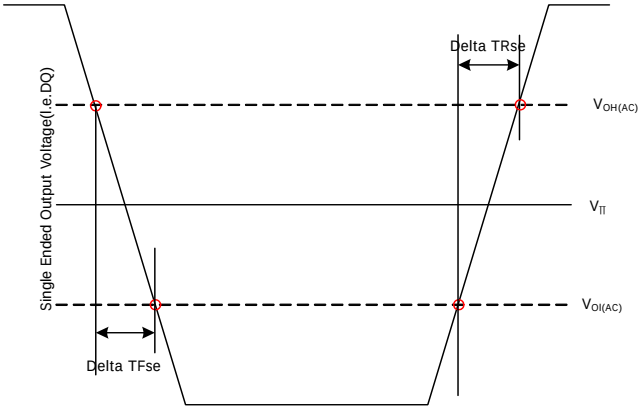
When the Reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals are shown in table and Figure below.

Single-ended Output slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	[$V_{OH(AC)}$-$V_{OL(AC)}$] / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	[$V_{OH(AC)}$-$V_{OL(AC)}$] / DeltaTFse

Notes:

1. Output slew rate is verified by design and characterisation, and may not be subject to production test.



Single Ended Output slew Rate Definition

Output Slew Rate (single-ended)

		DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	1.75	5[1)]	1.75	5[1)]	1.75	5[1)]	1.75	5[1)]	1.75	5[1)]	V/ns

Description: SR; Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

Note 1): In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.

Case 1 is a defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

Case 2 is a defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane switching into the opposite direction (i.e. from low to high of high to low respectively). For the remaining DQ signal switching in to the opposite direction, the regular maximum limite of 5 V/ns applies.

Differential Output Slew Rate

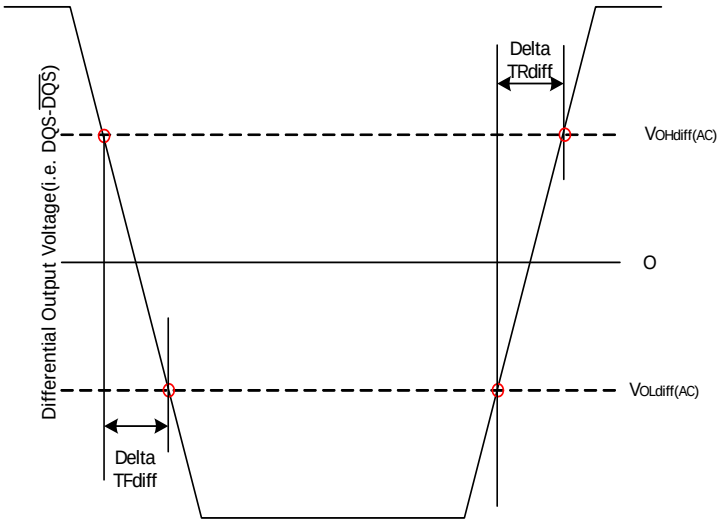
With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff (AC) and VOHdiff (AC) for differential signals as shown in table and figure below.

Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff\ (AC)}$	$V_{OHdiff\ (AC)}$	$[V_{OHdiff\ (AC)}-V_{OLdiff\ (AC)}]$ / DeltaTRdiff
Differential output slew rate for falling edge	$V_{OHdiff\ (AC)}$	$V_{OLdiff\ (AC)}$	$[V_{OHdiff\ (AC)}-V_{OLdiff\ (AC)}]$ / DeltaTFdiff

Notes:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.



Differential Output slew Rate Definition

Differential Output Slew Rate

Parameter	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	3.5	12	3.5	12	3.5	12	3.5	12	3.5	12	V/ns

Description: SR; Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

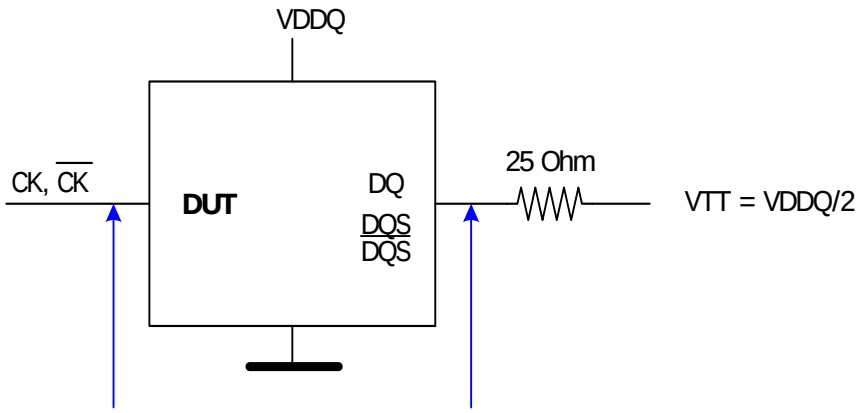
se: Single-ended Signals

For Ron = RZQ/7 setting

Reference Load for AC Timing and Output Slew Rate

Figure Below represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



Reference Load for AC Timing and Output Slew Rate

Overshoot and Undershoot Specifications

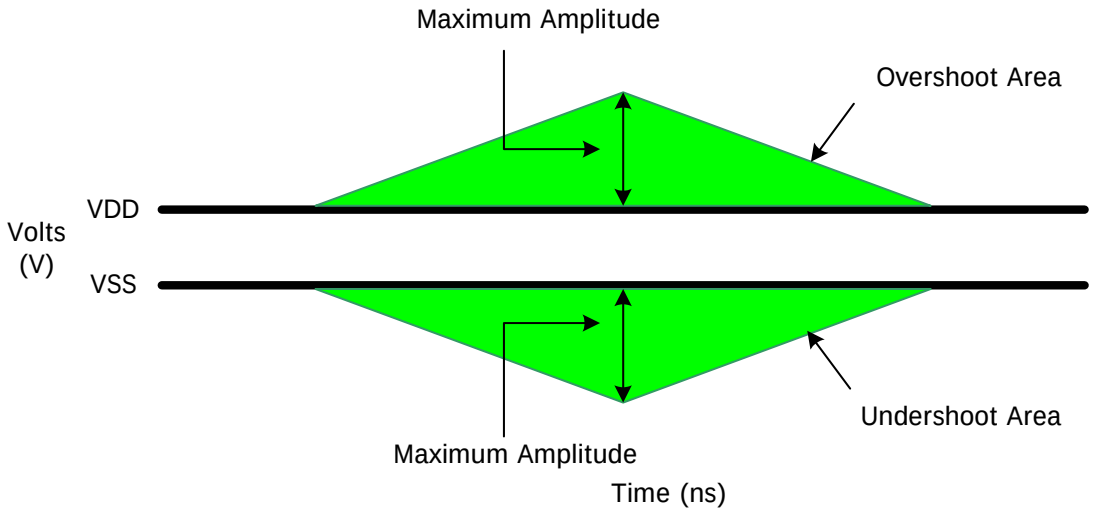
Address and Control Overshoot and Undershoot Specifications

AC Overshoot/Undershoot Specification for Address and Control Pins

Parameter	DDR3 L-800	DDR3 L-1066	DDR3 L-1333	DDR3 L-1600	DDR3 L-1866	Units
Maximum peak amplitude allowed for overshoot area. (See Figure below)	0.4	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area. (See Figure below)	0.4	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDD (See Figure below)	0.67	0.5	0.4	0.33	0.28	V-ns
Maximum undershoot area below VSS (See Figure below)	0.67	0.5	0.4	0.33	0.28	V-ns

(A0-A15, BA0-BA3, CS, RAS, CAS, WE, CKE, ODT)

See figure below for each parameter definition



Address and Control Overshoot and Undershoot Definition

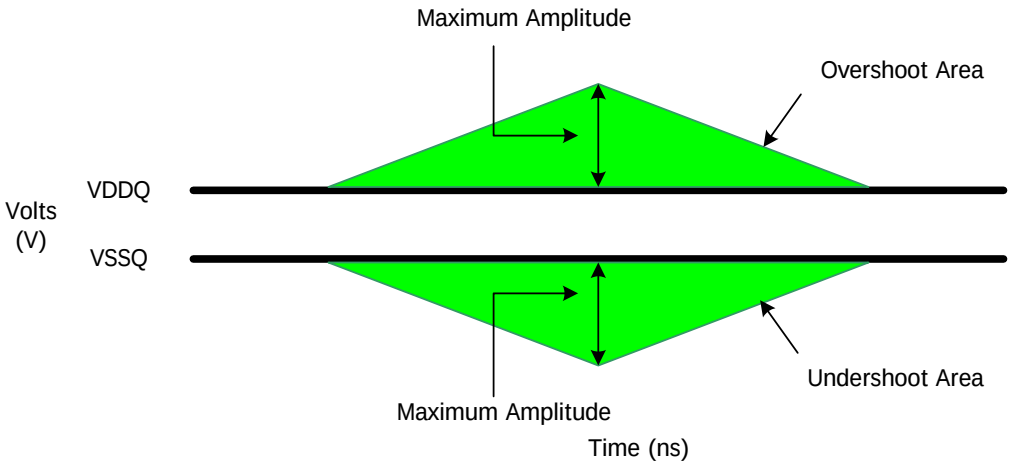
Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask

Parameter	DDR3 L-800	DDR3 L-1066	DDR3 L-1333	DDR3 L-1600	DDR3 L-1866	Units
Maximum peak amplitude allowed for overshoot area. (See Figure below)	0.4	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area. (See Figure below)	0.4	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDD (See Figure below)	0.25	0.19	0.15	0.13	0.11	V-ns
Maximum undershoot area below VSS (See Figure below)	0.25	0.19	0.15	0.13	0.11	V-ns

(CK, $\overline{CK}$, DQ, DQS, $\overline{DQS}$, DM)

See figure below for each parameter definition



Clock, Data, Strobe and Mask Overshoot and Undershoot Definition

Refresh parameters by device density

Refresh parameters by device density

Parameter	RTT_Nom Setting		512Mb	1Gb	2Gb	4Gb	8Gb	Units	Notes
REF command ACT or REF command time	tRFC		90	110	160	260	350	ns	
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85 °C	7.8	7.8	7.8	7.8	7.8	us	
		85 °C < T_{CASE} ≤ 95 °C	3.9	3.9	3.9	3.9	3.9	us	

Notes:

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this materia.

Standard Speed Bins

DDR3L SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

DDR3L-800 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 36.

Speed Bin			DDR3L-800E		Unit	Notes
CL - nRCD - nRP			6-6-6			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	15	—	ns	
PRE command period		t_{RP}	15	—	ns	
ACT to ACT or REF command period		t_{RC}	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	ns	
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3
Supported CL Settings			6		n_{CK}	
Supported CWL Settings			5		n_{CK}	

DDR3L-1066 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 36.

Speed Bin			DDR3L-1066F		Unit	Note
CL - nRCD - nRP			7-7-7			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.125	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.125	—	ns	
PRE command period		t_{RP}	13.125	—	ns	
ACT to ACT or REF command period		t_{RC}	50.625	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	ns	
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,6
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3
Supported CL Settings			6, 7, 8		n_{CK}	
Supported CWL Settings			5, 6		n_{CK}	

DDR3L-1333 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 36.

Speed Bin			DDR3L-1333H		Unit	Note
CL - nRCD - nRP			9-9-9			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.5 (13.125)[5,10]	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.5 (13.125)[5,10]	—	ns	
PRE command period		t_{RP}	13.5 (13.125)[5,10]	—	ns	
ACT to ACT or REF command period		t_{RC}	49.5 (49.125)[5,10]	—	ns	
ACT to PRE command period		t_{RAS}	36	9 * tREFI	ns	
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,7
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4,7
			(Optional)[5,10]			
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3
			(Optional)		ns	5
Supported CL Settings			6, 7, 8, 9, 10		n_{CK}	
Supported CWL Settings			5, 6, 7		n_{CK}	

DDR3L-1600 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 36.

Speed Bin			DDR3L-1600K		Unit	Note
CL - nRCD - nRP			11-11-11			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.75 (13.125)[5,10]	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.75 (13.125)[5,10]	—	ns	
PRE command period		t_{RP}	13.75 (13.125)[5,10]	—	ns	
ACT to ACT or REF command period		t_{RC}	48.75 (48.125)[5,10]	—	ns	
ACT to PRE command period		t_{RAS}	35	9 * tREFI	ns	
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,8
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4,8
			(Optional)[5,10]			
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,4,8
			(Optional)[5,10]			
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 11	CWL = 5, 6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	<1.5	ns	1,2,3
Supported CL Settings			5, 6, 7, 8, 9, 10, 11		n_{CK}	
Supported CWL Settings			5, 6, 7, 8		n_{CK}	

DDR3L-1866 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 36.

Speed Bin			DDR3L-1866M		Unit	Note
CL - nRCD - nRP			13-13-13			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.91 (13.125)[5,11]	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.91 (13.125)[5,11]	—	ns	
PRE command period		t_{RP}	13.91 (13.125)[5,11]	—	ns	
ACT to PRE command period		t_{RAS}	34	9 * tREFI	ns	
ACT to ACT or PRE command period		t_{RC}	47.91 (47.125)[5,11]	-	ns	
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,9
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,9
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4,9
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,9
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,9
	CWL = 8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,4,9
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,9
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,9
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,9
CL = 11	CWL = 5,6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	<1.5	ns	1,2,3,4,9
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 12	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 13	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	1.07	<1.25	ns	1, 2, 3
Supported CL Settings			6, 7, 8, 9, 10, 11, 13		n_{CK}	
Supported CWL Settings			5, 6, 7, 8, 9		n_{CK}	

Speed Bin Table Notes

Absolute Specification (T_{OPER}; V_{DDQ} = V_{DD} = 1.35V +0.100/- 0.067 V);

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to DIMM data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. DDR3 SDRAM devices supporting optional down binning to CL=7 and CL=9, and tAA/tRCD/tRP must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333H devices supporting down binning to DDR3-1066F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600K devices supporting down binning to DDR3-1333H or DDR3-1600F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 49.125ns (tRASmin + tRPmin = 36 ns + 13.125 ns) for DDR3-1333H and 48.125ns (tRASmin + tRPmin = 35 ns + 13.125 ns) for DDR3-1600K.
11. DDR3 SDRAM devices supporting optional down binning to CL=11, CL=9 and CL=7, tAA/tRCD/tRPmin must be 13.125ns. SPD setting must be programed to match. For example, DDR3-1866 devices supporting down binning to DDR3-1600 or DDR3-1333 or 1066 should program 13.125ns in SPD bytes for tAAmin(byte 16), tRCDmin(byte 18) and tRPmin(byte 20) is programmed to 13.125ns, tRCmin(byte 21,23) also should be programmed accordingly. For example, 47.125ns (tRASmin + tRPmin = 34ns + 13.125ns)

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature (ambient)	0 to +55	^{o}C	3
H_{OPR}	Operating humidity (relative)	10 to 90	%	
T_{STG}	Storage temperature	-50 to +100	^{o}C	1
H_{STG}	Storage humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

Note:

1. Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Expousure to absolute maximum rating conditions for extended periods may affect reliablility.
2. Up to 9850 ft.
3. The designer must meet the case temperature specifications for individual module components.

IDD and IDDQ Specification Parameters and Test Conditions

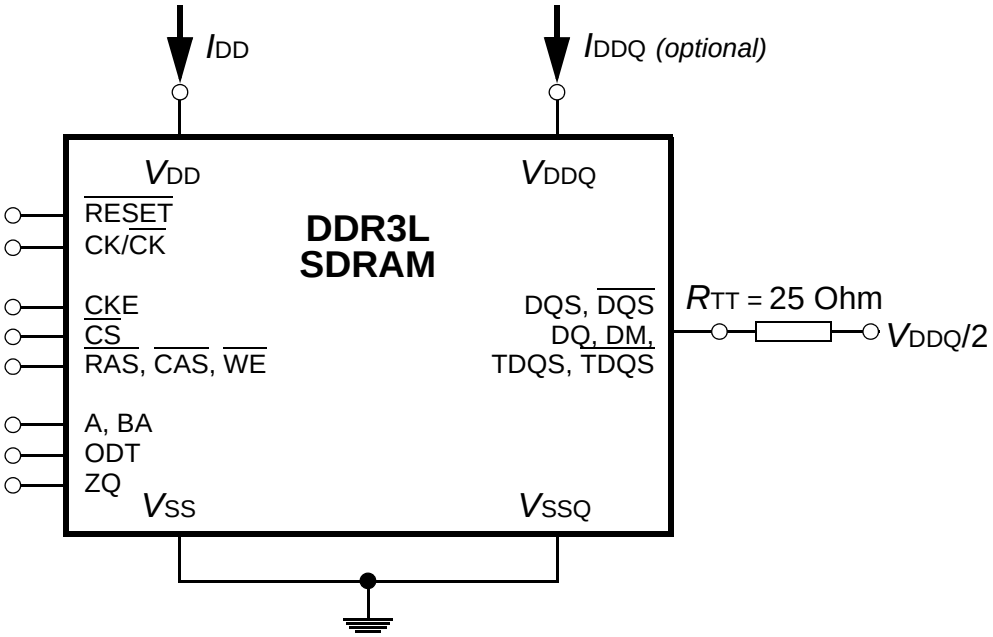
IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure below (Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements) shows the setup and test load for IDD and IDDQ measurements.

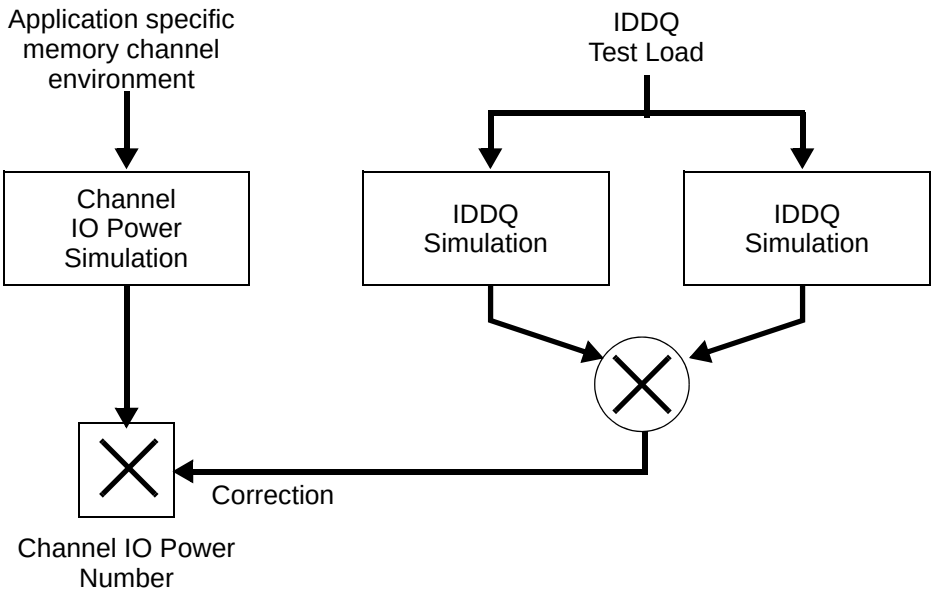
- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3L SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3L SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in the Figure below (Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement). In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using on merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- ”0” and “LOW” is defined as VIN <= $V_{ILAC(max)}$.
- ”1” and “HIGH” is defined as VIN >= $V_{IHAC(max)}$.
- “MID_LEVEL” is defined as inputs are VREF = VDD/2.
- Timing used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 1.
- Basic IDD and IDDQ Measurement Conditions are described in Table 2.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 3 through Table 10.
- IDD Measurements are done after properly initializing the DDR3L SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  Qoff = 0_B (Output Buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40 Ohm in MR1);
  RTT_Wr = RZQ/2 (120 Ohm in MR2);
  TDQS Feature disabled in MR1
- Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, LOW, LOW, LOW}
- Define $\overline{D}$ = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, HIGH, HIGH, HIGH}



Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements
[Note: DIMM level Output test load condition may be different from above



Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 1 -Timings used for IDD and IDDQ Measurement-Loop Patterns

Symbol		DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	Unit
		7-7-7	9-9-9	11-11-11	13-13-13	
t_{CK}		1.875	1.5	1.25	1.07	ns
CL		7	9	11	13	nCK
n_{RCD}		7	9	11	13	nCK
n_{RC}		27	33	39	45	nCK
n_{RAS}		20	24	28	32	nCK
n_{RP}		7	9	11	13	nCK
n_{FAW}	1KB page size	20	20	24	26	nCK
	2KB page size	27	30	32	33	nCK
n_{RRD}	1KB page size	4	4	5	5	nCK
	2KB page size	6	5	6	6	nCK
n_{RFC} -512Mb		48	60	72	85	nCK
n_{RFC}-1 Gb		59	74	88	103	nCK
n_{RFC}- 2 Gb		86	107	128	150	nCK
n_{RFC}- 4 Gb		139	174	208	243	nCK
n_{RFC}- 8 Gb		187	234	280	328	nCK

Table 2 -Basic IDD and IDDQ Measurement Conditions

Symbol	Description
I_{DD0}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 3; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 3.
I_{DD1}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address; Bank Address Inputs, Data IO: partially toggling according to Table 4; DM: stable at 0; Bank Activity: Cycling with on bank active at a time: 0,0,1,1,2,2,... (see Table 4); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 4.

Symbol	Description
I_{DD2N}	Precharge Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 5.
I_{DD2NT}	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 6; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: toggling according to Table 6; Pattern Details: see Table 6.
I_{DD2P0}	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit[c]
I_{DD2P1}	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit[c]
I_{DD2Q}	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0
I_{DD3N}	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 5.
I_{DD3P}	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0

Symbol	Description
I_{DD4R}	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 7; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...(see Table 7); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 7.
I_{DD4W}	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 8; Data IO: seamless read data burst with different data between one burst and the next one according to Table 8; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...(see Table 8); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at HIGH; Pattern Details: see Table 8.
I_{DD5B}	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 9; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: REF command every nREF (see Table 9); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 9.
I_{DD6}	Self-Refresh Current: Normal Temperature Range T_{CASE}: 0 - 85 °C; Auto Self-Refresh (ASR): Disabled[d)];Self-Refresh Temperature Range (SRT): Normal[e)]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: MID_LEVEL
I_{DD6ET}	Self-Refresh Current: Extended Temperature Range T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Disabled[d)];Self-Refresh Temperature Range (SRT): Extended[e)]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: MID_LEVEL

Symbol	Description
I_{DD7}	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, NRRD, nFAW, CL: see Table 1; BL: 8[a),f)]; AL: CL-1; $\overline{CS}$: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to Table 10; Data IO: read data burst with different data between one burst and the next one according to Table 10; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, wee Table 10; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 10.

a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B

c) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12 = 1B for Fast Exit

d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable

e) Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range

f) Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B

Table 3 - IDD0 Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1, 2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3, 4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 1*nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.

b) DQ signals are MID-LEVEL.

Table 4 - IDD1 Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until nRC + nRCE - 1, truncate if necessary												
			1*nRC+nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			...	repeat pattern nRC + 1,...4 until nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until *2 nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID_LEVEL.

Table 5 - IDD2N and IDD3N Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	8-11	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	12-15	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	16-19	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24-17	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
b) DQ signals are MID-LEVEL.

Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8-11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20-23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24-17	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
b) DQ signals are MID-LEVEL.

Table 7 - IDD4R and IDDQ4R Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 8 - IDD4W Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to WR Commands, otherwise MID-LEVEL.
b) Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 9 - IDD5B Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	-
		1	1.2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			5...8	repeat cycles 1...4, but BA[2:0] = 1												
			9...12	repeat cycles 1...4, but BA[2:0] = 2												
			13...16	repeat cycles 1...4, but BA[2:0] = 3												
			17...20	repeat cycles 1...4, but BA[2:0] = 4												
			21...24	repeat cycles 1...4, but BA[2:0] = 5												
			25...28	repeat cycles 1...4, but BA[2:0] = 6												
			29...32	repeat cycles 1...4, but BA[2:0] = 7												
		2	33...nRFC-1	repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary.												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
b) DQ signals are MID-LEVEL.

Table 10 - IDD7 Measurement-Loop Pattern[a)]

ATTENTION! Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD+1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD+2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2* nRRD - 1												
		2	2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4*nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
				Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW+nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
				Assert and repeat above D Command until 2* nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2&nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2* nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2&nFAW+nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
				Repeat above D Command until 2* nFAW + 2* nRRD - 1												
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 3												
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	3	00	0	0	0	0	-
				Assert and repeat above D Command until 3* nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 7												
		19	3*nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	0	0	-
				Assert and repeat above D Command until 4* nFAW - 1, if necessary												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

IDD Specifications (Tcase: 0 to 95°C)

* Module IDD values in the datasheet are only a calculation based on the component IDD spec.
The actual measurements may vary according to DQ loading cap.

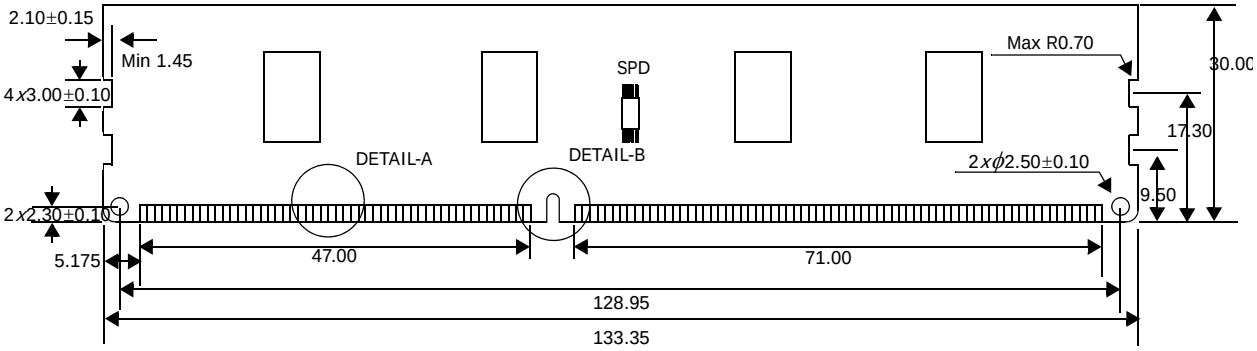
2GB, 256M x 64 U-DIMM: HMT425U6CFR6A

Symbol	DDR3L 1066	DDR3L 1333	DDR3L 1600	DDR3L 1866	Unit	note
IDD0	132	136	140	152	mA	
IDD1	168	172	176	188	mA	
IDD2N	52	56	60	68	mA	
IDD2NT	64	68	76	92	mA	
IDD2P0	40	40	40	44	mA	
IDD2P1	40	40	40	44	mA	
IDD2Q	52	52	56	64	mA	
IDD3N	112	120	124	136	mA	
IDD3P	84	88	88	92	mA	
IDD4R	368	428	500	568	mA	
IDD4W	380	440	488	568	mA	
IDD5B	520	520	520	540	mA	
IDD6	40	40	40	48	mA	
IDD6ET	52	52	52	80	mA	
IDD7	620	700	720	740	mA	

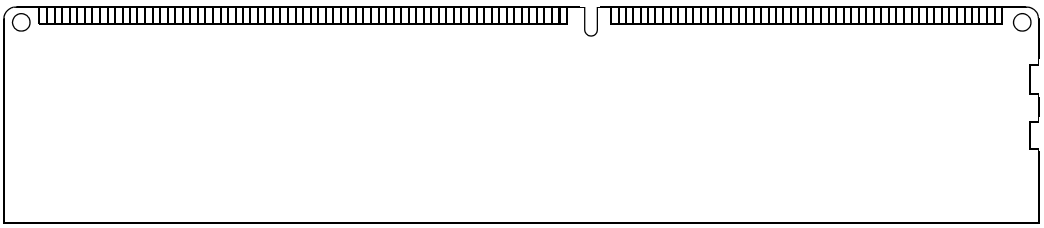
Module Dimensions

256Mx64 - HMT425U6CFR6A

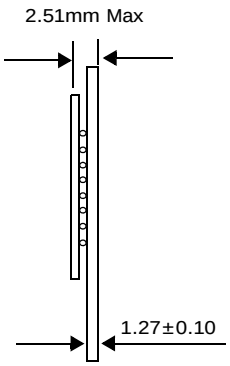
Front



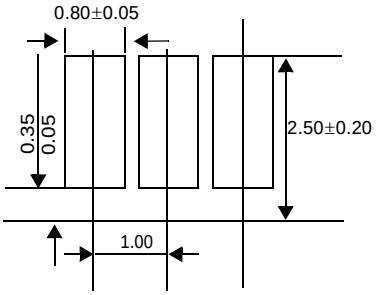
Back



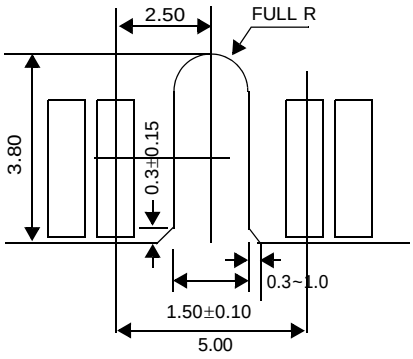
Side



Detail - A



Detail - B



Note:

1. ± 0.13 tolerance on all dimensions unless otherwise stated.

Units: millimeters