HMU16, HMU17

16 x 16-Bit CMOS Parallel Multipliers

FN2803
Rev 4.00
November 1999

The HMU16 and HMU17 are high speed, low power CMOS 16-bit x 16-bit multipliers ideal for fast, real time digital signal processing applications.

The X and Y operands along with their mode controls (TCX and TCY) have 17-bit input registers. The mode controls independently specify the operands as either two's complement or unsigned magnitude format, thereby allowing mixed mode multiplication operations.

Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP). For asynchronous output, these registers may be made transparent through the use of the Feedthrough Control (FT).

Additional inputs are provided for format adjustment and rounding. The Format Adjust control (FA) allows the user to select either a left shifted 31-bit product or a full 32-bit product, whereas the round control (RND) provides the capability of rounding the most significant portion of the result.

The HMU16 has independent clocks (CLKX, CLKY, CLKL, CLKM) associated with each of these registers to maximize throughput and simplify bus interfacing. The HMU17 has only a single clock input (CLK), but makes use of three register enables ($\overline{ENX}$, $\overline{ENY}$ and $\overline{ENP}$). The $\overline{ENX}$ and $\overline{ENY}$ inputs control the X and Y Input Registers, while $\overline{ENP}$ controls both the MSP and LSP Output Registers. This configuration facilitates the use of the HMU17 for microprogrammed systems.

The two halves of the product may be routed to a single 16-bit three-state output port via a multiplexer, and in addition, the LSP is connected to the Y-input port through a separate three-state buffer.

Features

- 16 x 16-Bit Parallel Multiplier with Full 32-Bit Product
- High-Speed (35ns) Clocked Multiply Time
- Low Power Operation
  - I_{CCSB} = 500µA Maximum
  - I_{CCOP} = 7.0mA Maximum at 1MHz
- Supports Two's Complement, Unsigned Magnitude and Mixed Mode Multiplication
- HMU16 is Compatible with the AM29516, LMU16, IDT7216 and the CY7C516
- HMU17 is Compatible with the AM29517, LMU17, IDT7217 and the CY7C517
- TTL Compatible Inputs/Outputs
- Three-State Outputs

Applications

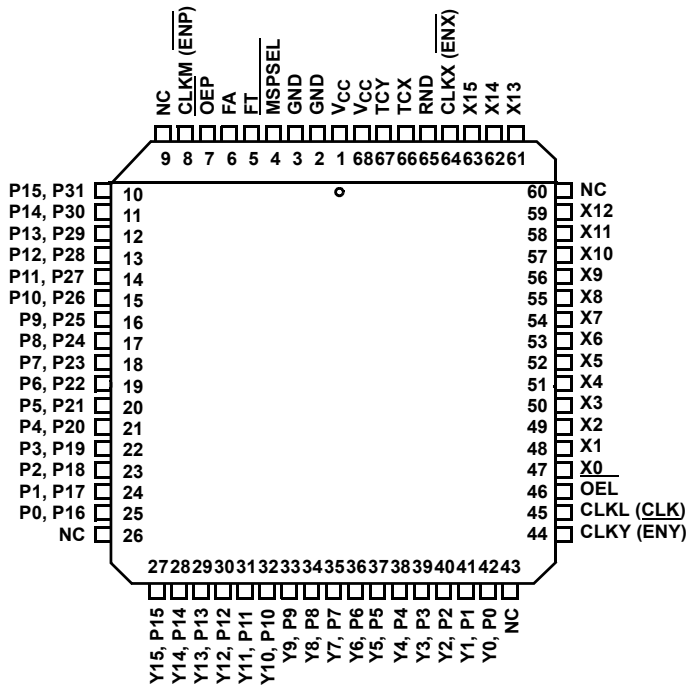
- Fast Fourier Transform Analysis
- Digital Filtering
- Graphic Display Systems
- Image Processing
- Radar and Sonar
- Speech Synthesis and Recognition

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HMU16JC-35	0 to 70	68 Ld PLCC	N68.95
HMU16JC-45	0 to 70	68 Ld PLCC	N68.95
HMU16GC-35	0 to 70	68 Ld CPGA	G68.B
HMU16GC-45	0 to 70	68 Ld CPGA	G68.B
HMU17JC-35	0 to 70	68 Ld PLCC	N68.95
HMU17JC-45	0 to 70	68 Ld PLCC	N68.95
HMU17GC-35	0 to 70	68 Ld CPGA	G68.B
HMU17GC-45	0 to 70	68 Ld CPGA	G68.B

Pinouts

68 LEAD PLCC
TOP VIEW

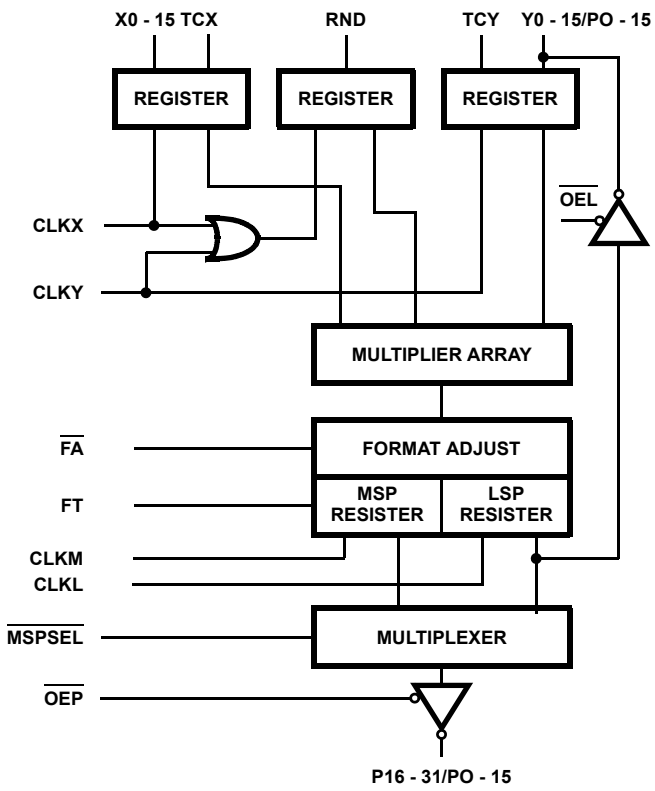


68 LEAD CPGA
TOP VIEW

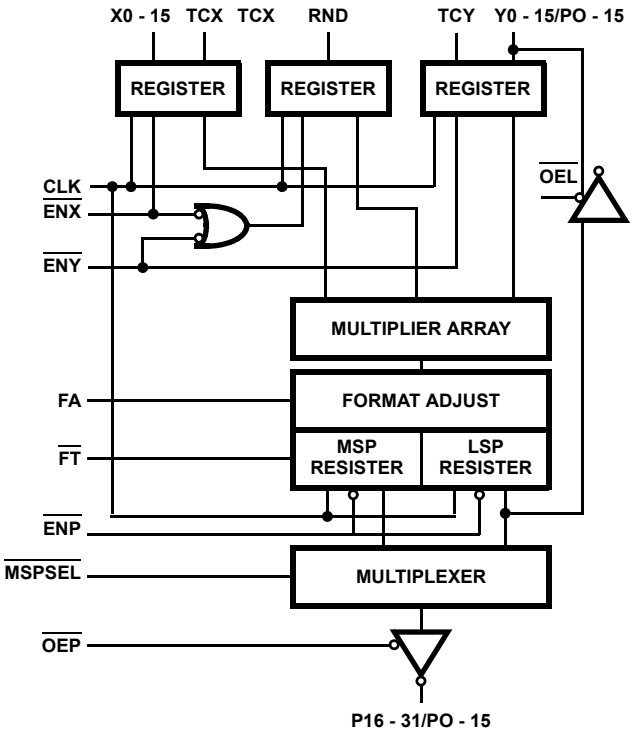
	A	B	C	D	E	F	G	H	J	K	L
11		N/C	X13	X15	RND	TCY	V_{CC}	GND	FT	$\overline{OEP}$	
10	X11	X12	X14	CLKX (ENX)	TCX	V_{CC}	GND	$\overline{MSP}$ SEL	$\overline{FA}$	CLKM (ENP)	N/C
9	X9	X10								P30/ P14	P31/ P15
8	X7	X8								P28/ P12	P29/ P13
7	X5	X6								P26/ P10	P27/ P11
6	X3	X4								P24/ P8	P25/ P9
5	X1	X2								P22/ P6	P23/ P7
4	$\overline{OEL}$	X0								P20/ P4	P21/ P5
3	CLKY (ENY)	CLKL (CLK)								P18/ P2	P19/ P3
2	N/C	Y0/P0	Y2/P2	Y4/P4	Y6/P6	Y8/P8	Y10/ P10	Y12/ P12	Y14/ P14	P16/ P0	P17/ P1
1		Y1/P1	Y3/P3	Y5/P5	Y7/P7	Y9/P9	Y11/ P11	Y13/ P13	Y15/ P15	N/C	

Functional Block Diagrams

HMU16



HMU17



Pin Description

SYMBOL	PLCC PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	1, 68		V_{CC}. The +5V power supply pins. A 0.1µF capacitor between the V_{CC} and GND pins is recommended.
GND	2, 3		GND. The device ground.
X0-X15	47-59, 61-63	I	X-Input Data. These 16 data inputs provide the multiplicand which may be in two's complement or unsigned magnitude format.
Y0-Y15/ P0-P15	27-42	I/O	Y-Input/LSP Output Data. This 16-bit port is used to provide the multiplier which may be in two's complement or unsigned magnitude format. It may also be used for output of the Least Significant Product (LSP).
P16-P31/ P0-P15	10-25	O	Output Data. This 16-bit port may provide either the MSP (P16-31) or the LSP (P0-15).
TCY, TCX	66, 67	I	Two's Complement Control. Input data is interpreted as two's complement when this control is HIGH. A LOW indicates the data is to be interpreted as unsigned magnitude format.
FT	5	I	Feed through Control. When this control is HIGH, both the MSP and LSP Registers are transparent. When LOW, the registers are latched by their associated clock signals.
$\overline{FA}$	6	I	Format Adjust Control. A full 32-bit product is selected when this control line is HIGH. A LOW on this control line selects a left shifted 31-bit product with the sign bit replicated in the LSP. This control is normally HIGH, except for certain two's complement integer and fractional applications.
RND	65	I	Round Control. When this control is HIGH, a one is added to the Most Significant Bit (MSB) of the LSP. This position is dependent on the $\overline{FA}$ control; $\overline{FA}$ = HIGH indicates RND adds to the 2-15 bit (P15), and $\overline{FA}$ = LOW indicates RND adds to the 2^{-16} bit (P14).
$\overline{MSPSEL}$	4	I	Output Multiplexer Control. When this control is LOW, the MSP is available for output at the dedicated output port, and the LSP is available at the Y-input/LSP output port. When $\overline{MSPSEL}$ is HIGH, the LSP is available at both ports and the MSP is not available for output.
$\overline{OEL}$	46	I	Y-In/P0-15 Output Port Three-State Control. When $\overline{OEL}$ is HIGH, the output drivers are in the high impedance state. This state is required for Ydata input. When $\overline{OEL}$ is LOW, the port is enabled for LSP output.
$\overline{OEP}$	7	I	P16-31/P0-15 Output Port Three-State Control. A LOW on this control line enables the output port. When $\overline{OEP}$ is HIGH, the output drivers are in the high impedance state.
THE FOLLOWING PIN DESCRIPTIONS APPLY TO THE HMU16 ONLY			
CLKX	64	I	X-Register Clock. The rising edge of this clock loads the X-data Input Register along with the TCX and RND Registers.
CLKY	44	I	Y-Register Clock. The rising edge of this clock loads the Y-data Input Register along with the TCY and RND Registers.
CLKM	8	I	MSP Register Clock. The rising edge of CLKM loads the Most Significant Product (MSP) Register.
CLKL	45	I	LSP Register Clock. The rising edge of CLKL loads the Least Significant Product (LSP) Register.
THE FOLLOWING PIN DESCRIPTIONS APPLY TO THE HMU17 ONLY			
CLK	45	I	Clock. The rising edge of this clock will load all enabled registers.
$\overline{ENX}$	64	I	X-Register Enable. When $\overline{ENX}$ is LOW, the X-register is enabled; X-input data and TCX will be latched at the rising edge of CLK. When $\overline{ENX}$ is high, the X-register is in a hold mode.
$\overline{ENY}$	44	I	Y-Register Enable. $\overline{ENY}$ enables the Y-register. (See $\overline{ENX}$).
$\overline{ENP}$	8	I	Product Register Enable. $\overline{ENP}$ enables the Product Register. Both the MSP and LSP Sections are enabled by $\overline{ENP}$. (See $\overline{ENX}$).

Functional Description

The HMU16/HMU17 are high speed 16 x 16-bit multipliers designed to perform very fast multiplication of two 16-bit binary numbers. The two 16-bit operands (X and Y) may be independently specified as either two's complement or unsigned magnitude format by the two's complement controls (TCX and TCY). When either of these control lines is LOW, the respective operand is treated as an unsigned 16-bit value; and when it is HIGH, the operand is treated as a signed value represented in two's complement format. The operands along with their respective controls are latched at the rising edge of the associated clock signal. The HMU16 accomplishes this through the use of independent clock inputs for each of the Input Registers (CLKX and CLKY), while the HMU17 utilizes a single clock signal (CLK) along with the X and Y register enable inputs ($\overline{ENX}$ and $\overline{ENY}$).

Input controls are also provided for rounding and format adjustment of the 32-bit product. The Round input (RND) is provided to accommodate rounding of the most significant portion of the product by adding one to the Most Significant Bit (MSB) of the LSP Register. The position of the MSB is dependent on the state of the Format Adjust Control (see Pin Descriptions and Multiplier Input/Output Format Tables). The Round input is latched into the RND Register whenever either of the input registers is clocked. The Format Adjust control ($\overline{FA}$) allows the product output to be formatted. When the $\overline{FA}$ control is HIGH, a full 32-bit product is output; and when $\overline{FA}$ is LOW, a left-shifted 31-bit product is output with the sign bit replicated in bit position 15 of the LSP. The $\overline{FA}$ control must be HIGH for unsigned magnitude, and mixed mode multiplication operations. It may be LOW for certain two's complement integer and fractional operations only (see Multiplier Input/ Output Formats Table).

The HMU16/HMU17 multipliers are equipped with two 16-bit Output Registers (MSP and LSP) which are provided to hold the most and least significant portions of the resultant product respectively. The HMU16 uses independent clocks (CLKM and CLKL) for latching the two output registers, while the HMU17 uses a single clock input (CLK) along with the Product Latch Enable ($\overline{ENP}$). The MSP and LSP Registers may also be made transparent for asynchronous output through the use of the Feed through Control (FT). There are two output configurations which may be selected when using the HMU16/HMU17 multipliers. The first configuration allows the simultaneous access of the most and least significant halves of the product. When the $\overline{MSPSEL}$ input is LOW, the Most Significant Product will be available at the dedicated output port (P16-31/P0-15). The Least Significant Product is simultaneously available at the bidirectional port shared with the Y-inputs (Y0-15/P0-15) through the use of the LSP output enable ($\overline{OEL}$). The other output configuration involves multiplexing the MSP and LSP Registers onto the dedicated output port through the use of the $\overline{MSPSEL}$ control. When the $\overline{MSPSEL}$ control is LOW, the Most Significant Product will be available at the dedicated output port; and when $\overline{MSPSEL}$ is HIGH, the Least Significant Product will be available at this port. This configuration allows access of the entire 32-bit product by a 16-bit wide system bus.

Multiplier Input/Output Formats

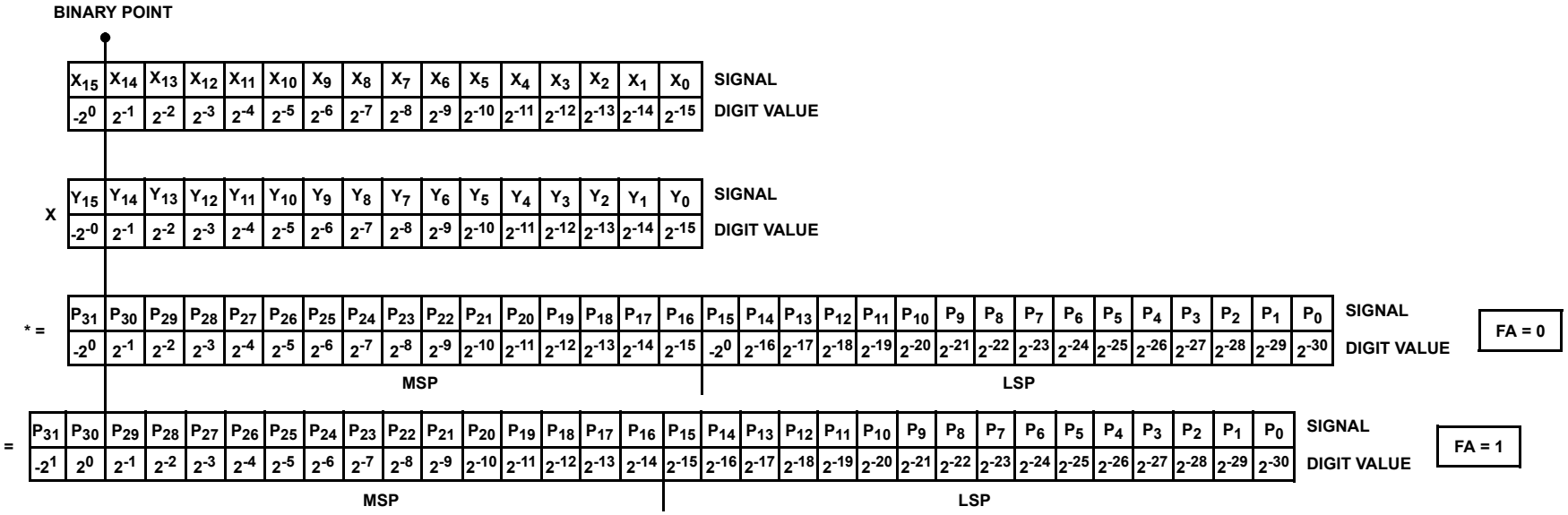


FIGURE 1. FRACTIONAL TWO'S COMPLEMENT NOTATION

NOTE: In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000 . . . 0 with 1,000 . . . 0 yielding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

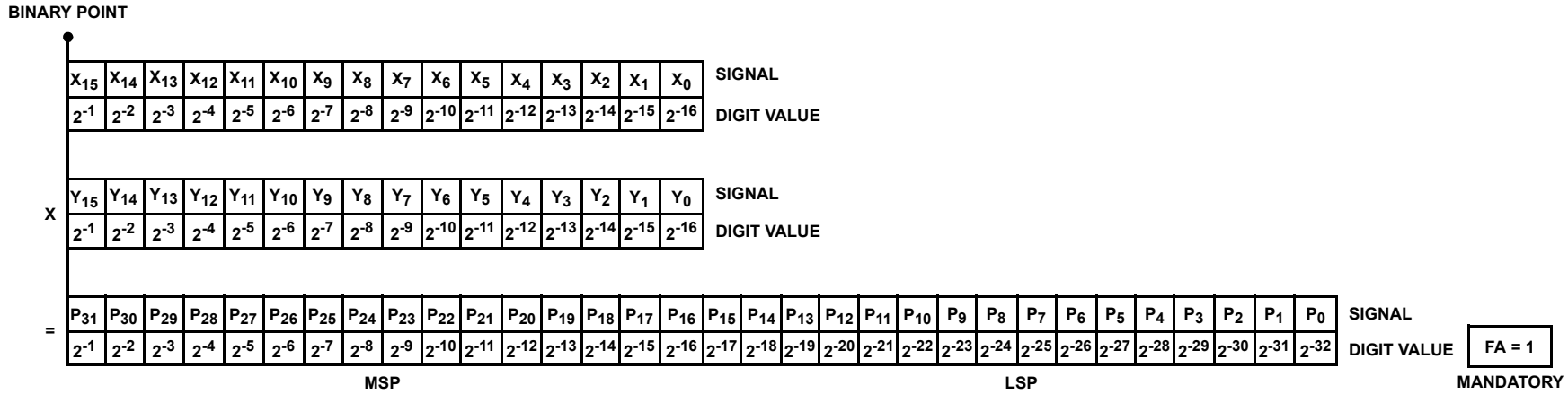


FIGURE 2. FRACTIONAL UNSIGNED MAGNITUDE NOTATION

Multiplier Input/Output Formats (Continued)

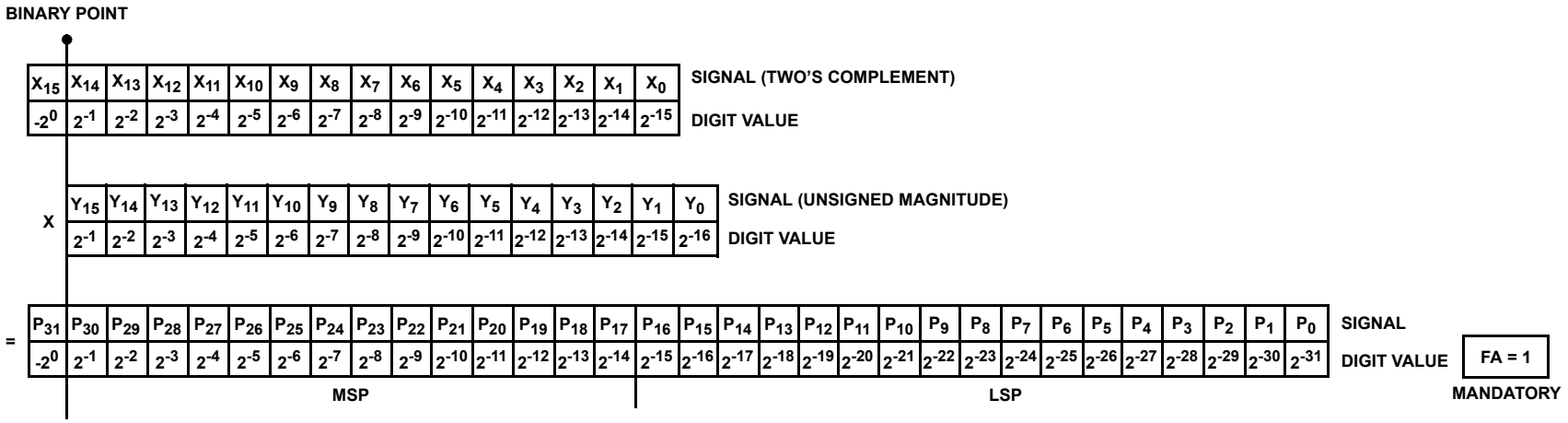


FIGURE 3. FRACTIONAL MIXED MODE NOTATION

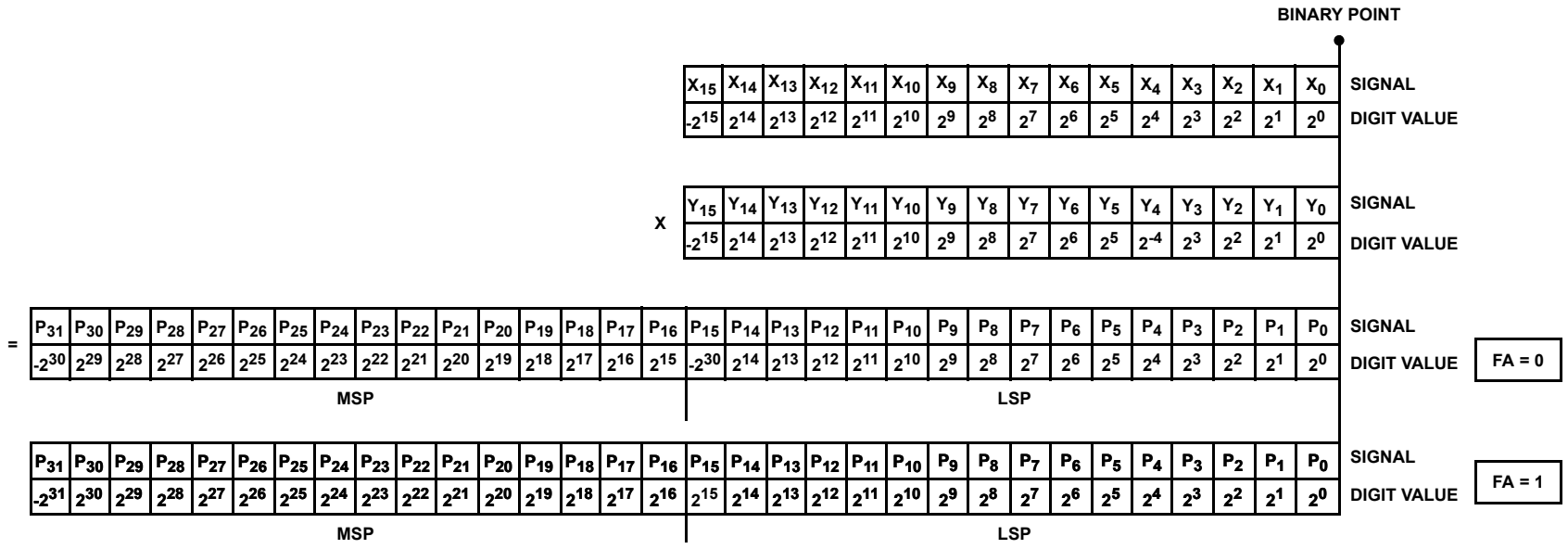


FIGURE 4. INTEGER TWO'S COMPLEMENT NOTATION

NOTE: In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000 . . . 0 with 1,000 . . . 0 yielding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

Multiplier Input/Output Formats (Continued)

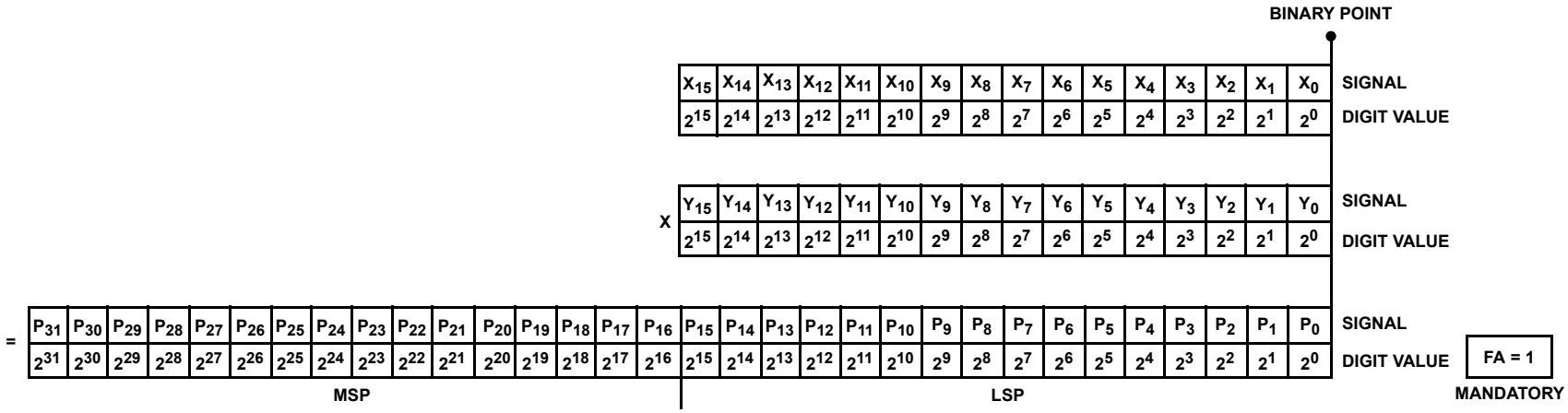


FIGURE 5. INTEGER UNSIGNED MAGNITUDE NOTATION

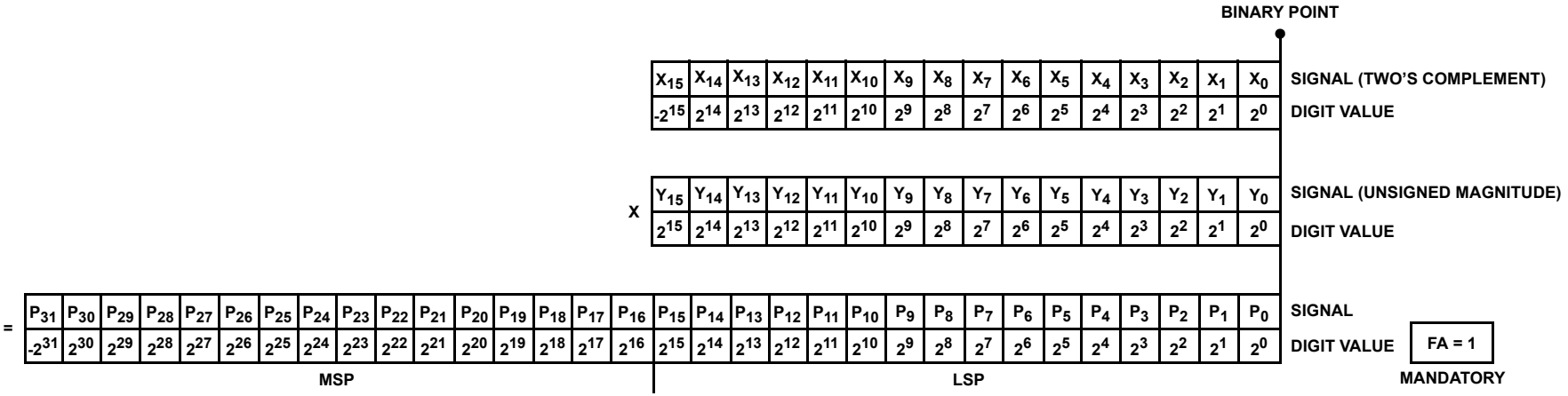


FIGURE 6. INTEGER MIXED MODE NOTATION

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage Applied . . . . . GND 0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . . 65^oC to 150^oC

Operating Conditions

Voltage Range . . . . . +4.75V to +5.25V
Temperature Range . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}(^oC/W)$	$\theta_{JC}(^oC/W)$
PLCC	43.2	15.1
CPGA	42.69	10.0

Maximum Package Power Dissipation at 70^oC
PLCC 1.7W
CPGA 2.46
Maximum Junction Temperature
PLCC . . . . . 150^oC
CPGA . . . . . 175^oC
Maximum Lead Temperature (Soldering, 10s) . . . . . 300^oC

Die Characteristics

Gate Count . . . . . 4500 Gates

CAUTION: Stresses above those listed in the ``Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating, and operation at these or any other conditions above those indicated in the operations sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications V_{CC} = 5.0V ±5%, T_A = 0^oC to 70^oC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.25V	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.75V	-	0.8	V
Output High Voltage	V_{OH}	I_{OH} = 400mA, V_{CC} = 4.75V	2.6	-	V
Output Low Voltage	V_{OL}	I_{OL} = +4.0mA, V_{CC} = 4.75V	-	0.4	V
Input Leakage Current	I_I	V_I = V_{CC} or GND, V_{CC} = 5.25V	10	10	µA
Output or I/O Leakage Current	I_O	V_O = V_{CC} or GND, V_{CC} = 5.25V	10	10	µA
Standby Power Supply Current	I_{CCSB}	V_I = V_{CC} or GND, V_{CC} = 5.25V Outputs Open	-	500	µA
Operating Power Supply Current	I_{CCOP}	V_I = V_{CC} or GND, V_{CC} = 5.25V f = 1MHz (Note 2)	-	7.0	mA

NOTE:

2. Operating Supply Current is proportional to frequency, Typical rating is 5mA/MHz.

Capacitance T_A = 25^oC, Note 3

PARAMETER	SYMBOL	TEST CONDITIONS	TYPICAL	UNITS
Input Capacitance	C_{IN}	Frequency = 1MHz. All measurements referenced to device ground.	15	pF
Output Capacitance	C_{OUT}		10	pF
I/O Capacitance	$C_{I/O}$		10	pF

NOTE:

3. Not tested, but characterized at initial design and at major process/design changes.

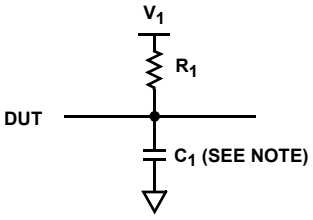
AC Electrical Specifications V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C, Note 6

PARAMETER	SYMBOL	TEST CONDITIONS	HMU16/HMU17-35		HMU16/HMU17-45		UNITS
			MIN	MAX	MIN	MAX	
Unclocked Multiply Time	t_{MUC}		-	55	-	70	ns
Clocked Multiply Time	t_{MC}		-	35	-	45	ns
X, Y, RND Setup Time	t_S		15	-	18	-	ns
X, Y, RND Hold Time	t_H		2	-	2	-	ns
Clock Pulse Width High	t_{PWH}		10	-	15	-	ns
Clock Pulse Width Low	t_{PWL}		10	-	15	-	ns
$\overline{\text{MSPSEL}}$ to Product Out	t_{PDSEL}		-	22	-	25	ns
Output Clock to P	t_{PDP}		-	22	-	25	ns
Output Clock to Y	t_{PDY}		-	22	-	25	ns
Three-State Enable Time	t_{ENA}	Note 4	-	22	-	25	ns
Three-State Disable Time	t_{DIS}		-	22	-	25	ns
Clock Enable Setup Time (HMU17 Only)	t_{SE}		15	-	15	-	ns
Clock Enable Hold Time (HMU17 Only)	t_{HE}		2	-	2	-	ns
Clock Low Hold Time CLKXY Relative to CLKML (HMU16 Only)	t_{HCL}	Note 5	0	-	0	-	ns
Output Rise Time	t_r	From 0.8V to 2.0V	-	8	-	8	ns
Output Fall Time	t_f	From 2.0V to 0.8V	-	8	-	8	ns

NOTES:

4. Transition is measured at ±200mV from steady state voltage with loading specified in AC Test Circuit, V_1 = 1.5V, R_1 = 500Ω and C_1 = 40pF.
5. To ensure the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.
6. Refer to AC Test Circuit, with V_1 = 2.4V, R_1 = 500Ω and C_1 = 40pF.

AC Test Circuit



NOTE: Includes Stray and Jig Capacitance.

AC Testing Input, Output Waveforms

NOTE: AC Testing: All parameters tested as per test circuit. Input rise and fall times are driven at 1ns/V.

Timing Diagrams

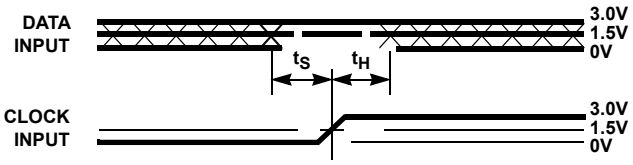


FIGURE 7. SETUP AND HOLD TIME

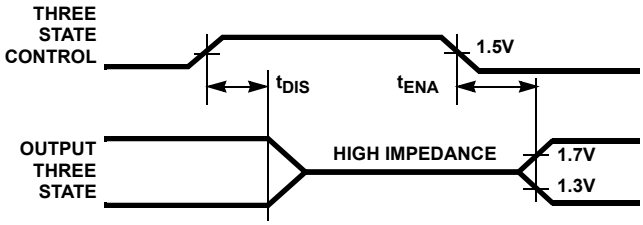


FIGURE 8. THREE-STATE CONTROL

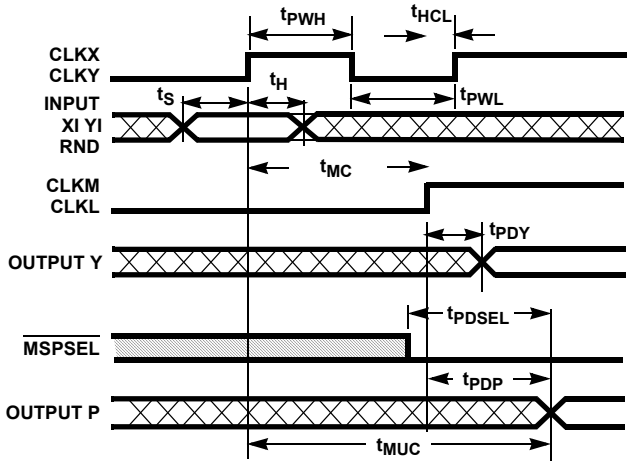


FIGURE 9. HMU16 TIMING DIAGRAM

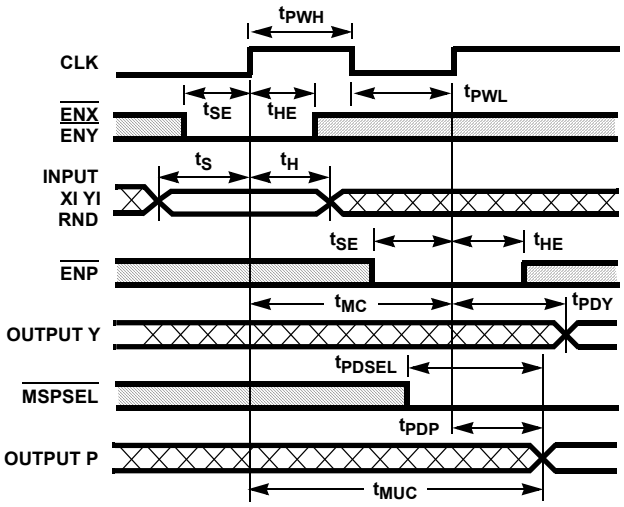
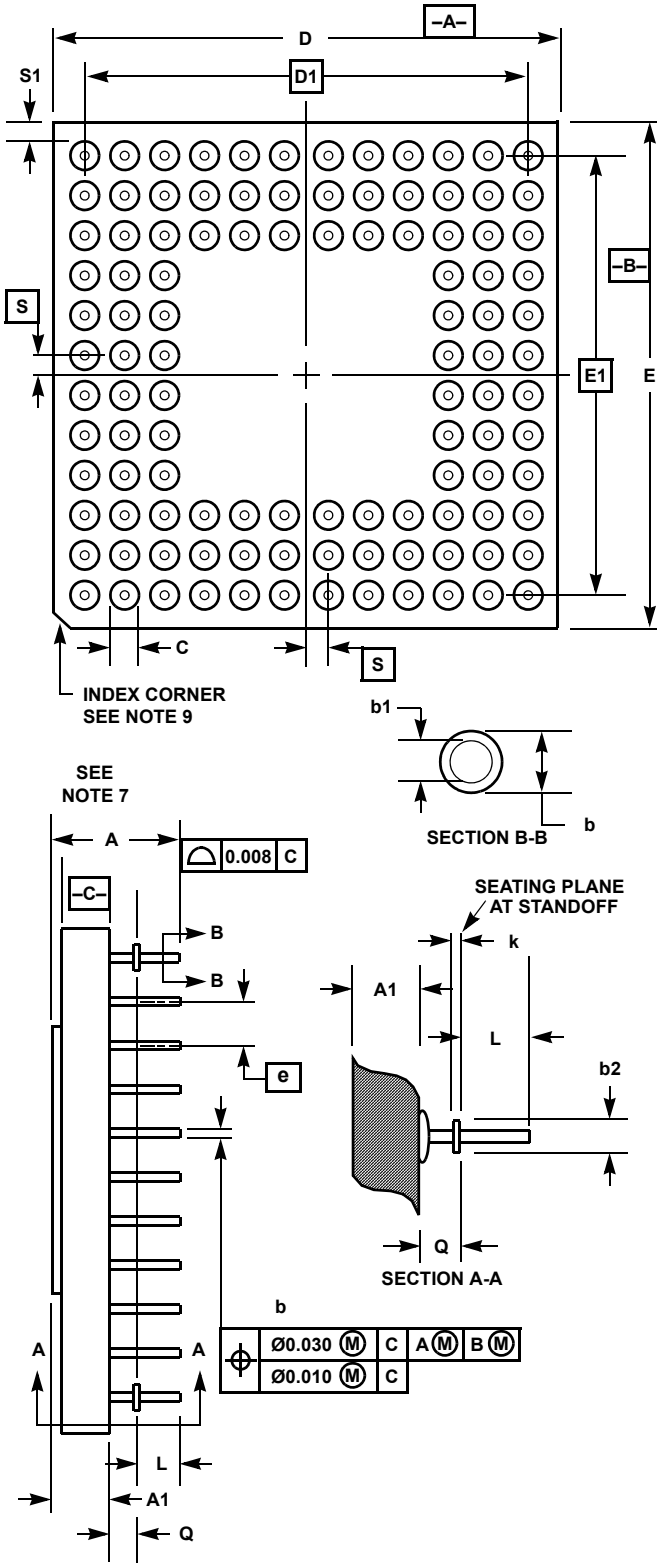


FIGURE 10. HMU17 TIMING DIAGRAM

Ceramic Pin Grid Array Packages (CPGA)



G68.B **MIL-STD-1835 CMGA3-P68D (P-AC)**
68 LEAD CERAMIC PIN GRID ARRAY PACKAGE

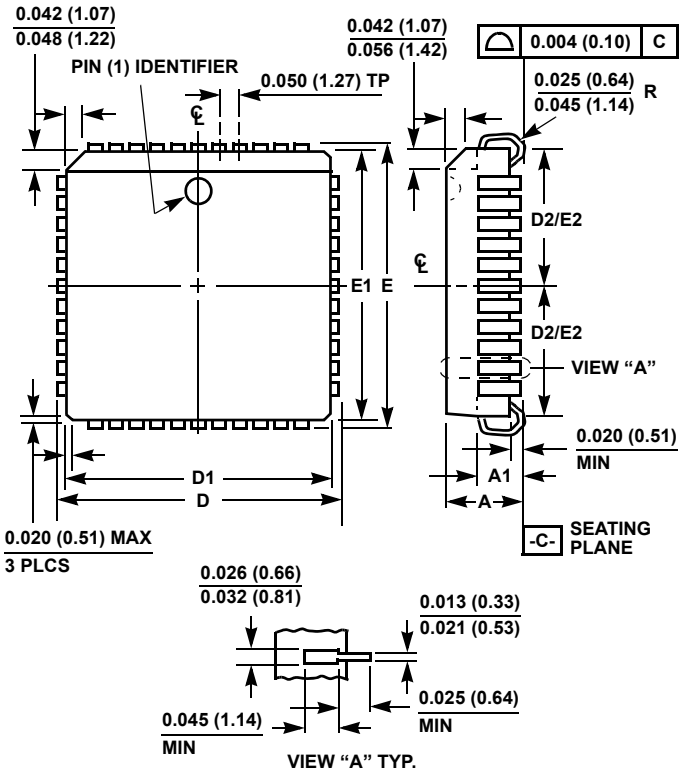
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.215	0.345	5.46	8.76	-
A1	0.070	0.145	1.78	3.68	3
b	0.016	0.0215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.042	0.058	1.07	1.47	4
C	-	0.080	-	2.03	-
D	1.140	1.180	28.96	29.97	-
D1	1.000 BSC		25.4 BSC		-
E	1.140	1.180	28.96	29.97	-
E1	1.000 BSC		25.4 BSC		-
e	0.100 BSC		2.54 BSC		6
k	0.008 REF		0.20 REF		-
L	0.120	0.140	3.05	3.56	-
Q1	0.025	0.060	0.64	1.52	5
S	0.000 BSC		0.00 BSC		10
S1	0.003	-	0.08	-	-
M	11		11		1
N	-	121	-	121	2

Rev. 0 6/20/95

NOTES:

1. “M” represents the maximum pin matrix size.
2. “N” represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension “A1” includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity down. Dimension “A1” does not include heatsinks or other attached features.
4. Standoffs are required and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimension “Q1”.
5. Dimension “Q1” applies to cavity-down configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension “S” is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling dimension: INCH.

Plastic Leaded Chip Carrier Packages (PLCC)



N68.95 (JEDEC MS-018AE ISSUE A)
68 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.985	0.995	25.02	25.27	-
D1	0.950	0.958	24.13	24.33	3
D2	0.441	0.469	11.21	11.91	4, 5
E	0.985	0.995	25.02	25.27	-
E1	0.950	0.958	24.13	24.33	3
E2	0.441	0.469	11.21	11.91	4, 5
N	68		68		6

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NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.