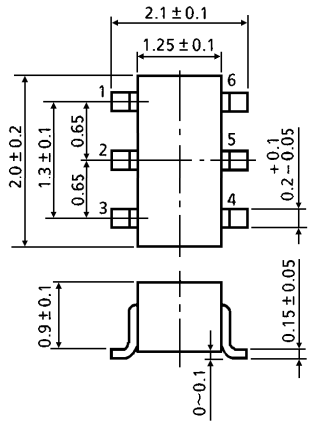
TOSHIBA FIELD EFFECT TRANSISTOR SILICON N·P CHANNEL MOS TYPE

HN1L03FU

HIGH SPEED SWITCHING APPLICATIONS

ANAROG SWITCH APPLICATIONS

Unit in mm



1. SOURCE 1 4. SOURCE 2
2. GATE 1 5. GATE 2
3. DRAIN 2 6. DRAIN 1

US6	
JEDEC	—
EIAJ	—
TOSHIBA	2-2J1C

Weight : 6.8 mg

Q1, Q2 COMMON

- Low Threshold Voltage
  Q1 : V_{th} = 0.8~2.5 V Q2 : V_{th} = −0.5~−1.5 V
- High Speed
- Small Package

Q1 MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Drain-Source Voltage	V_{DS}	50	V
Gate-Source Voltage	V_{GSS}	10	V
Drain Current	I_D	50	mA

Q2 MAXIMUM RATINGS (Ta = 25°C)

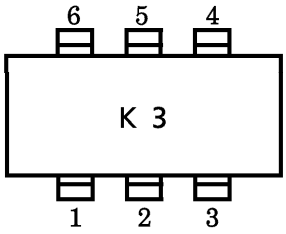
CHARACTERISTIC	SYMBOL	RATING	UNIT
Drain-Source Voltage	V_{DS}	−20	V
Gate-Source Voltage	V_{GSS}	−7	V
Drain Current	I_D	−50	mA

MAXIMUM RATINGS (Q1, Q2 COMMON) (Ta = 25°C)

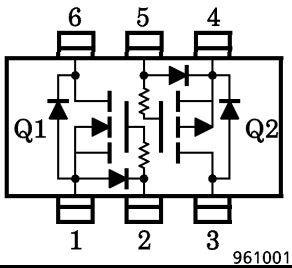
CHARACTERISTIC	SYMBOL	RATING	UNIT
Drain Power Dissipation	P_D*	200	mW
Channel Temperature	T_{ch}	150	°C
Storage Temperature Range	T_{stg}	−55 ~ 150	°C

* : Total Rating

MARKING



EQUIVALENT CIRCUIT (TOP VIEW)



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Q1 ELECTRICAL CHARACTERISTICS (Ta = 25°C)

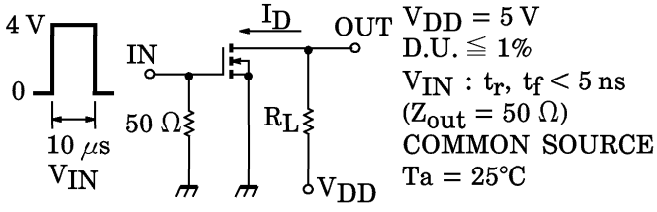
CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GSS}	V_{GS} = 10 V, V_{DS} = 0	—	—	1	μA
Drain-Source Breakdown Voltage		$V_{(BR)\,DSS}$	I_D = 100 μA, V_{GS} = 0	50	—	—	V
Drain Cut-off Current		I_{DSS}	V_{DS} = 50 V, V_{GS} = 0	—	—	1	μA
Gate Threshold Voltage		V_{th}	V_{DS} = 5 V, I_D = 0.1 mA	0.8	—	2.5	V
Forward Transfer Admittance		$\|Y_{fs}\|$	V_{DS} = 5 V, I_D = 10 mA	20	—	—	mS
Drain-Source ON Resistance		$R_{DS\,(ON)}$	I_D = 10 mA, V_{GS} = 4.0 V	—	20	50	Ω
Input Capacitance		C_{iss}	V_{DS} = 5 V, V_{GS} = 0, f = 1 MHz	—	6.3	—	pF
Reverse Transfer Capacitance		C_{rss}	V_{DS} = 5 V, V_{GS} = 0, f = 1 MHz	—	1.3	—	pF
Output Capacitance		C_{oss}	V_{DS} = 5 V, V_{GS} = 0, f = 1 MHz	—	5.7	—	pF
Switching Time	Turn-on Time	t_{on}	V_{DD} = 5 V, I_D = 10 mA, V_{GS} = 0~4.0 V	—	0.11	—	μs
	Turn-off Time	t_{off}	V_{DD} = 5 V, I_D = 10 mA, V_{GS} = 0~4.0 V	—	0.15	—	μs

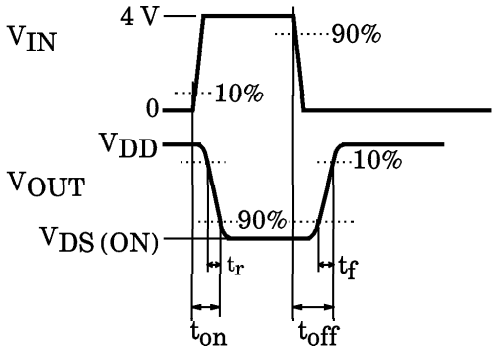
Q2 ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GSS}	V_{GS} = −7 V, V_{DS} = 0	—	—	−1	μA
Drain-Source Breakdown Voltage		$V_{(BR)\,DSS}$	I_D = −100 μA, V_{GS} = 0	−20	—	—	V
Drain Cut-off Current		I_{DSS}	V_{DS} = −20 V, V_{GS} = 0	—	—	−1	μA
Gate Threshold Voltage		V_{th}	V_{DS} = −3 V, I_D = −0.1 mA	−0.5	—	−1.5	V
Forward Transfer Admittance		$\|Y_{fs}\|$	V_{DS} = −3 V, I_D = −10 mA	15	—	—	mS
Drain-Source ON Resistance		$R_{DS\,(ON)}$	I_D = −10 mA, V_{GS} = −2.5 V	—	20	40	Ω
Input Capacitance		C_{iss}	V_{DS} = −3 V, V_{GS} = 0, f = 1 MHz	—	10.4	—	pF
Reverse Transfer Capacitance		C_{rss}	V_{DS} = −3 V, V_{GS} = 0, f = 1 MHz	—	2.8	—	pF
Output Capacitance		C_{oss}	V_{DS} = −3 V, V_{GS} = 0, f = 1 MHz	—	8.4	—	pF
Switching Time	Turn-on Time	t_{on}	V_{DD} = −3 V, I_D = −10 mA, V_{GS} = 0~−2.5 V	—	0.15	—	μs
	Turn-off Time	t_{off}	V_{DD} = −3 V, I_D = −10 mA, V_{GS} = 0~−2.5 V	—	0.13	—	μs

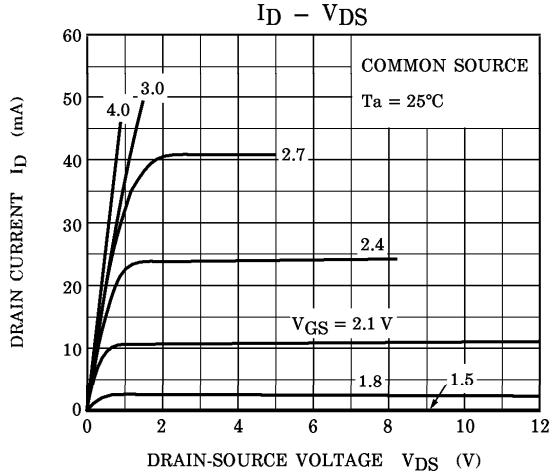
Q1 (Nch MOS FET)

SWITCHING TIME TEST CIRCUIT

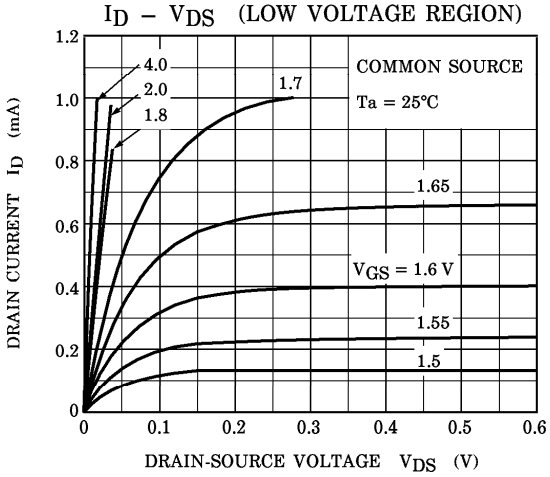




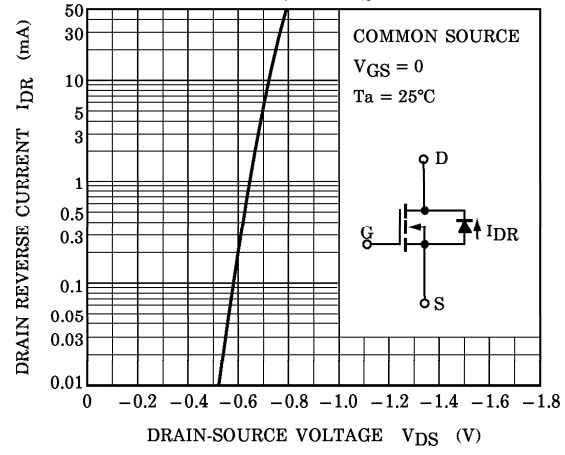
I_D – V_{DS}



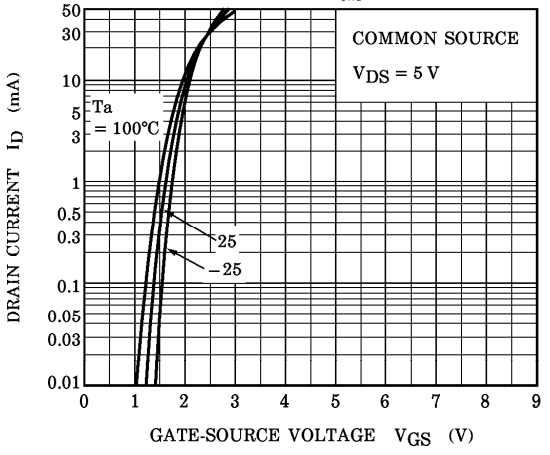
I_D – V_{DS} (LOW VOLTAGE REGION)



I_{DR} – V_{DS}

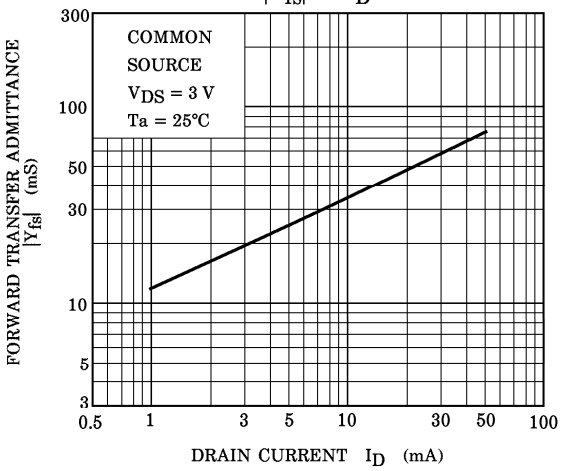


I_D – V_{GS}

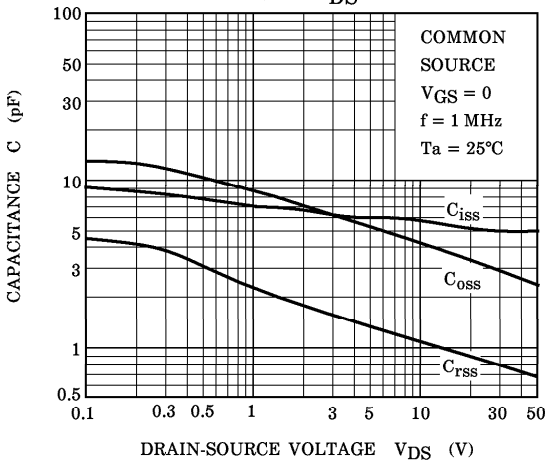


Q1 (Nch MOS FET)

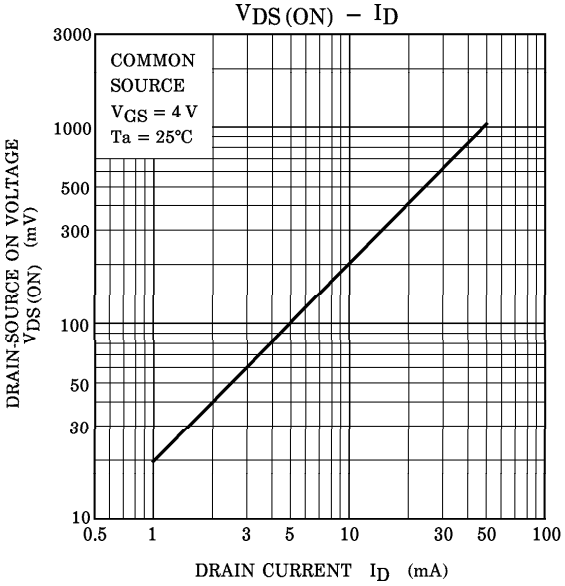
$|Y_{fs}|$ – I_D



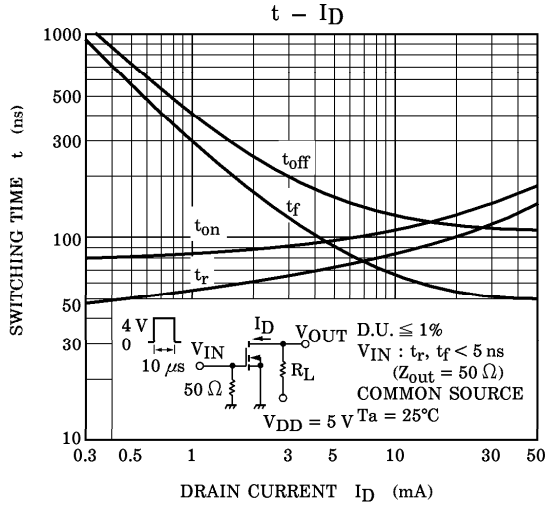
C – V_{DS}



$V_{DS\,(ON)}$ – I_D

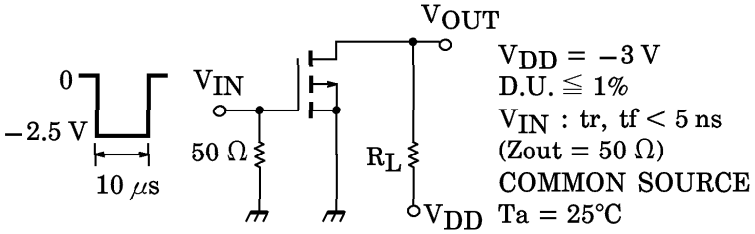


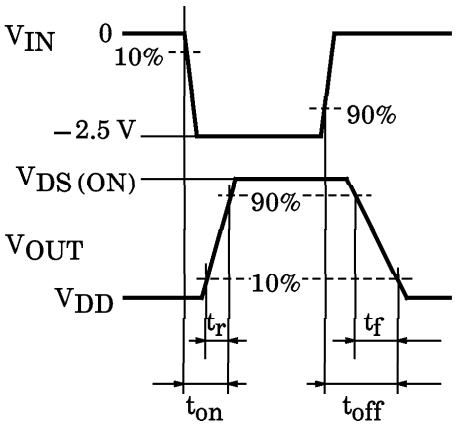
t – I_D

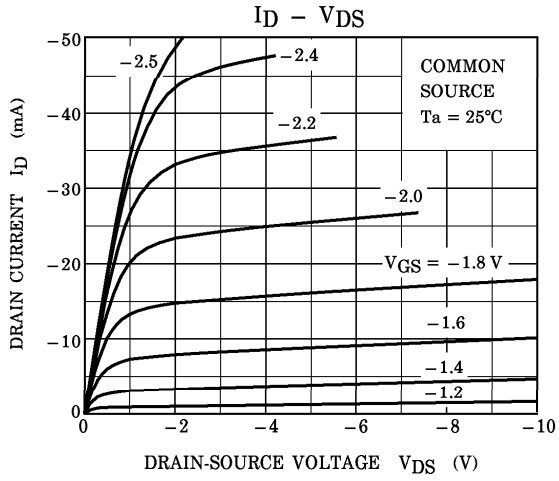


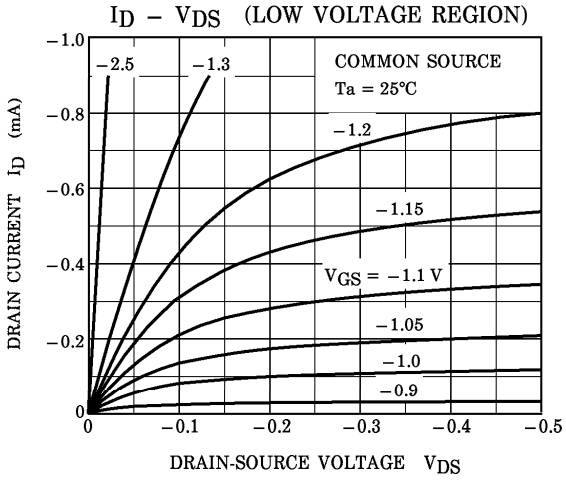
Q2 (Pch MOS FET)

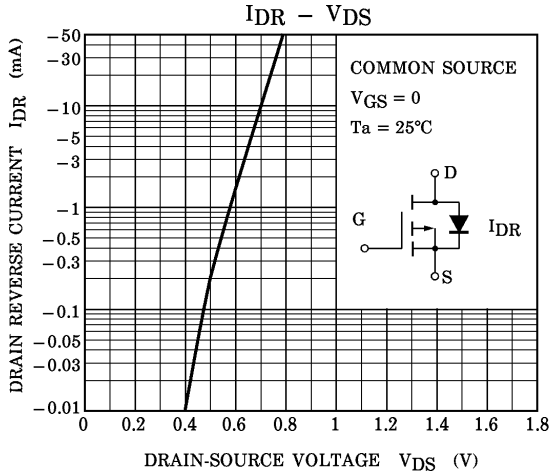
SWITCHING TIME TEST CIRCUIT

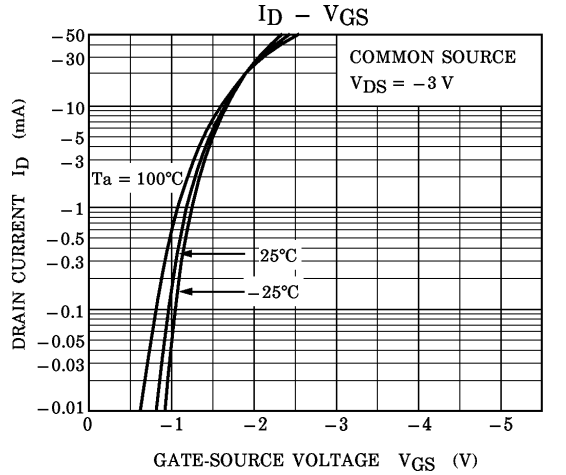






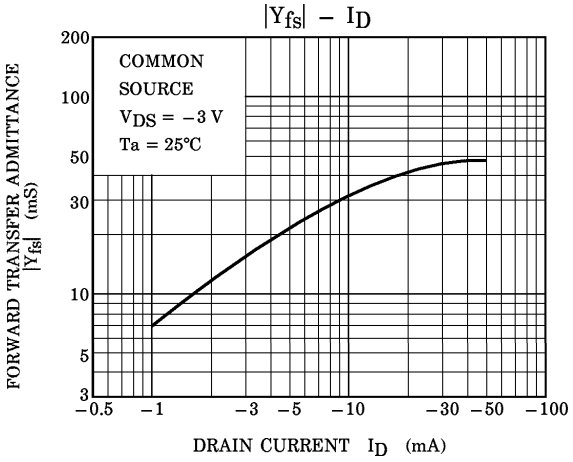




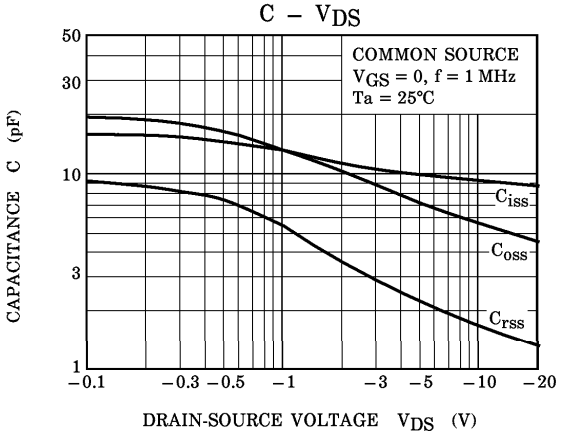


Q2 (Pch MOS FET)

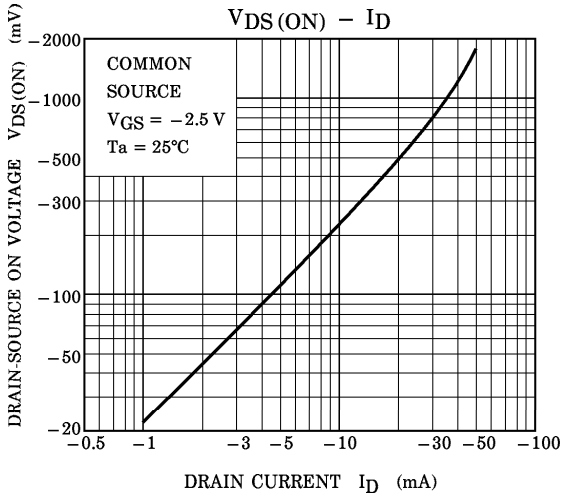
$|Y_{fs}|$ – I_D



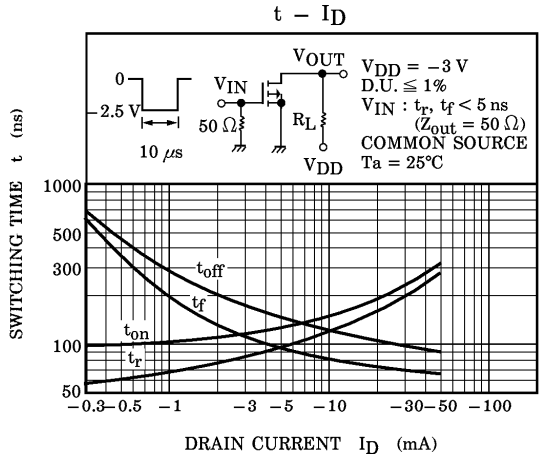
C – V_{DS}



$V_{DS\,(ON)}$ – I_D

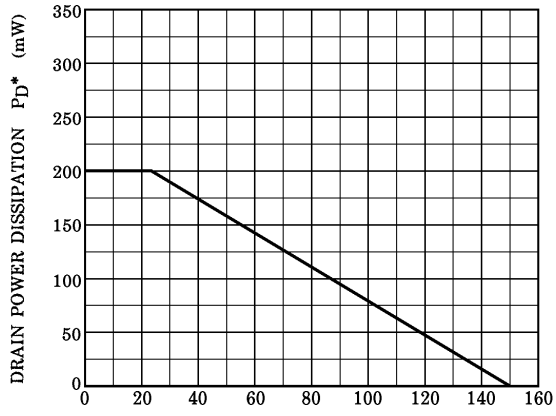


t – I_D



(Q1, Q2 COMMON)

P_D* – Ta



* : Total Rating