

# HN27C4001 Series

## 4M (512K x 8-bit) UV and OTP EPROM

### DESCRIPTION

The Hitachi HN27C4001 is a 4-Megabit Ultraviolet Erasable and One-Time Programmable Electrically Programmable Read Only Memory organized as 524,288 x 8-bits.

The HN27C4001 features fast address access times of 100, 120 and 150 ns and low power dissipation. This combination makes the HN27C4001 suitable for high speed 16 and 32-bit microcomputer systems. The HN27C4001 offers high speed programming using page programming mode.

Hitachi's HN27C4001 is offered in JEDEC-Standard Byte-Wide EPROM pinouts in 32-pin Ceramic DIP. This allows socket replacement with Mask ROMs and Flash Memory. The HN27C4001 is also available in 32-lead Plastic TSOP packages with both standard and reverse bend leads.

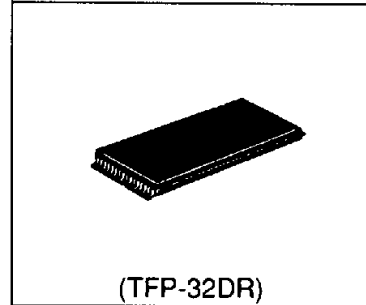
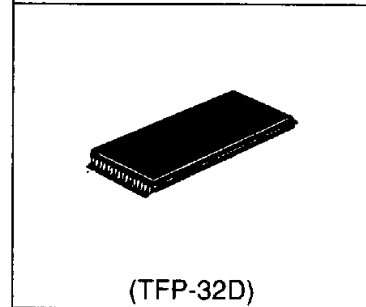
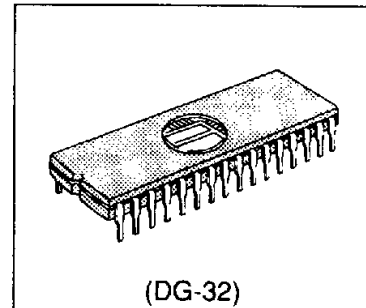
The Ceramic DIP package is erasable by exposure to Ultraviolet light. The TSOP packaged device is One-Time Programmable and once programmed, can not be rewritten.

### FEATURES

- Fast Access Times:  
100 ns/120 ns/150 ns (max)
- Single Power Supply:  
 $V_{CC} = 5 V \pm 10\%$
- Low Power Dissipation:  
Active Mode: 35 mW/MHz (typ)  
Standby Mode: 5  $\mu$ W (max)
- High Speed Page and Word Programming:  
Page Programming Time: 3.5 sec (min)
- Programming Power Supply:  
 $V_{PP} = 12.5 V \pm 0.3 V$
- Pin Arrangement:  
JEDEC Standard Byte-Wide EPROM  
Mask ROM and Flash Memory Compatible
- Packages:  
32-pin Ceramic DIP  
32-lead Plastic TSOP (Type II)

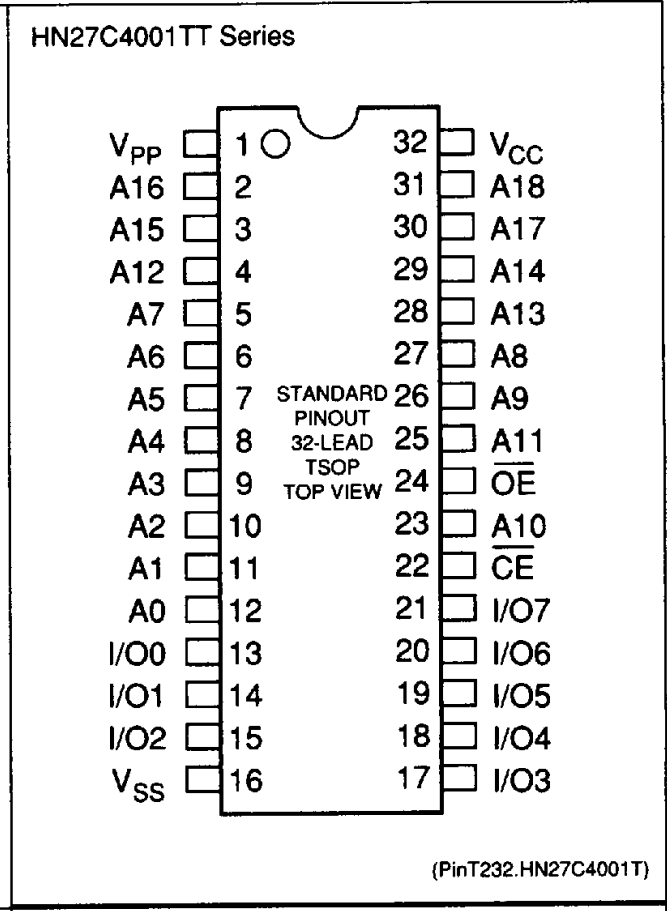
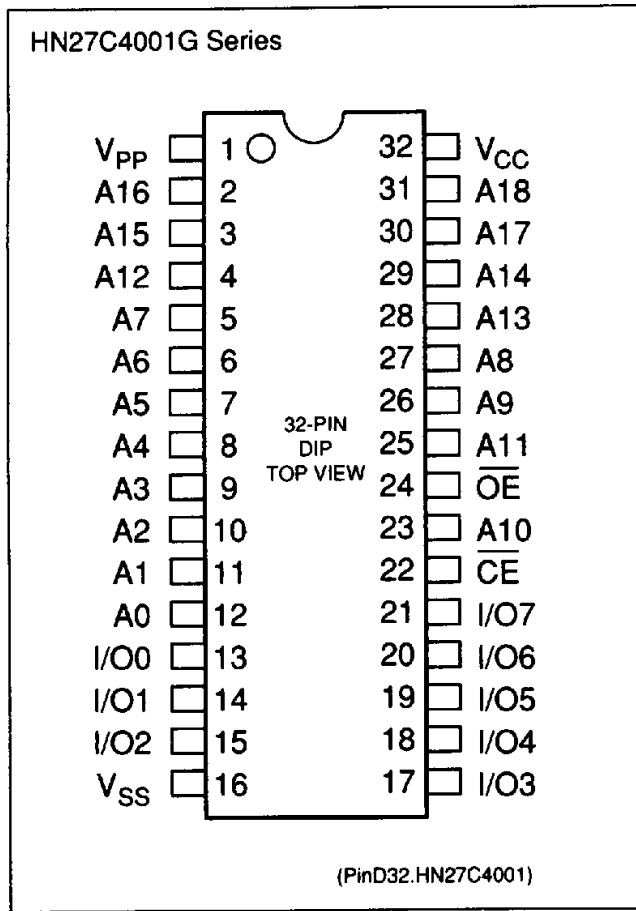
### ORDERING INFORMATION

Type No.	Access Time	Package
HN27C4001G-10	100 ns	32-pin Ceramic DIP
HN27C4001G-12	120 ns	(DG-32)
HN27C4001G-15	150 ns	
HN27C4001TT-12	120 ns	32-lead Plastic TSOP
HN27C4001TT-15	150 ns	(TFP-32D)
HN27C4001RR-12	120 ns	32-lead Plastic TSOP
HN27C4001RR-15	150 ns	(TFP-32D) Reverse bend



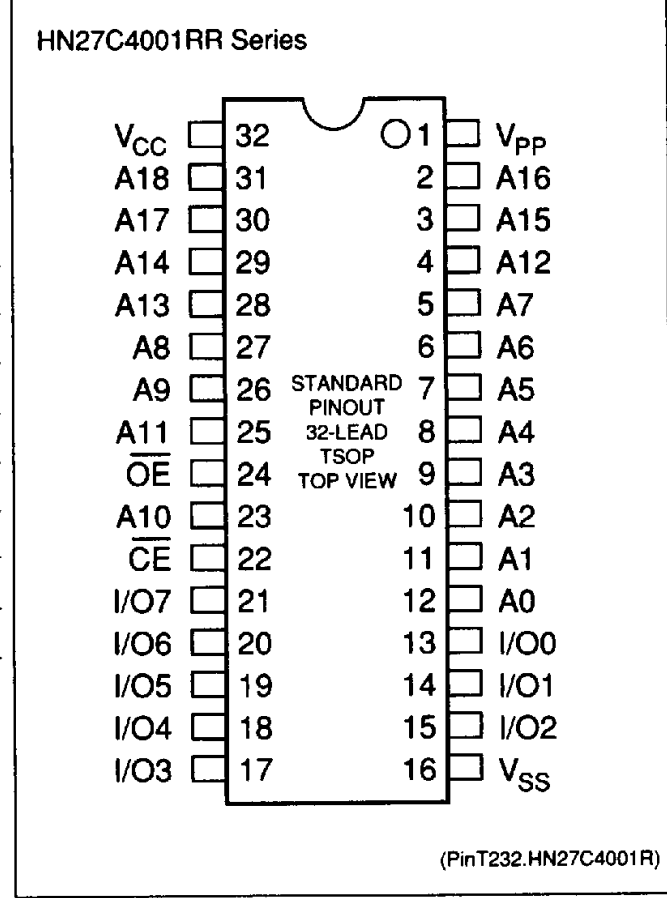
# HN27C4001 Series

## PIN ARRANGEMENT



## PIN DESCRIPTION

Pin Name	Function
A <sub>0</sub> - A <sub>18</sub>	Address
I/O <sub>0</sub> - I/O <sub>7</sub>	Input/Output
CE	Chip Enable
OE	Output Enable
V <sub>CC</sub>	Power Supply
V <sub>PP</sub>	Programming Supply
V <sub>SS</sub>	Ground





# HN27C4001 Series

## ■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage <sup>1</sup>	$V_{CC}$	-0.6 to +7.0	V
Programming Voltage <sup>1</sup>	$V_{PP}$	-0.6 to +13.5	V
All Input and Output Voltage <sup>1,2</sup>	$V_{IN}, V_{OUT}$	-0.6 to +7.0	V
$A_9$ and $\overline{OE}$ Voltage <sup>2</sup>	$V_{ID}$	-0.6 to +13.0	V
Operating Temperature Range	$T_{OPR}$	0 to +70	°C
Storage Temperature Range <sup>3</sup>	$T_{STG}$	-65 to +125 <sup>4</sup> -55 to +125 <sup>5</sup>	°C
Storage Temperature Under Bias	$T_{BIAS}$	-20 to +80 <sup>4</sup> -10 to +80 <sup>5</sup>	°C

- Notes:
1. Relative to  $V_{SS}$ .
  2.  $V_{IN}$ ,  $V_{OUT}$ , and  $V_{ID}$  min = -2.0V for pulse width  $\leq$  20 ns.
  3. Device storage temperature range before programming.
  4. HN27C4001G.
  5. HN27C4001TT and HN27C4001RR.

## ■ CAPACITANCE ( $T_a = 25^\circ\text{C}$ , $f = 1\text{MHz}$ )

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	$C_{IN}$	-	-	12	pF	$V_{IN} = 0\text{V}$
Output Capacitance	$C_{OUT}$	-	-	20	pF	$V_{OUT} = 0\text{V}$

## ■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $V_{CC} = 5\text{V} \pm 10\%$ ,  $V_{PP} = V_{SS}$  to  $V_{CC}$ ,  $T_a = 0$  to  $70^\circ\text{C}$ )

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	$I_{LI}$	-	-	2	$\mu\text{A}$	$V_{IN} = 5.5\text{V}$
Output Leakage Current	$I_{LO}$	-	-	2	$\mu\text{A}$	$V_{OUT} = 5.5\text{V}/0.45\text{V}$
Operating $V_{CC}$ Current	$I_{CC1}$	-	-	30	mA	$I_{OUT} = 0\text{mA}$ , $f = 1\text{MHz}$
	$I_{CC2}$	-	-	100 <sup>3</sup> 90 <sup>4</sup>	mA mA	$I_{OUT} = 0\text{mA}$ , $f = 10\text{MHz}$ $I_{OUT} = 0\text{mA}$ , $f = 8.4\text{MHz}$
Standby $V_{CC}$ Current	$I_{SB1}$	-	-	1	mA	$\overline{CE} = V_{IH}$
	$I_{SB2}$	-	1	20	$\mu\text{A}$	$\overline{CE} = V_{CC} \pm 0.3\text{V}$
$V_{PP}$ Current	$I_{PP1}$	-	1	20	$\mu\text{A}$	$V_{PP} = 5.5\text{V}$
Input Voltage	$V_{IH}$	2.2	-	$V_{CC} + 1$ <sup>2</sup>	V	
	$V_{IL}$	-0.3 <sup>1</sup>	-	0.8	V	
Output Voltage	$V_{OH}$	2.4	-	-	V	$I_{OH} = -400\mu\text{A}$
	$V_{OL}$	-	-	0.45	V	$I_{OL} = 2.1\text{mA}$

- Notes:
1.  $V_{IL}$  min = -1.0 V for pulse width  $\leq$  50 ns.  
 $V_{IL}$  min = -2.0 V for pulse width  $\leq$  20 ns.
  2.  $V_{IH}$  max =  $V_{CC} + 1.5\text{V}$  for pulse width  $\leq$  20 ns.  
If  $V_{IH}$  is over the specified maximum value, Read operation can not be guaranteed.
  3. HN27C4001G.
  4. HN27C4001TT and HN27C4001RR.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

( $V_{CC} = 5V \pm 10\%$ ,  $V_{PP} = V_{SS}$  to  $V_{CC}$ ,  $T_a = 0$  to  $70^\circ C$ )

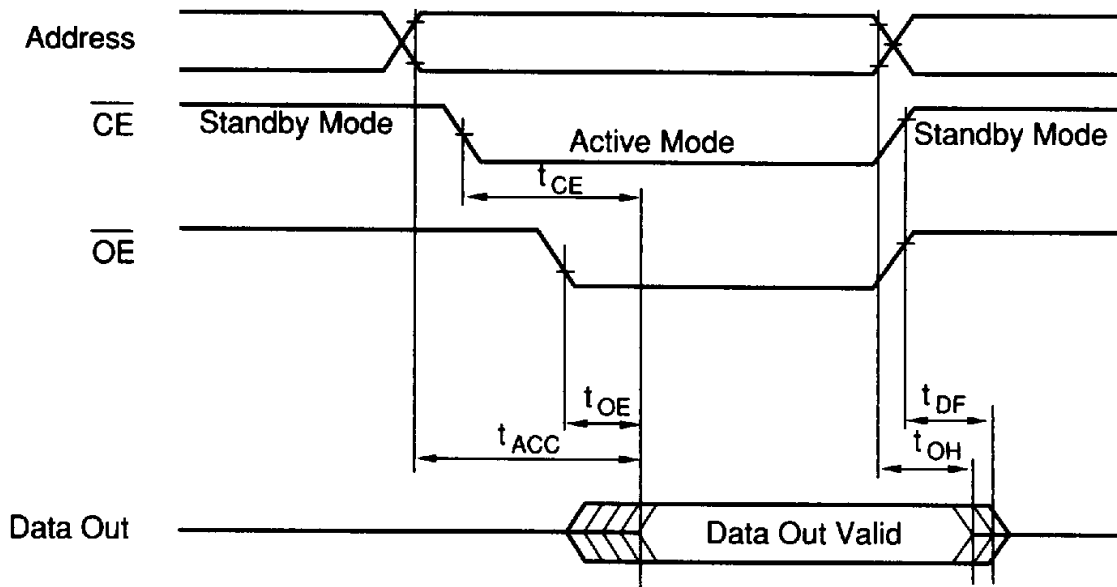
Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times:  $\leq 10$  ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V/2.0 V

Item	Symbol	HN27C4001-10		HN27C4001-12		HN27C4001-15		Unit	Test Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
Address Access Time	$t_{ACC}$	-	100	-	120	-	150	ns	$\overline{CE} = \overline{OE} = V_{IL}$
Chip Enable Access Time	$t_{CE}$	-	100	-	120	-	150	ns	$\overline{OE} = V_{IL}$
Output Enable Access Time	$t_{OE}$	-	60	-	60	-	70	ns	$\overline{CE} = V_{IL}$
Output Disable to High-Z <sup>1</sup>	$t_{DF}$	0	35	0	40	0	50	ns	$\overline{CE} = V_{IL}$
Output Hold to Address Change	$t_{OH}$	5	-	5	-	5	-	ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note: 1.  $t_{DF}$  is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ READ TIMING WAVEFORM



(T.D.R.HN27C4001)

**■ DC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS**
 $(V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}, V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}, T_a = 25 \text{ }^\circ\text{C} \pm 5 \text{ }^\circ\text{C})$ 

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	$I_{LI}$	-	-	2	$\mu\text{A}$	$V_{IN} = 6.5 \text{ V} / 0.45 \text{ V}$
Operating $V_{CC}$ Current	$I_{CC}$	-	-	50	$\text{mA}$	
Operating $V_{PP}$ Current	$I_{PP}$	-	-	70	$\text{mA}$	$\overline{CE} = V_{IL}$
Input Voltage <sup>3</sup>	$V_{IH}$	2.2	-	$V_{CC} + .5$ <sup>6</sup>	$\text{V}$	
	$V_{IL}$	-0.1 <sup>5</sup>	-	0.8	$\text{V}$	
	$V_H$	11.5	12.0	12.5	$\text{V}$	
Output Voltage	$V_{OH}$	2.4	-	-	$\text{V}$	$I_{OH} = -400 \mu\text{A}$
	$V_{OL}$	-	-	0.45	$\text{V}$	$I_{OH} = 2.1 \text{ mA}$

- Notes:
- $V_{CC}$  must be applied before  $V_{PP}$  and removed after  $V_{PP}$ .
  - $V_{PP}$  must not exceed 13 V, including overshoot.
  - Device reliability may be adversely affected if the device is installed or removed while  $V_{PP} = 12.5 \text{ V}$ .
  - Do not change  $V_{PP}$  from  $V_{IL}$  to 12.5 V or 12.5 V to  $V_{IL}$  when  $\overline{CE} = \text{low}$ .
  - $V_{IL} \text{ min} = -0.6 \text{ V}$  for pulse width  $\leq 20 \text{ ns}$ .
  - If  $V_{IH}$  is over the specified maximum value, programming operation can not be guaranteed.

### ■ AC ELECTRICAL CHARACTERISTICS FOR PROGRAMMING OPERATIONS

( $V_{CC} = 6.25 \text{ V} \pm 0.25 \text{ V}$ ,  $V_{PP} = 12.5 \text{ v} \pm 0.3 \text{ V}$ ,  $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ )

#### Test Conditions

- Input pulse levels: 0.45 V / 2.4 V
- Input rise and fall times:  $\leq 20 \text{ ns}$
- Reference levels for measuring timing: 0.8 V / 2.0V

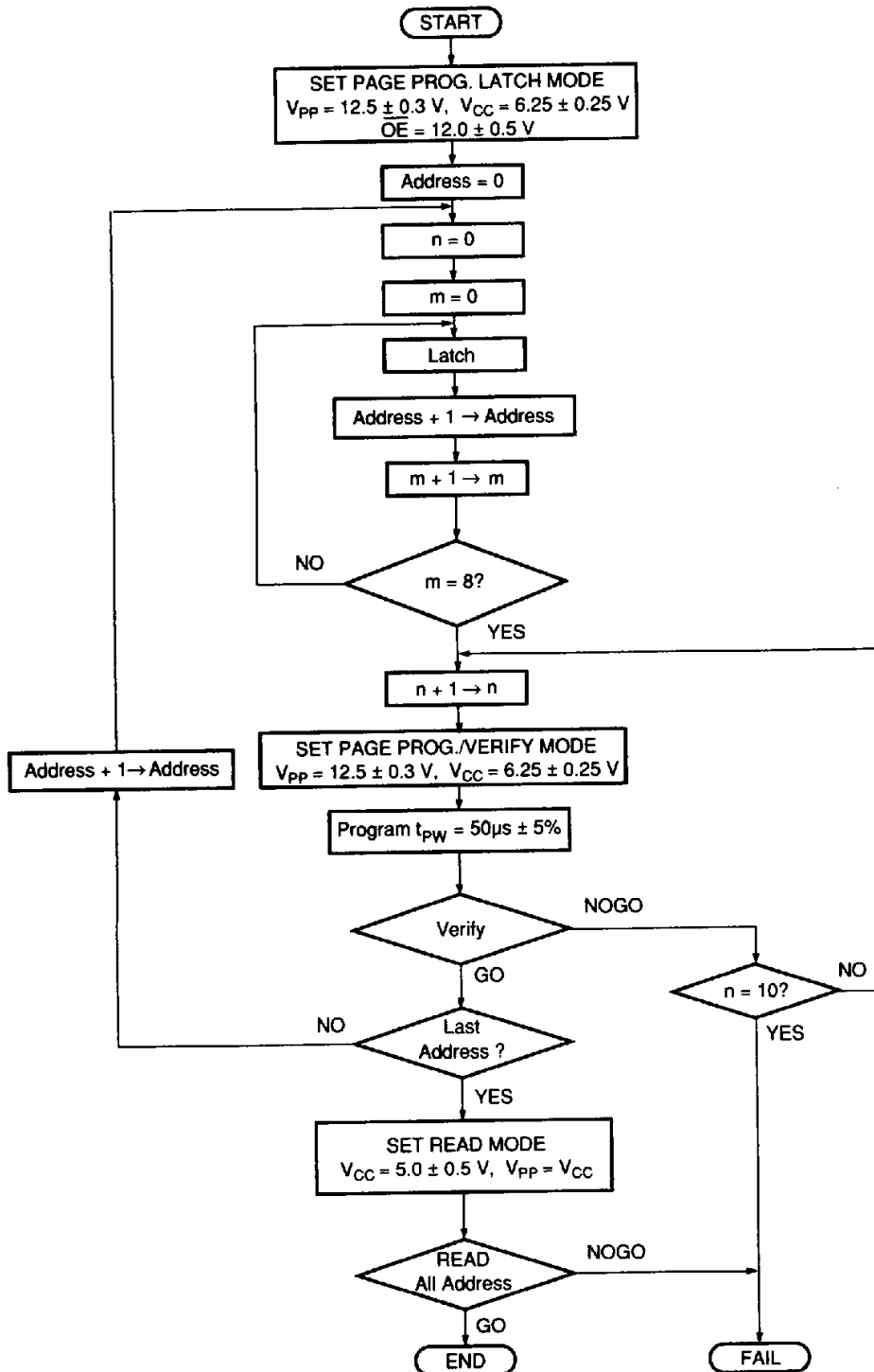
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Address Setup Time	$t_{AS}$	2	-	-	$\mu\text{s}$	
Address Hold Time	$t_{AH}$	0	-	-	$\mu\text{s}$	
Data Setup Time	$t_{DS}$	2	-	-	$\mu\text{s}$	
Data Hold Time	$t_{DH}$	2	-	-	$\mu\text{s}$	
Chip Enable Setup Time	$t_{CES}$	2	-	-	$\mu\text{s}$	
$V_{PP}$ Setup Time	$t_{VPS}$	2	-	-	$\mu\text{s}$	
$V_{CC}$ Setup Time	$t_{VCS}$	2	-	-	$\mu\text{s}$	
Output Enable Setup Time	$t_{OES}$	2	-	-	$\mu\text{s}$	
Output Disable Time	$t_{DF}$	0	-	130	ns	
Programming Pulse Width	$t_{PW}$	47.5	50.0	52.5	$\mu\text{s}$	
Data Valid from Output Enable Time	$t_{OE}$	0	-	150	ns	
Chip Enable Pulse Width During Data Latch	$t_{LW}$	1	-	-	$\mu\text{s}$	
Output Enable = $V_H$ Setup Time	$t_{OHS}$	2	-	-	$\mu\text{s}$	
Output Enable = $V_H$ Hold Time	$t_{OHH}$	2	-	-	$\mu\text{s}$	
Output Enable Hold Time	$t_{OEH}$	2	-	-	$\mu\text{s}$	
$V_{PP}$ Hold Time	$t_{VRS}$	1	-	-	$\mu\text{s}$	
Page Programming Reset Time	$t_{VLW}$	1	-	-	$\mu\text{s}$	

Note: 1.  $t_{DF}$  is defined as the time at which the output becomes an open circuit and data is no longer driven.

## ■ PAGE PROGRAMMING FLOWCHART

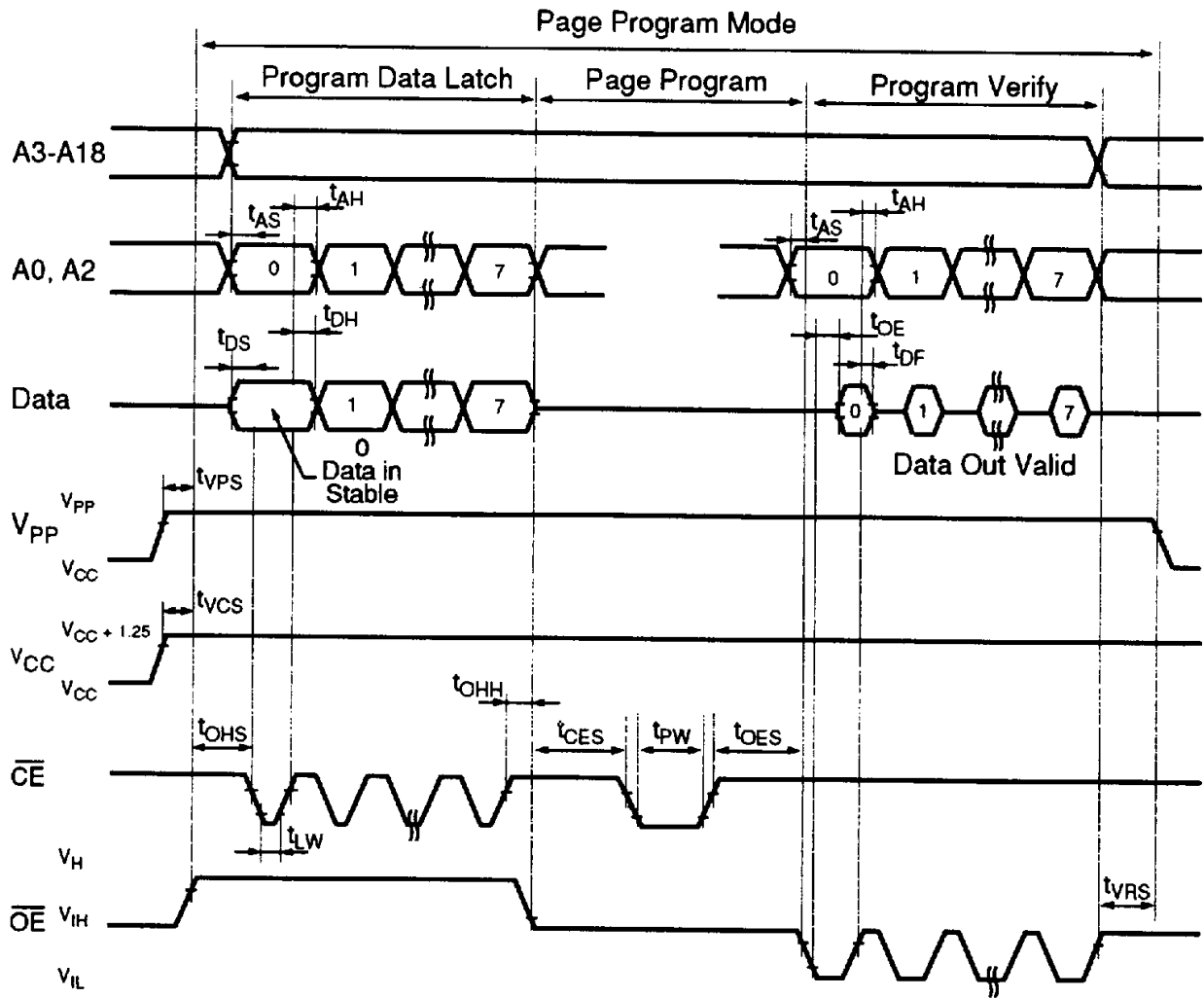
The Hitachi HN27C4001 can be programmed with the high performance Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

- Note:
1. To set the device into Page Programming, apply 12.5 V to  $V_{PP}$  then followed by applying 12 V to  $\overline{OE}$ . The device operates in Page Program Mode until reset.
  2. To reset the Page Program Mode, set  $V_{PP} = V_{CC}$  or less.





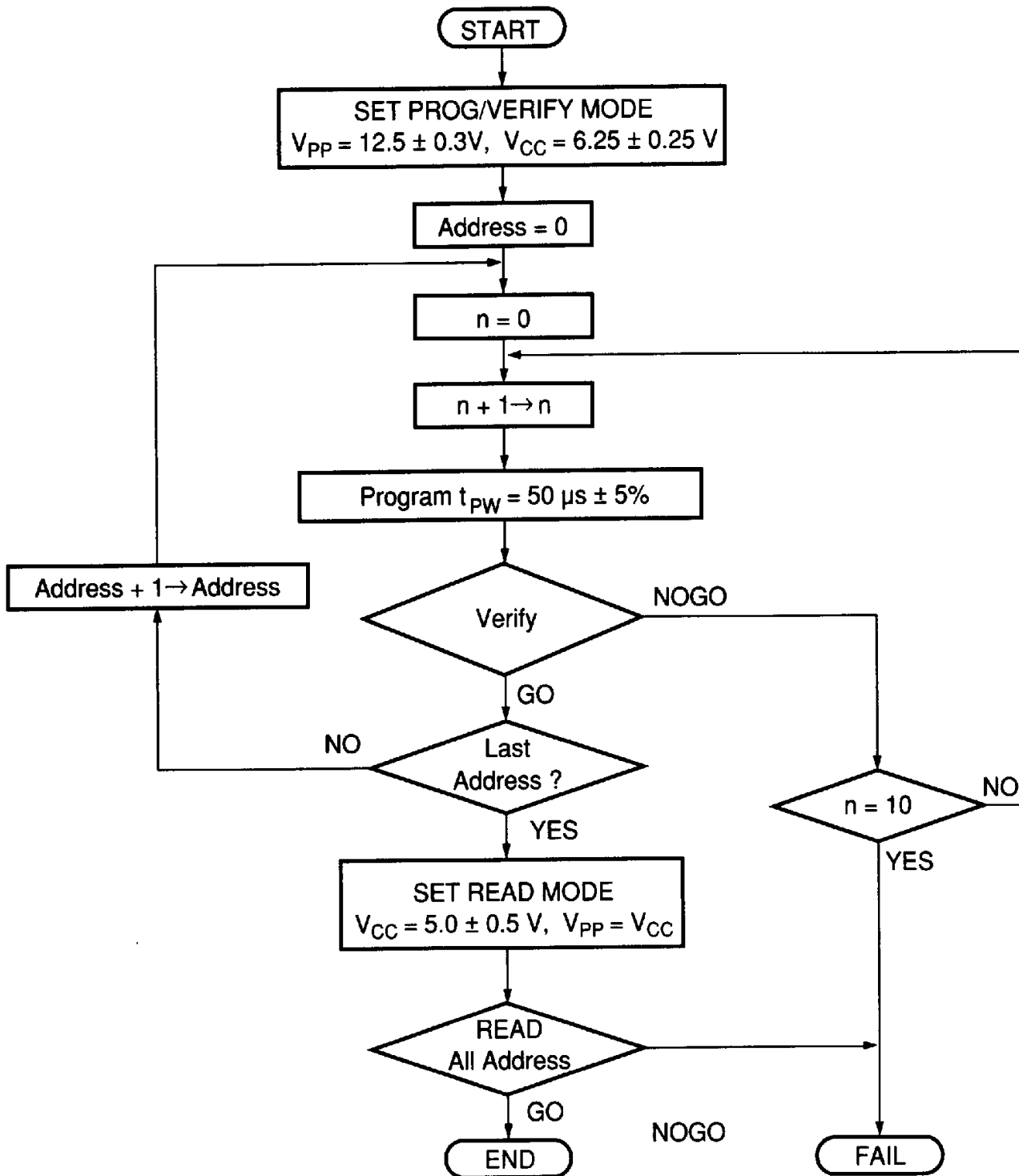
■ PAGE PROGRAMMING TIMING WAVEFORM



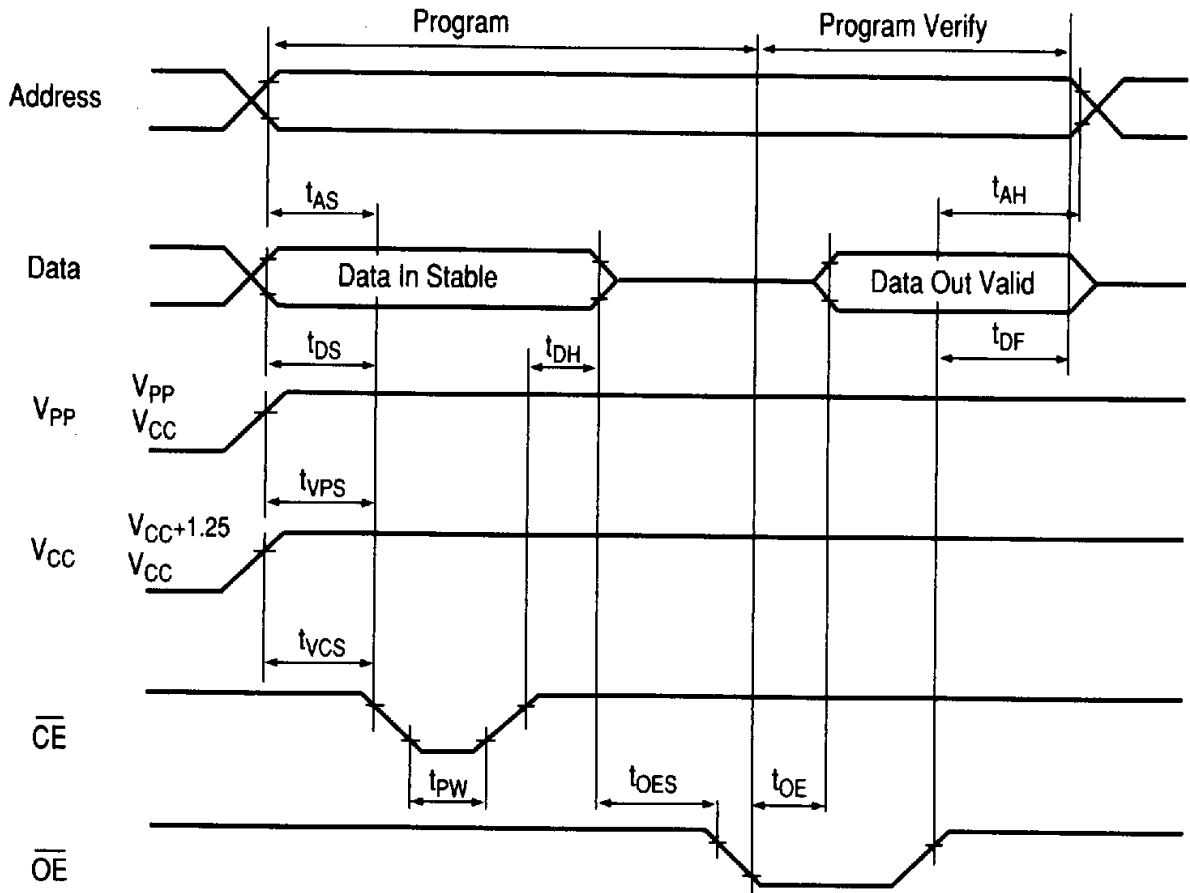
(TD.PP.HN27C4001)

■ BYTE PROGRAMMING FLOWCHART

The Hitachi HN27C4096H can be programmed with the high performance Byte Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.



■ BYTE PROGRAMMING TIMING WAVEFORM



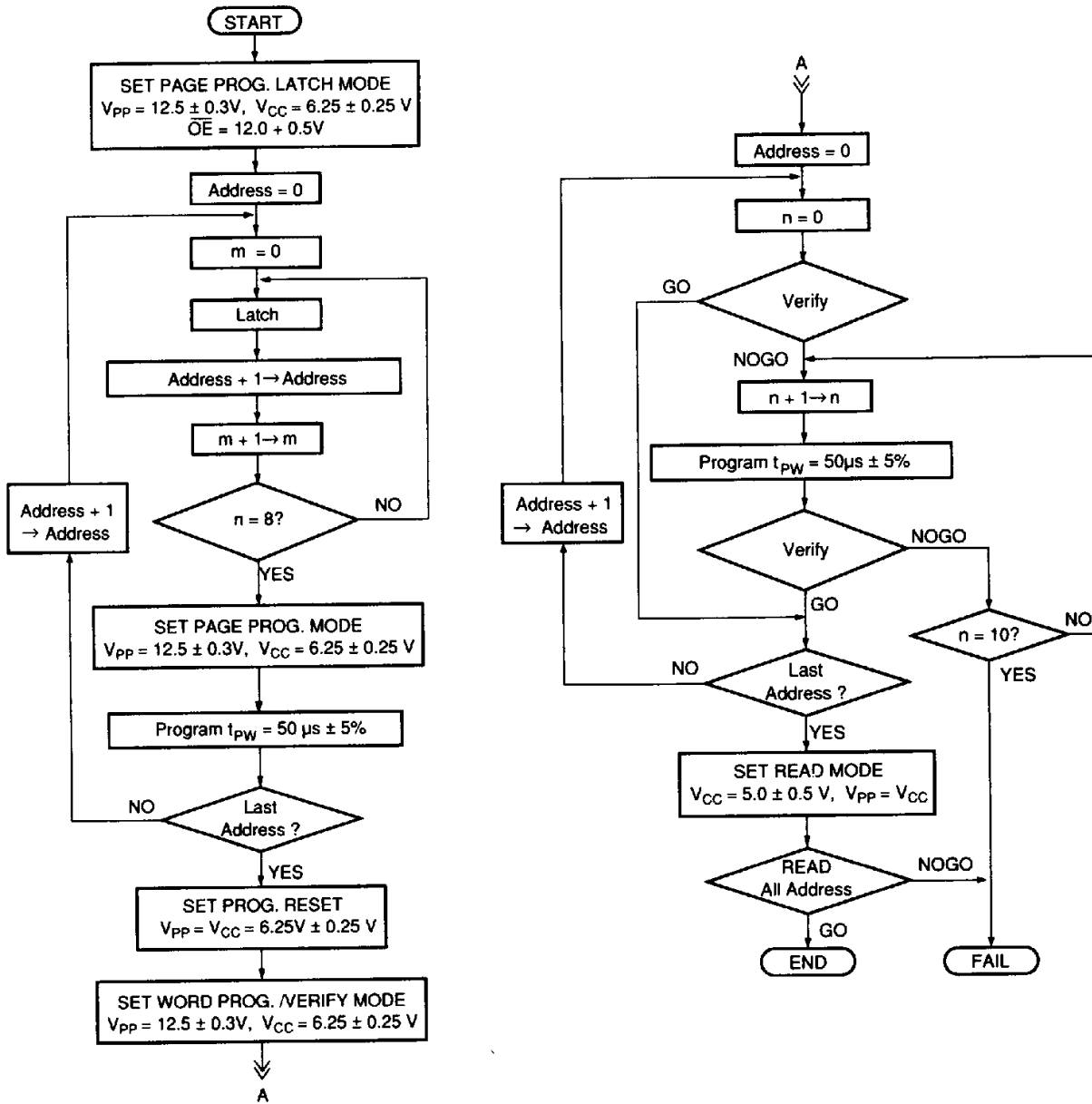
(TD.P.HN27C4001)

OPTIONAL PAGE PROGRAMMING FLOWCHART

The Hitachi HN27C4001 can be programmed with the high performance Optional Page Programming algorithm shown in the following flowchart. This algorithm provides a fast programming time without voltage stress to the device or deterioration in reliability of programmed data.

This programming algorithm is a combination of Page Programming and Byte Verify. It can be used to avoid the increased programming verify time when a programmer with a slower machine cycle is used and shorten the total programming time.

Please refer to the timing specifications for page programming and byte programming.





## HN27C4001 Series

### ■ ERASING THE HN27C4001

The Hitachi HN27C4001 Ceramic DIP package allows the device to be erased by exposure to ultraviolet light of 2537Å. All of the data is changed to "1" after this erasure procedure. The minimum integrated dose (UV intensity x exposure time) for erasure is 15 W-sec/cm<sup>2</sup>.

### ■ DEVICE IDENTIFIER MODE DESCRIPTION

The Device Identifier Mode allows binary codes to be read from the outputs that identify the manufacturer and the type of device. Using this mode with programming equipment, the device will automatically match its own erase and programming algorithm.

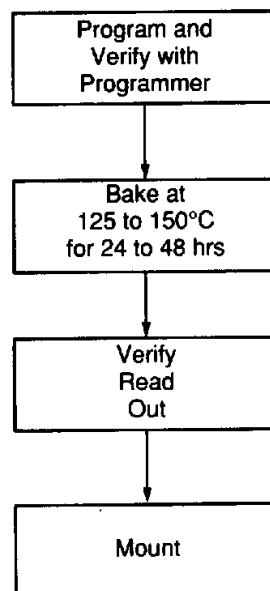
### ■ HN27C4001 SERIES IDENTIFIER CODE

Identifier	A <sub>0</sub>	I/O <sub>7</sub>	I/O <sub>6</sub>	I/O <sub>5</sub>	I/O <sub>4</sub>	I/O <sub>3</sub>	I/O <sub>2</sub>	I/O <sub>1</sub>	I/O <sub>0</sub>	Hex Data
Manufacturer Code	V <sub>IL</sub>	0	0	0	0	0	1	1	1	07
Device Code	V <sub>IH</sub>	0	0	1	0	0	0	0	0	20

- Notes:
1. V<sub>CC</sub> = 5.0 V ± 10%
  2. A<sub>9</sub> = 12.0 V ± 0.5V
  3. A<sub>1</sub>-A<sub>8</sub>, A<sub>10</sub>-A<sub>18</sub>,  $\overline{CE}$ ,  $\overline{OE}$  = V<sub>IL</sub>
  4. X = Don't Care

### ■ HN27C4001TT/RR RECOMMENDED SCREENING CONDITIONS

Before mounting the HN27C4001TT/RR packages, please make the following screening (baking without bias) shown below:



(RSC.EPROM)