
HN29V25611ABP Series

256M AND type Flash Memory
More than 16,057-sector (271,299,072-bit)

HITACHI

ADE-203-1281 (Z)
Preliminary
Rev. 0.0
Aug. 10, 2001

Description

The Hitachi HN29V25611A Series is a CMOS Flash Memory with AND type multi-level memory cells. It has fully automatic programming and erase capabilities with a single 3.0 V power supply. The functions are controlled by simple external commands. To fit the I/O card applications, the unit of programming and erase is as small as (2048 + 64) bytes. Initial available sectors of HN29V25611A are more than 16,057 (98% of all sector address) and less than 16,384 sectors.

Features

- On-board single power supply (V_{CC}): $V_{CC} = 2.7\text{ V to }3.6\text{ V}$
- Organization
 - AND Flash Memory: (2048 + 64) bytes \times (More than 16,057 sectors)
 - Data register: (2048 + 64) bytes
- Multi-level memory cell
 - 2 bit/per memory cell
- Automatic programming
 - Sector program time: 1.0 ms (typ)
 - System bus free
 - Address, data latch function
 - Internal automatic program verify function
 - Status data polling function
- Automatic erase
 - Single sector erase time: 1.0 ms (typ)
 - System bus free
 - Internal automatic erase verify function
 - Status data polling function

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Preliminary: The specification of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specification.



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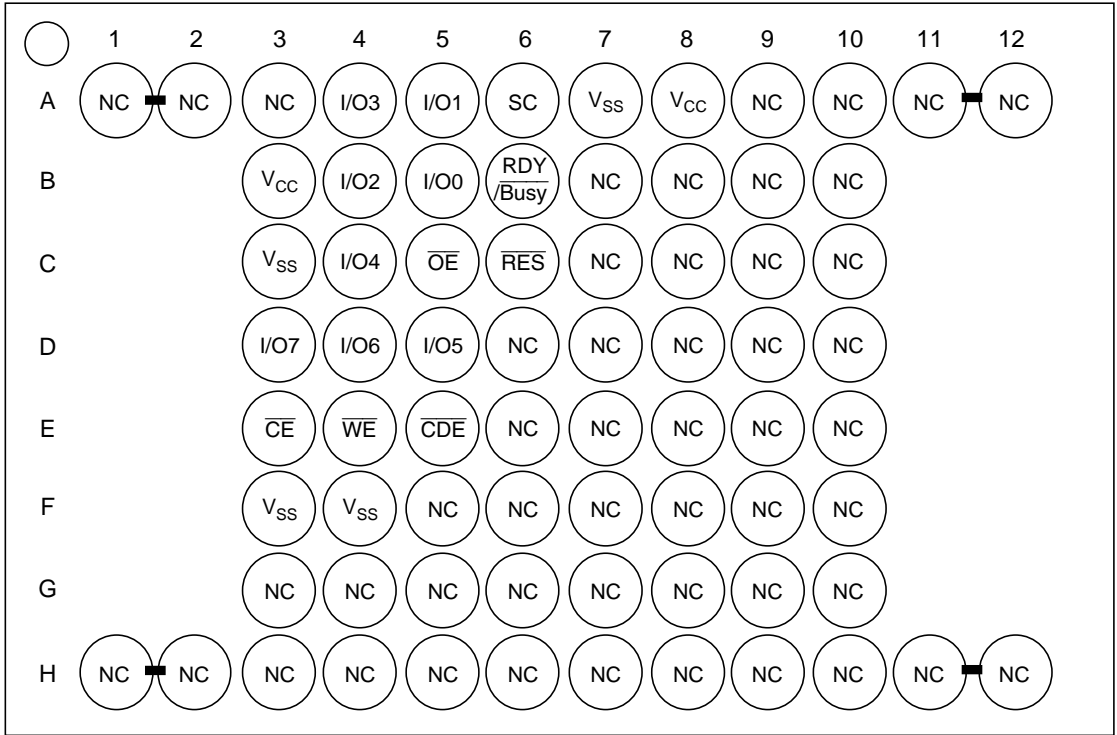
- Erase mode
 - Single sector erase ((2048 + 64) byte unit)
- Fast serial read access time:
 - First access time: 50 μ s (max)
 - Serial access time: 50 ns (max)
- Low power dissipation:
 - I_{CC1} = 2 mA (typ) (Read)
 - I_{CC2} = 20 mA (max) (Read)
 - I_{SB2} = 50 μ A (max) (Standby)
 - I_{CC3}/I_{CC4} = 40 mA (max) (Erase/Program)
 - I_{SB3} = 20 μ A (max) (Deep standby)
- The following architecture is required for data reliability.
 - Error correction: more than 3-bit error correction per each sector read
 - Spare sectors: 1.8% (290 sectors) (min) within usable sectors

Ordering Information

| Type No. | Available sector | Package |
|------------------|--------------------------|---|
| HN29V25611ABP-50 | More than 16,057 sectors | 72-bump 0.8 mm ball pitch CSP (TBP-72A) |

Pin Arrangement

72-bump CSP



(Top view)

Note: 1. Two pins of 4 corners are connected.

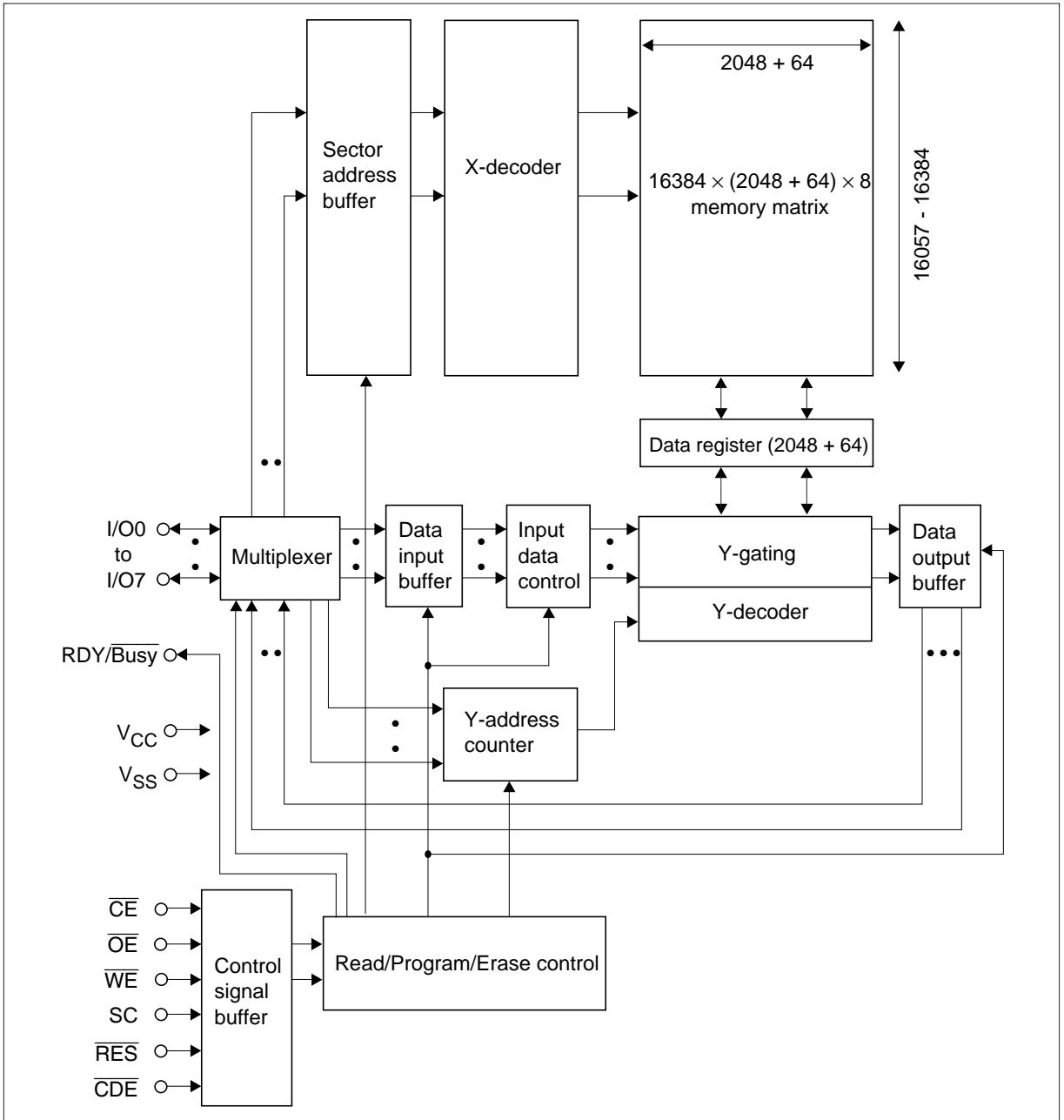
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Pin Description

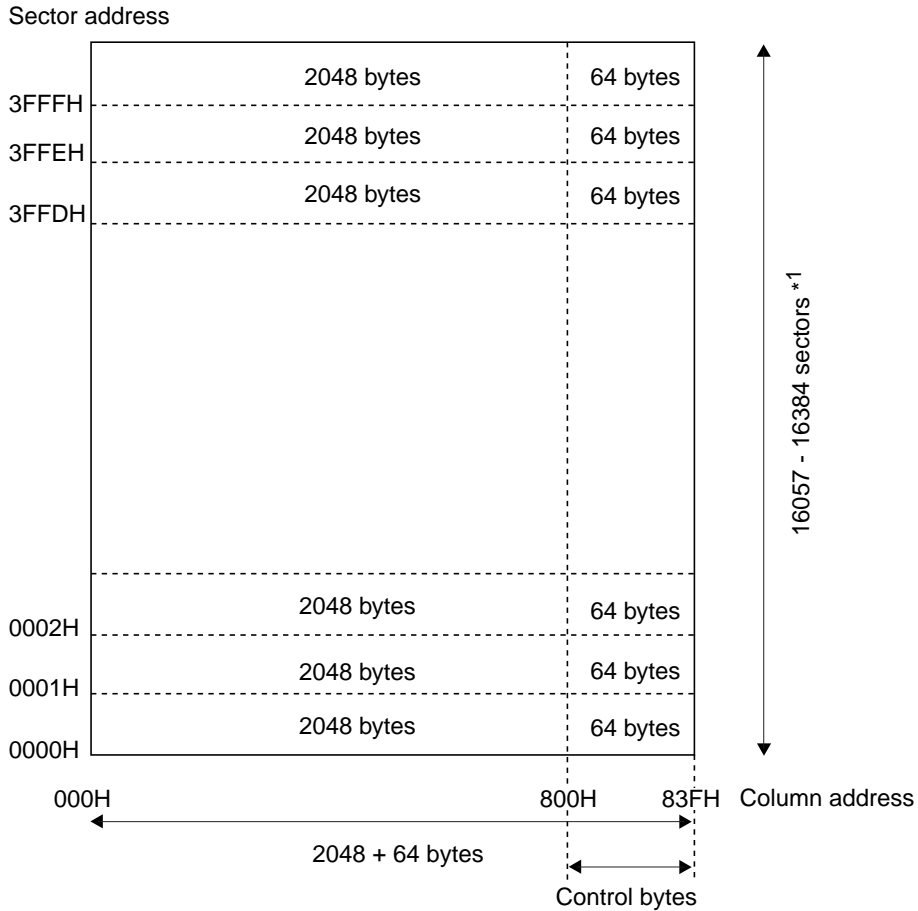
| Pin name | Function |
|------------------------------|---------------------------------|
| I/O0 to I/O7 | Input/output |
| $\overline{\text{CE}}$ | Chip enable |
| $\overline{\text{OE}}$ | Output enable |
| $\overline{\text{WE}}$ | Write enable |
| $\overline{\text{CDE}}$ | Command data enable |
| V_{CC}^{*1} | Power supply |
| V_{SS}^{*1} | Ground |
| $\overline{\text{RDY/Busy}}$ | Ready/ $\overline{\text{Busy}}$ |
| $\overline{\text{RES}}$ | Reset |
| SC | Serial clock |
| NC | No connection |

Note: 1. All V_{CC} and V_{SS} pins should be connected to a common power supply and a ground, respectively.

Block Diagram



Memory Map and Address



| Address | Cycles | I/O0 | I/O1 | I/O2 | I/O3 | I/O4 | I/O5 | I/O6 | I/O7 |
|----------------|----------------------|------|------|------|------|------|------|------|------|
| Sector address | SA (1): First cycle | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 |
| | SA (2): Second cycle | A8 | A9 | A10 | A11 | A12 | A13 | ×*2 | × |
| Column address | CA (1): First cycle | A0 | A1 | A2 | A3 | A4 | A5 | A6 | A7 |
| | CA (2): Second cycle | A8 | A9 | A10 | A11 | × | × | × | × |

- Notes:
- Some failed sectors may exist in the device. The failed sectors can be recognized by reading the sector valid data written in a part of the column address 800 to 83F (The specific address is TBD.). The sector valid data must be read and kept outside of the sector before the sector erase. When the sector is programmed, the sector valid data should be written back to the sector.
 - An × means "Don't care". The pin level can be set to either V_{IL} or V_{IH} , referred to DC characteristics.

Pin Function

\overline{CE} : \overline{CE} is used to select the device. The status returns to the standby at the rising edge of \overline{CE} in the reading operation. However, the status does not return to the standby at the rising edge of \overline{CE} in the busy state in programming and erase operation.

\overline{OE} : Memory data and status register data can be read, when \overline{OE} is V_{IL} .

\overline{WE} : Commands and address are latched at the rising edge of \overline{WE} .

SC: Programming and reading data is latched at the rising edge of SC.

\overline{RES} : \overline{RES} pin must be kept at the V_{ILR} ($V_{SS} \pm 0.2$ V) level when V_{CC} is turned on and off. In this way, data in the memory is protected against unintentional erase and programming. \overline{RES} must be kept at the V_{IHR} ($V_{CC} \pm 0.2$ V) level during any operations such as programming, erase and read.

\overline{CDE} : Commands and data are latched when \overline{CDE} is V_{IL} and address is latched when \overline{CDE} is V_{IH} .

RDY/ \overline{Busy} : The RDY/ \overline{Busy} indicates the program/erase status of the flash memory. The RDY/ \overline{Busy} signal is initially at a high impedance state. It turns to a V_{OL} level after the (40H) command in programming operation or the (B0H) command in erase operation. After the erase or programming operation finishes, the RDY/ \overline{Busy} signal turns back to the high impedance state.

I/O0 to I/O7: The I/O pins are used to input data, address and command, and are used to output memory data and status register data.

Mode Selection

| Mode | \overline{CE} | \overline{OE} | \overline{WE} | SC | \overline{RES} | \overline{CDE} | RDY/ \overline{Busy} *3 | I/O0 to I/O7 |
|------------------------|-----------------|-----------------|-----------------|----------|------------------|------------------|---------------------------|-------------------------|
| Deep standby | \times *4 | \times | \times | \times | V_{ILR} | \times | V_{OH} | High-Z |
| Standby | V_{IH} | \times | \times | \times | V_{IHR} | \times | V_{OH} | High-Z |
| Output disable | V_{IL} | V_{IH} | V_{IH} | \times | V_{IHR} | \times | V_{OH} | High-Z |
| Status register read*1 | V_{IL} | V_{IL} | V_{IH} | \times | V_{IHR} | \times | V_{OH} | Status register outputs |
| Command write*2 | V_{IL} | V_{IH} | V_{IL} | V_{IL} | V_{IHR} | V_{IL} | V_{OH} | Din |

- Notes: 1. Default mode after the power on is the status register read mode (refer to status transition). From I/O0 to I/O7 pins output the status, when $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$ (conventional read operation condition).
2. Refer to the command definition. Data can be read, programmed and erased after commands are written in this mode.
3. The RDY/ \overline{Busy} bus should be pulled up to V_{CC} to maintain the V_{OH} level while the RDY/ \overline{Busy} pin outputs a high impedance.
4. An \times means "Don't care". The pin level can be set to either V_{IL} or V_{IH} referred to DC characteristics.

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Command Definition*^{1, 2}

| Command | | Bus cycles | First bus cycle | | Second bus cycle | | |
|--------------------------|---|-----------------------------|------------------------------|---------|------------------|----------------------|----------------------|
| | | | Operation mode* ³ | Data in | Operation mode | Data in | Data out |
| Read | Serial read (1) (Without CA) | 3 | Write | 00H | Write | SA (1)* ⁴ | |
| | | (With CA) | 3 + 2h* ⁶ | Write | | | 00H |
| | Serial read (2) | 3 | Write | F0H | Write | SA (1)* ⁴ | |
| | Read identifier codes | 1 | Write | 90H | Read | ID* ^{8, 9} | |
| | Data recovery read | 1 | Write | 01H | Read | Recovery data | |
| Auto erase | Single sector | 4 | Write | 20H | Write | SA (1)* ⁴ | |
| Auto program | Program (1) | (Without CA* ⁷) | 4 | Write | 10H | Write | SA (1)* ⁴ |
| | | (With CA* ⁷) | 4 + 2h* ⁶ | Write | 10H | Write | SA (1)* ⁴ |
| | Program (2)* ¹⁰ | 4 | Write | 1FH | Write | SA (1)* ⁴ | |
| | Program (3) (Control bytes)* ⁷ | 4 | Write | 0FH | Write | SA (1)* ⁴ | |
| | Program (4) | (Without CA* ⁷) | 4 | Write | 11H | Write | SA (1)* ⁴ |
| (With CA* ⁷) | | 4 + 2h* ⁶ | Write | 11H | Write | SA (1)* ⁴ | |
| Reset | | 1 | Write | FFH | | | |
| Clear status register | | 1 | Write | 50H | | | |
| Data recovery write | | 4 | Write | 12H | Write | SA (1)* ⁴ | |

| Command | | Bus cycles | Third bus cycle | | Fourth bus cycle | |
|-----------------------|---|----------------------|----------------------|----------------------|------------------|------------------------|
| | | | Operation mode | Data in | Operation mode | Data in |
| Read | Serial read (1) (Without CA) | 3 | Write | SA (2) ^{*4} | | |
| | | 3 + 2h ^{*6} | Write | SA (2) ^{*4} | Write | CA (1) ^{*5} |
| | Serial read (2) | 3 | Write | SA (2) ^{*4} | | |
| | Read identifier codes | 1 | | | | |
| | Data recovery read | 1 | | | | |
| Auto erase | Single sector | 4 | Write | SA (2) ^{*4} | Write | B0H ^{*11} |
| Auto program | Program (1) (Without CA ^{*7}) | 4 | Write | SA (2) ^{*4} | Write | 40H ^{*11, 12} |
| | | 4 + 2h ^{*6} | Write | SA (2) ^{*4} | Write | CA (1) |
| | Program (2) ^{*10} | 4 | Write | SA (2) ^{*4} | Write | 40H ^{*11, 12} |
| | Program (3) (Control bytes) ^{*7} | 4 | Write | SA (2) ^{*4} | Write | 40H ^{*11, 12} |
| | Program (4) (Without CA ^{*7}) | 4 | Write | SA (2) ^{*4} | Write | 40H ^{*11, 12} |
| 4 + 2h ^{*6} | | Write | SA (2) ^{*4} | Write | CA (1) | |
| Reset | | 1 | | | | |
| Clear status register | | 1 | | | | |
| Data recovery write | | 4 | Write | SA (2) ^{*4} | Write | 40H ^{*11, 12} |

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| Command | | Bus cycles | Fifth bus cycle | | Sixth bus cycle | | |
|-----------------------|---|--------------------------|----------------------|---------|----------------------|---------|------------------------|
| | | | Operation mode | Data in | Operation mode | Data in | |
| Read | Serial read (1) (Without CA) | 3 | | | | | |
| | | (With CA) | 3 + 2h* ⁶ | Write | CA (2)* ⁵ | | |
| | Serial read (2) | 3 | | | | | |
| | Read identifier codes | 1 | | | | | |
| | Data recovery read | 1 | | | | | |
| Auto erase | Single sector | 4 | | | | | |
| Auto program | Program (1) (Without CA* ⁷) | 4 | | | | | |
| | | (With CA* ⁷) | 4 + 2h* ⁶ | Write | CA (2)* ⁵ | Write | 40H* ^{11, 12} |
| | Program (2)* ¹⁰ | 4 | | | | | |
| | Program (3) (Control bytes)* ⁷ | 4 | | | | | |
| | Program (4) (Without CA* ⁷) | 4 | | | | | |
| | | (With CA* ⁷) | 4 + 2h* ⁶ | Write | CA (2) | Write | 40H* ^{11, 12} |
| Reset | | 1 | | | | | |
| Clear status register | | 1 | | | | | |
| Data recovery write | | 4 | | | | | |

- Notes:
1. Commands and sector address are latched at rising edge of \overline{WE} pulses. Program data is latched at rising edge of SC pulses.
 2. The chip is in the read status register mode when \overline{RES} is set to V_{IHR} first time after the power up.
 3. Refer to the command read and write mode in mode selection.
 4. SA (1) = Sector address (A0 to A7), SA (2) = Sector address (A8 to A13).
 5. CA (1) = Column address (A0 to A7), CA (2) = Column address (A8 to A11).
($0 \leq A11$ to $A0 \leq 83FH$)
 6. The variable h is the input number of times of set of CA (1) and CA (2) ($1 \leq h \leq 2048 + 64$).
Set of CA (1) and CA (2) can be input without limitation.
 7. By using program (1) and (3), data can additionally be programmed maximum 15 times for each sector before erase.
 8. ID = Identifier code; Manufacturer code (07H), Device code (9AH).
 9. The manufacturer identifier code is output when \overline{CDE} is low and the device identifier code is output when \overline{CDE} is high.
 10. Before program (2) operations, data in the programmed sector must be erased.
 11. No commands can be written during auto program and erase (when the RDY/\overline{Busy} pin outputs a V_{OL}).
 12. The fourth or sixth cycle of the auto program comes after the program data input is complete.

Mode Description

Read

Serial Read (1): Memory data D0 to D2111 in the sector of address SA is sequentially read. Output data is not valid after the number of the SC pulse exceeds 2112. When CA is input, memory data D (m) to D (m + j) in the sector of address SA is sequentially read. Then output data is not valid after the number of the SC pulse exceeds (2112 to m). The mode turns back to the standby mode at any time when \overline{CE} is V_{IH} .

Serial Read (2): Memory data D2048 to D2111 in the sector of address SA is sequentially read. Output data is not valid after the number of the SC pulse exceeds 64. The mode turns back to the standby mode at any time when \overline{CE} is V_{IH} .

Automatic Erase

Single Sector Erase: Memory data D0 to D2111 in the sector of address SA is erased automatically by internal control circuits. After the sector erase starts, the erasure completion can be checked through the RDY/\overline{Busy} signal and status data polling. All the bits in the sector are "1" after the erase. The sector valid data stored in a part of memory data D2048 to D2111 must be read and kept outside of the sector before the sector erase.

Automatic Program

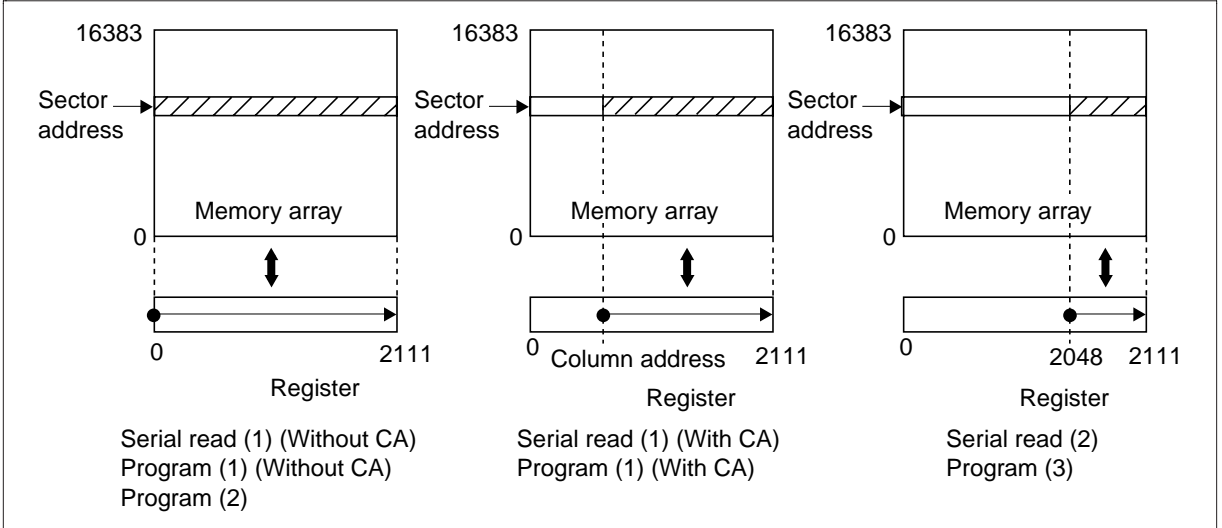
Program (1): Program data PD0 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. When CA is input, program data PD (m) to PD (m + j) is programmed from CA into the sector of address SA automatically by internal control circuits. By using program (1), data can additionally be programmed 15 times for each sector before the following erase. When the column is programmed, the data of the column must be [FF]. After the programming starts, the program completion can be checked through the RDY/\overline{Busy} signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed. The sector valid data should be included in the program data PD2048 to PD2111.

Program (2): Program data PD0 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. After the programming starts, the program completion can be checked through the RDY/\overline{Busy} signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed. The sector must be erased before programming. The sector valid data should be included in the program data PD2048 to PD2111.

Program (3): Program data PD2048 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. By using program (3), data can additionally be programmed 15 times for each sector before the following erase. When the column is programmed, the data of the column must be [FF]. After the programming starts, the program completion can be checked through the RDY/\overline{Busy} signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed.

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Program (4): Program data PD0 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. When CA is input, program data PD (m) to PD (m + j) is programmed from CA into the sector of address SA automatically by internal control circuits. By using program (4), data can be rewritten for each sector before the following erase. So the column data before programming operation are either "1" or "0". In this mode, E/W number of times must be counted whenever program (4) execute. After the programming starts, the program completion can be checked through the RDY/Busy signal and status data polling. The sector valid data should be included in the program data PD2048 to PD2111.



Status Register Read

The status returns to the status register read mode from standby mode, when \overline{CE} and \overline{OE} is V_{IL} . In the status register read mode, I/O pins output the same operation status as in the status data polling defined in the function description.

Identifier Read

The manufacturer and device identifier code can be read in the identifier read mode. The manufacturer and device identifier code is selected with $\overline{CDE} V_{IL}$ and V_{IH} , respectively.

Data Recovery Read

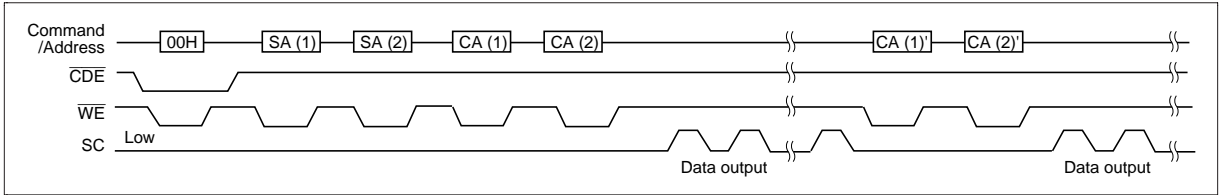
When the programming was an error, the program data can be read by using data recovery read. When an additional programming was an error, the data compounded of the program data and the origin data in the sector address SA can be read. Output data are not valid after the number of SA pulse exceeds 2112. The mode turns back to the standby mode at any time when \overline{CE} is V_{IH} . The read data are invalid when addresses are latched at a rising edge of \overline{WE} pulse after the data recovery read command is written.

Data Recovery Write

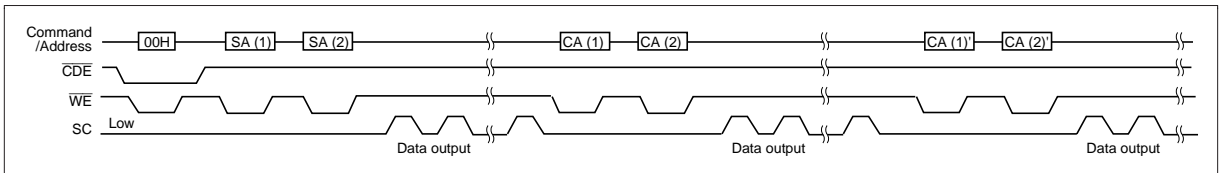
When the programming into a sector of address SA was an error, the program data can be rewritten automatically by internal control circuit into the other selected sector of address SA'. Since the data recovery write mode is internally Program (4) mode, rewritten sector of address SA' needs no sector erase before rewrite. After the data recovery write mode starts, the program completion can be checked through the RDY/Busy signal and the status data polling.

Command/Address/Data Input Sequence

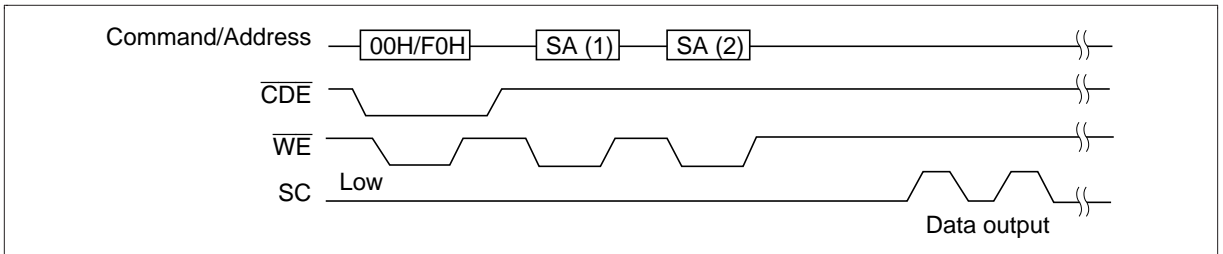
Serial Read (1) (With CA before SC)



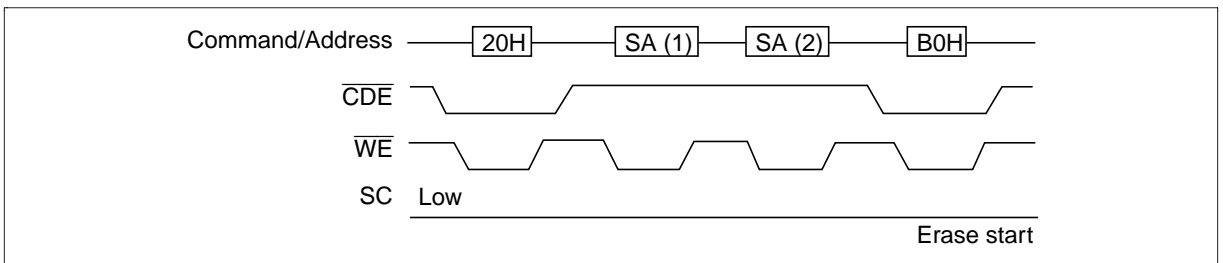
Serial Read (1) (With CA after SC)



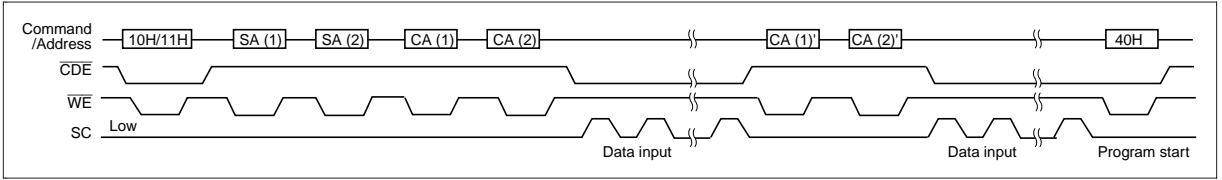
Serial Read (1) (Without CA), (2)



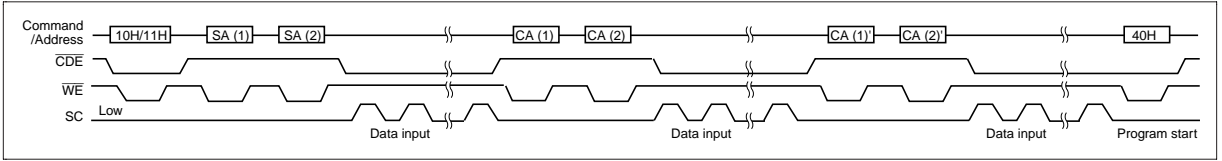
Single Sector Erase



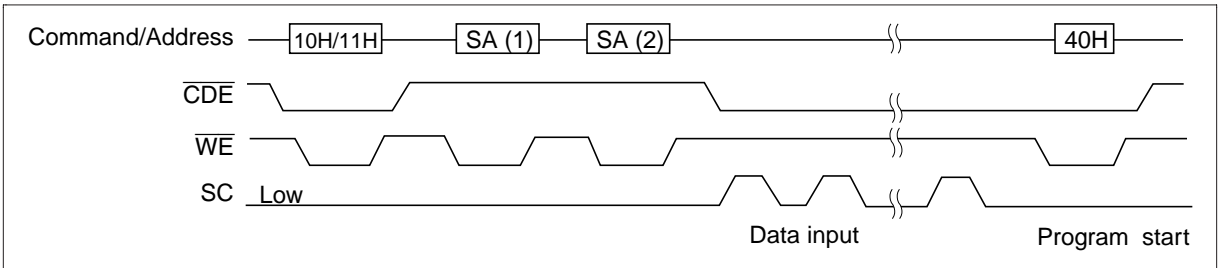
Program (1), (4) (With CA before SC)



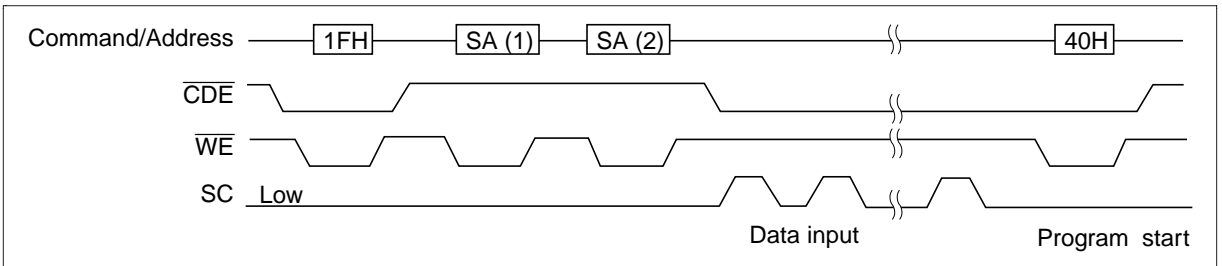
Program (1), (4) (With CA after SC)



Program (1), (4) (Without CA)

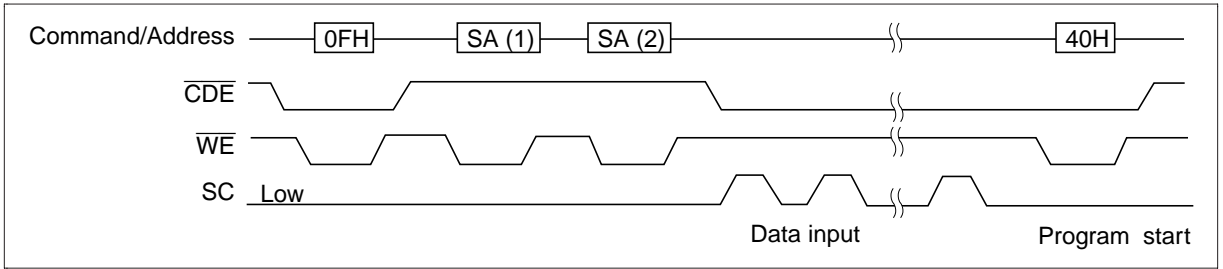


Program (2)

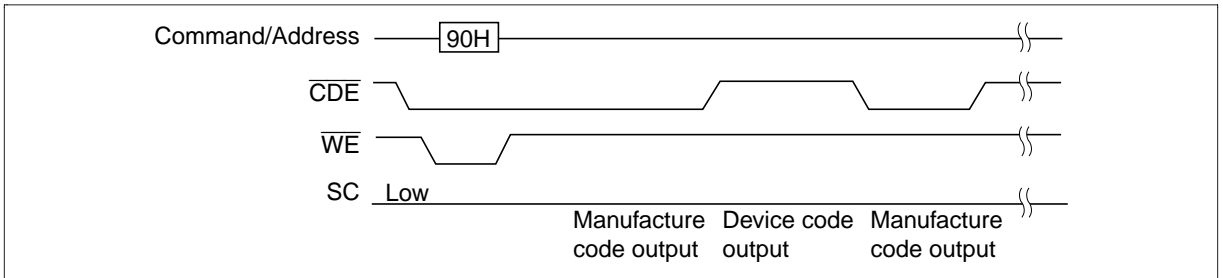


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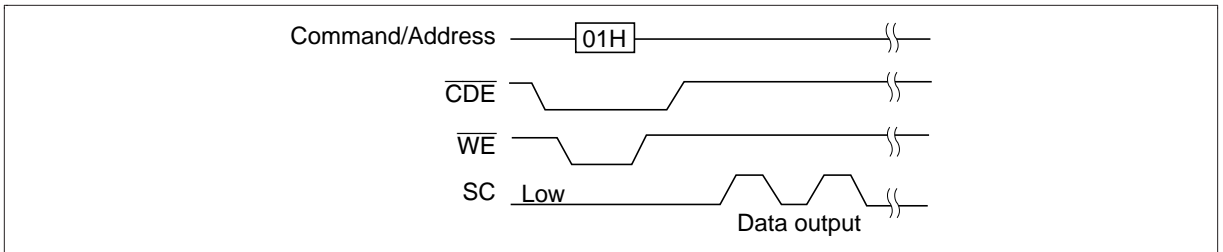
Program (3)



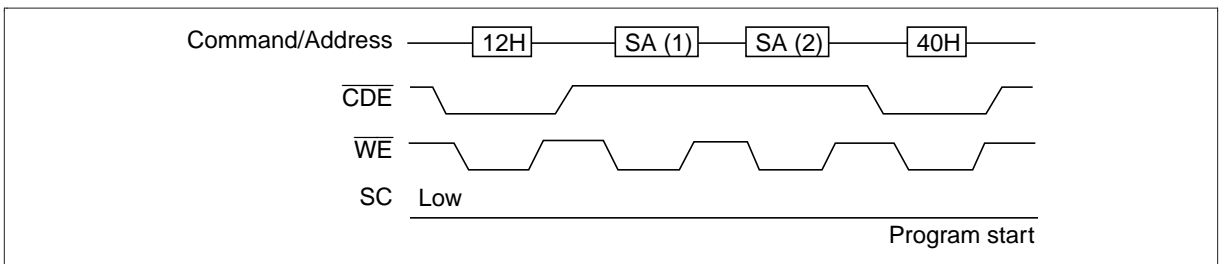
ID Read Mode



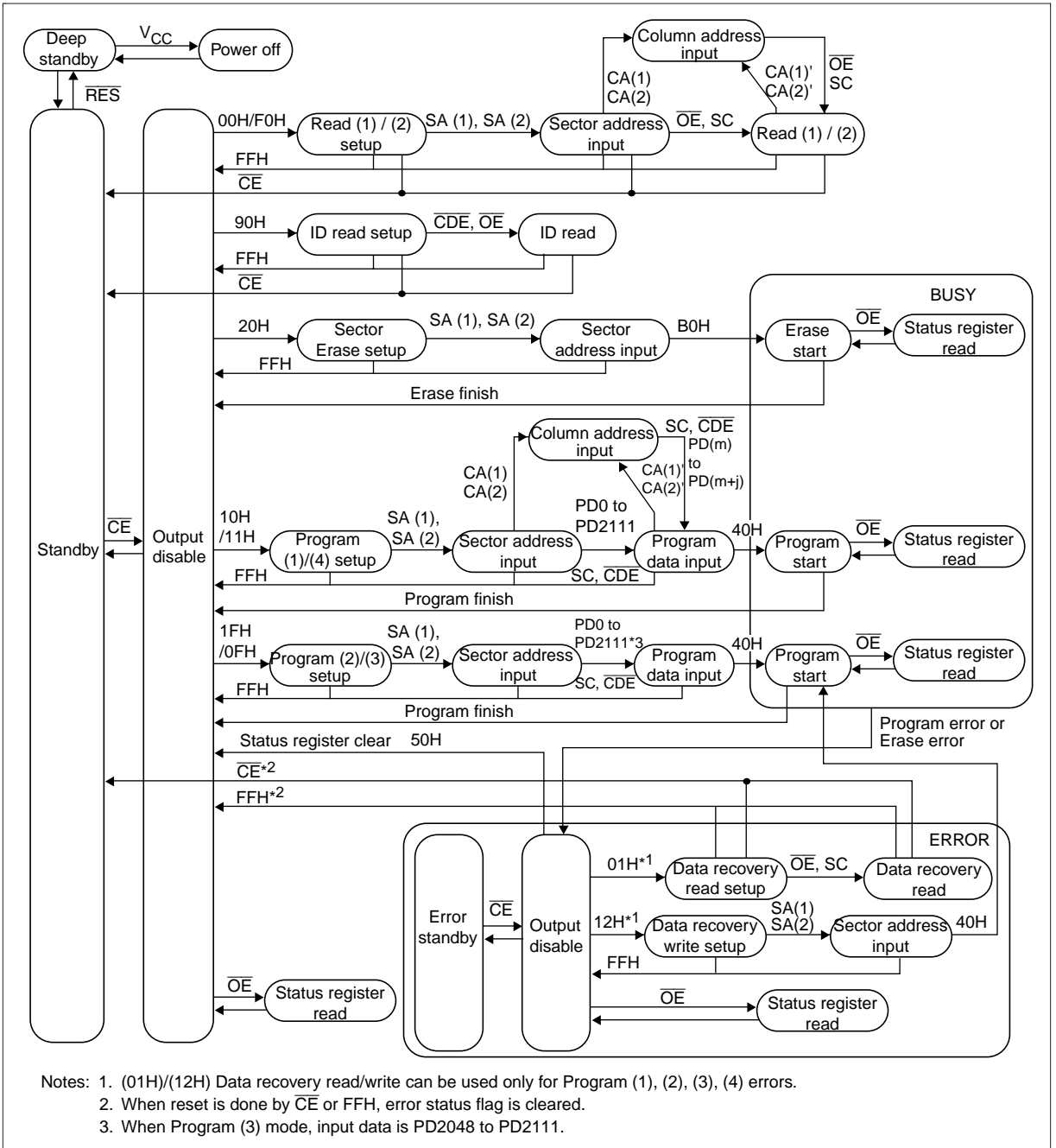
Data Recovery Read Mode



Data Recovery Write Mode



Status Transition



HN29V25611ABP Series

Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit | Notes |
|--------------------------------|------------------------------------|--------------|------|-------|
| V _{CC} voltage | V _{CC} | -0.6 to +4.6 | V | 1 |
| V _{SS} voltage | V _{SS} | 0 | V | |
| All input and output voltages | V _{in} , V _{out} | -0.6 to +4.6 | V | 1, 2 |
| Operating temperature range | T _{opr} | 0 to +70 | °C | |
| Storage temperature range | T _{stg} | -65 to +125 | °C | 3 |
| Storage temperature under bias | T _{bias} | -10 to +80 | °C | |

Notes: 1. Relative to V_{SS}.

2. V_{in}, V_{out} = -2.0 V for pulse width ≤ 20 ns.

3. Device storage temperature range before programming.

Capacitance (T_a = 25°C, f = 1 MHz)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|--------------------|------------------|-----|-----|-----|------|------------------------|
| Input capacitance | C _{in} | — | — | 6 | pF | V _{in} = 0 V |
| Output capacitance | C _{out} | — | — | 12 | pF | V _{out} = 0 V |

DC Characteristics ($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $T_a = 0\text{ to }+70^\circ\text{C}$)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|---------------------------------------|-----------|----------------|-----|---------------------|---------------|---|
| Input leakage current | I_{LI} | — | — | 2 | μA | $V_{in} = V_{SS}\text{ to }V_{CC}$ |
| Output leakage current | I_{LO} | — | — | 2 | μA | $V_{out} = V_{SS}\text{ to }V_{CC}$ |
| Standby V_{CC} current | I_{SB1} | — | 0.3 | 1 | mA | $\overline{CE} = V_{IH}$ |
| | I_{SB2} | — | 30 | 50 | μA | $\overline{CE} = V_{CC} \pm 0.2\text{ V}$, $\overline{RES} = V_{CC} \pm 0.2\text{ V}$ |
| Deep standby V_{CC} current | I_{SB3} | — | 1 | 20 | μA | $\overline{RES} = V_{SS} \pm 0.2\text{ V}$ |
| Operating V_{CC} current | I_{CC1} | — | 2 | 20 | mA | $I_{out} = 0\text{ mA}$, $f = 0.2\text{ MHz}$ |
| | I_{CC2} | — | 10 | 20 | mA | $I_{out} = 0\text{ mA}$, $f = 20\text{ MHz}$ |
| Operating V_{CC} current (Program) | I_{CC3} | — | 20 | 40 | mA | In programming |
| Operating V_{CC} current (Erase) | I_{CC4} | — | 20 | 40 | mA | In erase |
| Input voltage | V_{IL} | $-0.3^{*1,2}$ | — | 0.8 | V | |
| | V_{IH} | 2.0 | — | $V_{CC} + 0.3^{*3}$ | V | |
| Input voltage (\overline{RES} pin) | V_{ILR} | -0.2 | — | 0.2 | V | |
| | V_{IHR} | $V_{CC} - 0.2$ | — | $V_{CC} + 0.2$ | V | |
| Output voltage | V_{OL} | — | — | 0.4 | V | $I_{OL} = 2\text{ mA}$ |
| | V_{OH} | 2.4 | — | — | V | $I_{OH} = -2\text{ mA}$ |

- Notes: 1. V_{IL} min = -1.0 V for pulse width $\leq 50\text{ ns}$ in the read operation. V_{IL} min = -2.0 V for pulse width $\leq 20\text{ ns}$ in the read operation.
2. V_{IL} min = -0.6 V for pulse width $\leq 20\text{ ns}$ in the erase/data programming operation.
3. V_{IH} max = $V_{CC} + 1.5\text{ V}$ for pulse width $\leq 20\text{ ns}$. If V_{IH} is over the specified maximum value, the operations are not guaranteed.

AC Characteristics ($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $T_a = 0\text{ to }+70^\circ\text{C}$)

Test Conditions

- Input pulse levels: 0.4 V/2.4 V
- Input pulse levels for \overline{RES} : 0.2 V/ $V_{CC} - 0.2\text{ V}$
- Input rise and fall time: $\leq 5\text{ ns}$
- Output load: 1 TTL gate + 100 pF (Including scope and jig.)
- Reference levels for measuring timing: 0.8 V, 1.8 V

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Power on and off, Serial Read Mode

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | Notes |
|--|------------|-----|-----|-----|---------|--|-------|
| Write cycle time | t_{CWC} | 120 | — | — | ns | | |
| Serial clock cycle time | t_{SCC} | 50 | — | — | ns | | |
| \overline{CE} setup time | t_{CES} | 0 | — | — | ns | | |
| \overline{CE} hold time | t_{CEH} | 0 | — | — | ns | | |
| Write pulse time | t_{WP} | 60 | — | — | ns | $\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$ | |
| Write pulse high time | t_{WPH} | 40 | — | — | ns | | |
| Address setup time | t_{AS} | 50 | — | — | ns | | |
| Address hold time | t_{AH} | 10 | — | — | ns | | |
| Data setup time | t_{DS} | 50 | — | — | ns | | |
| Data hold time | t_{DH} | 10 | — | — | ns | | |
| SC to output delay | t_{SAC} | — | — | 50 | ns | $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ | |
| \overline{OE} setup time for SC | t_{OES} | 0 | — | — | ns | | |
| \overline{OE} low to output low-Z | t_{OEL} | 0 | — | 40 | ns | | |
| \overline{OE} setup time before read | t_{OER} | 100 | — | — | ns | | |
| \overline{OE} setup time before command write | t_{OEWS} | 0 | — | — | ns | | |
| SC to output hold | t_{SH} | 15 | — | — | ns | $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ | |
| \overline{OE} high to output float | t_{DF} | — | — | 40 | ns | $\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$ | 1 |
| \overline{WE} to SC delay time | t_{WSD} | 50 | — | — | μs | | 2 |
| \overline{RES} to \overline{CE} setup time | t_{RP} | 0.3 | — | — | ms | | |
| SC to \overline{OE} hold time | t_{SOH} | 50 | — | — | ns | | |
| SC pulse width | t_{SP} | 20 | — | — | ns | | |
| SC pulse low time | t_{SPL} | 20 | — | — | ns | | |
| SC setup time for \overline{CE} | t_{SCS} | 0 | — | — | ns | | |
| \overline{CDE} setup time for \overline{WE} | t_{CDS} | 0 | — | — | ns | | |
| \overline{CDE} hold time for \overline{WE} | t_{CDH} | 20 | — | — | ns | | |
| V_{CC} setup time for \overline{RES} | t_{VRS} | 1 | — | — | μs | $\overline{CE} = V_{IH}$ | |
| \overline{RES} to V_{CC} hold time | t_{VRH} | 1 | — | — | μs | $\overline{CE} = V_{IH}$ | |
| \overline{CE} setup time for \overline{RES} | t_{CESR} | 1 | — | — | μs | | |
| RDY/ \overline{Busy} undefined for V_{CC} off | t_{DFP} | 0 | — | — | ns | | |
| \overline{RES} high to device ready | t_{BSY} | — | — | 0.3 | ms | | |
| \overline{CE} pulse high time | t_{CPH} | 200 | — | — | ns | | |
| $\overline{CE}, \overline{WE}$ setup time for \overline{RES} | t_{CWRS} | 0 | — | — | ns | | |
| \overline{RES} to $\overline{CE}, \overline{WE}$ hold time | t_{CWRH} | 0 | — | — | ns | | |

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | Notes |
|---|------------|-----|-----|-----|---------|-----------------|-------|
| SC setup for \overline{WE} | t_{SW} | 50 | — | — | ns | | |
| \overline{CE} hold time for \overline{OE} | t_{COH} | 0 | — | — | ns | | |
| SA (2) to CA (2) delay time | t_{SCD} | — | — | 30 | μ s | | |
| RDY/ \overline{Busy} setup for SC | t_{RS} | 200 | — | — | ns | | |
| Time to device busy | t_{DB} | — | — | 150 | ns | | |
| Busy time on read mode | t_{RBSY} | — | 45 | — | μ s | | |

Notes: 1. t_{DF} is a time after which the I/O pins become open.

2. t_{WSD} (min) is specified as a reference point only for SC, if t_{WSD} is greater than the specified t_{WSD} (min) limit, then access time is controlled exclusively by t_{SAC} .

HN29V25611ABP Series

Program, Erase and Erase Verify

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | Note |
|--|------------|-----|-----|------|---------|---------------------------|------|
| Write cycle time | t_{CWC} | 120 | — | — | ns | | |
| Serial clock cycle time | t_{SCC} | 50 | — | — | ns | | |
| \overline{CE} setup time | t_{CES} | 0 | — | — | ns | | |
| \overline{CE} hold time | t_{CEH} | 0 | — | — | ns | | |
| Write pulse time | t_{WP} | 60 | — | — | ns | | |
| Write pulse high time | t_{WPH} | 40 | — | — | ns | | |
| Address setup time | t_{AS} | 50 | — | — | ns | | |
| Address hold time | t_{AH} | 10 | — | — | ns | | |
| Data setup time | t_{DS} | 50 | — | — | ns | | |
| Data hold time | t_{DH} | 10 | — | — | ns | | |
| \overline{OE} setup time before command write | t_{OEWS} | 0 | — | — | ns | | |
| \overline{OE} setup time before status polling | t_{OEPS} | 40 | — | — | ns | | |
| \overline{OE} setup time before read | t_{OER} | 100 | — | — | ns | | |
| Time to device busy | t_{DB} | — | — | 150 | ns | | |
| Auto erase time | t_{ASE} | — | 1.0 | 10.0 | ms | | |
| Auto program time Program(1), (3) | t_{ASP} | — | 1.5 | 20.0 | ms | | |
| Program(2) | t_{ASP} | — | 1.0 | 20.0 | ms | | |
| Program(4), Data recovery write | t_{ASP} | — | 2.0 | 30.0 | ms | | |
| \overline{WE} to SC delay time | t_{WSD} | 50 | — | — | μ s | | |
| \overline{CE} pulse high time | t_{CPH} | 200 | — | — | ns | | |
| SC pulse width | t_{SP} | 20 | — | — | ns | | |
| SC pulse low time | t_{SPL} | 20 | — | — | ns | | |
| Data setup time for SC | t_{SDS} | 0 | — | — | ns | | |
| Data hold time for SC | t_{SDH} | 30 | — | — | ns | $\overline{CDE} = V_{IL}$ | |
| SC setup for \overline{WE} | t_{SW} | 50 | — | — | ns | | |
| SC setup for \overline{CE} | t_{SCS} | 0 | — | — | ns | | |
| SC hold time for \overline{WE} | t_{SCHW} | 20 | — | — | ns | | |

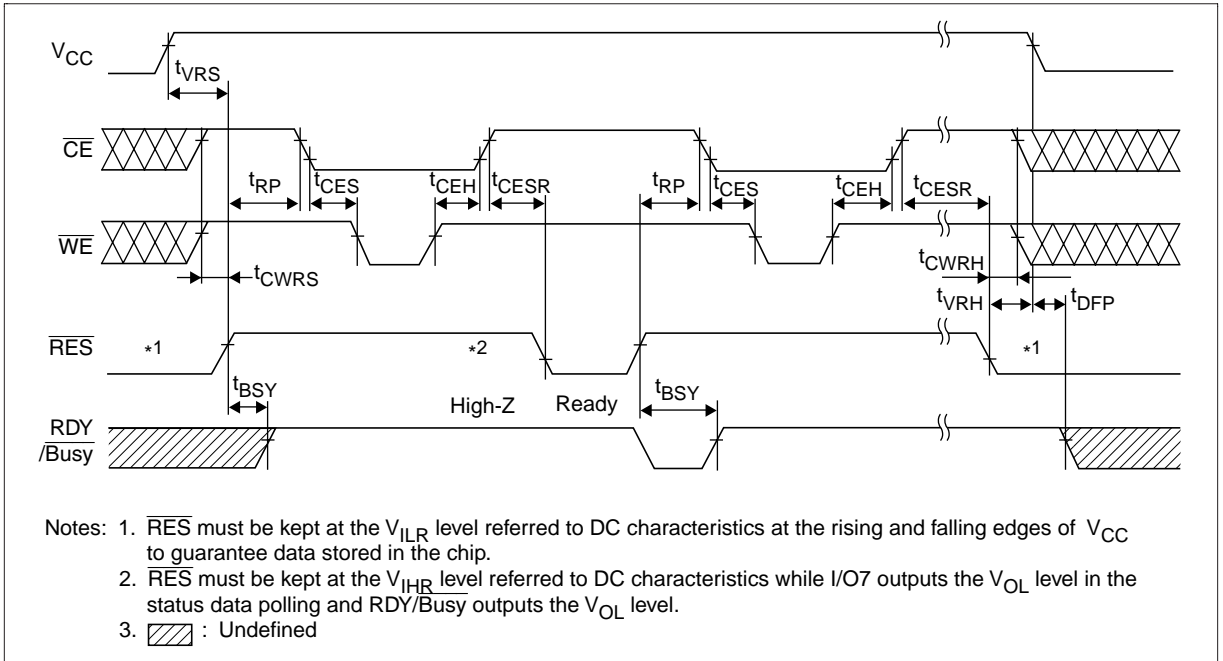
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| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | Note |
|---|-------------------|-----|-----|-----|---------------|-----------------|------|
| $\overline{\text{CE}}$ to output delay | t_{CE} | — | — | 120 | ns | | |
| $\overline{\text{OE}}$ to output delay | t_{OE} | — | — | 60 | ns | | |
| $\overline{\text{OE}}$ high to output float | t_{DF} | — | — | 40 | ns | | 1 |
| $\overline{\text{RES}}$ to $\overline{\text{CE}}$ setup time | t_{RP} | 0.3 | — | — | ms | | |
| $\overline{\text{CDE}}$ setup time for $\overline{\text{WE}}$ | t_{CDS} | 0 | — | — | ns | | |
| $\overline{\text{CDE}}$ hold time for $\overline{\text{WE}}$ | t_{CDH} | 20 | — | — | ns | | |
| $\overline{\text{CDE}}$ setup time for SC | t_{CDSS} | 1.5 | — | — | μs | | |
| $\overline{\text{CDE}}$ hold time for SC | t_{CDSH} | 30 | — | — | ns | | |
| Next cycle ready time | t_{RDY} | 0 | — | — | ns | | |
| $\overline{\text{CDE}}$ to $\overline{\text{OE}}$ hold time | t_{CDOH} | 50 | — | — | ns | | |
| $\overline{\text{CDE}}$ to output delay | t_{CDAC} | — | — | 50 | ns | | |
| $\overline{\text{CDE}}$ to output invalid | t_{CDF} | — | — | 100 | ns | | |
| $\overline{\text{CE}}$ hold time for $\overline{\text{OE}}$ | t_{COH} | 0 | — | — | ns | | |
| $\overline{\text{OE}}$ setup time for SC | t_{OES} | 0 | — | — | ns | | |
| $\overline{\text{OE}}$ low to output low-Z | t_{OEL} | 0 | — | 40 | ns | | |
| SC to output delay | t_{SAC} | — | — | 50 | ns | | |
| SC to output hold | t_{SH} | 15 | — | — | ns | | |
| RDY/Busy setup for SC | t_{RS} | 200 | — | — | ns | | |
| Busy time on read mode | t_{RBSY} | — | 45 | — | μs | | |

Note: 1. t_{DF} is a time after which the I/O pins become open.

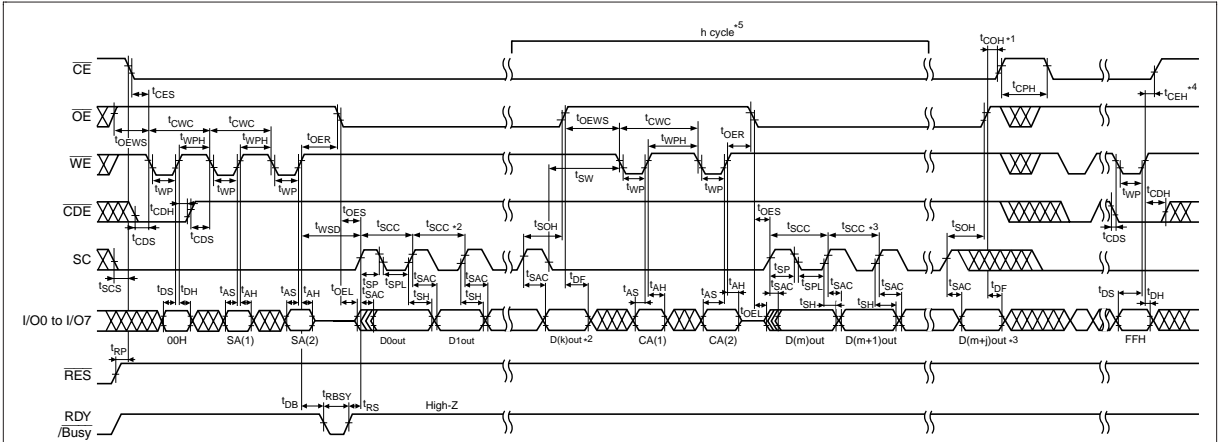
Timing Waveforms

Power on and off Sequence



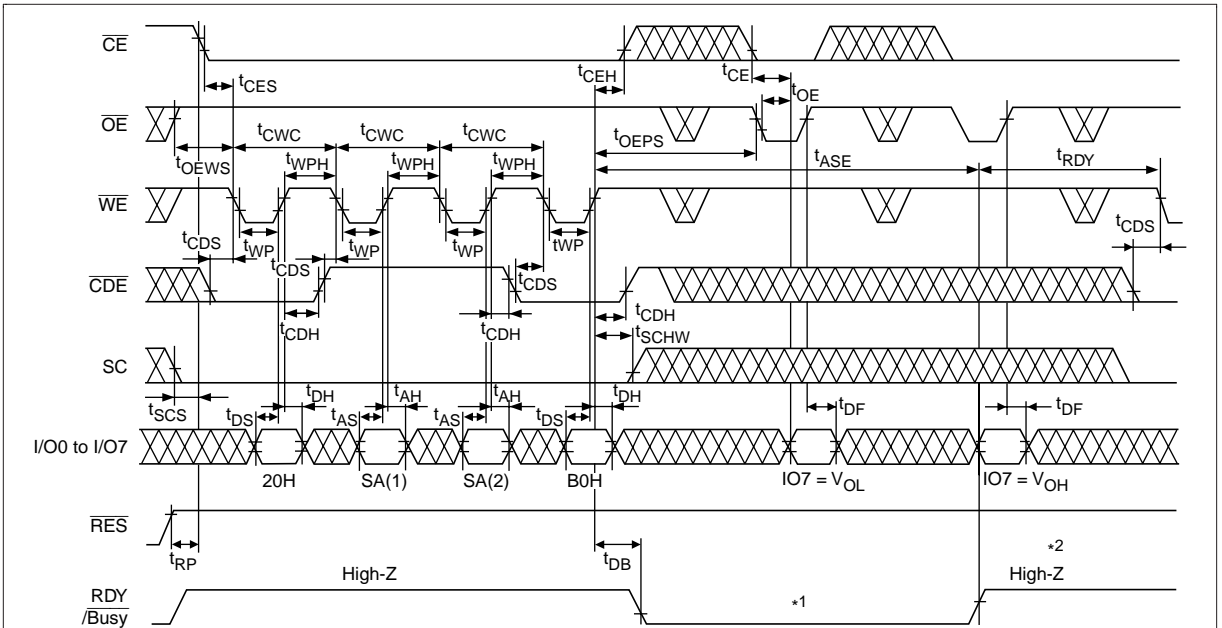
HN29V25611ABP Series

Serial Read (1) with CA after SC Timing Waveform



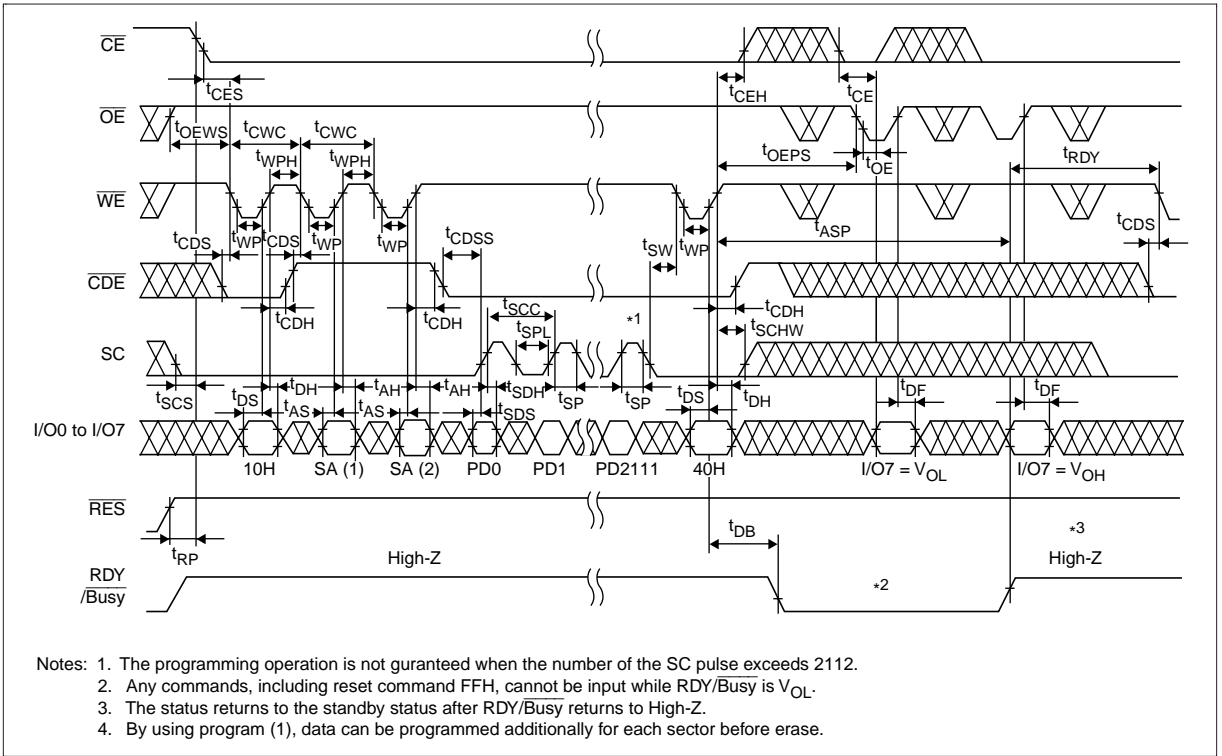
- Notes:
1. The status returns to the Standby at the rising edge of \overline{CE} .
 2. Output data is not valid after the number of the SC pulse exceeds 2112. ($0 \leq k \leq 2111$)
 3. Output data is not valid after the number of the SC pulse exceeds $(2112-m)$. ($j \leq 2111-m, 0 \leq m \leq 2111$)
 4. After any commands are written, the status can return to the standby after the command FFH is input and \overline{CE} turns to the V_{IH} level.
 5. This interval can be repeated h cycle. ($1 \leq h \leq 2048 + 64$)

Erase and Status Data Polling Timing Waveform (Sector Erase)

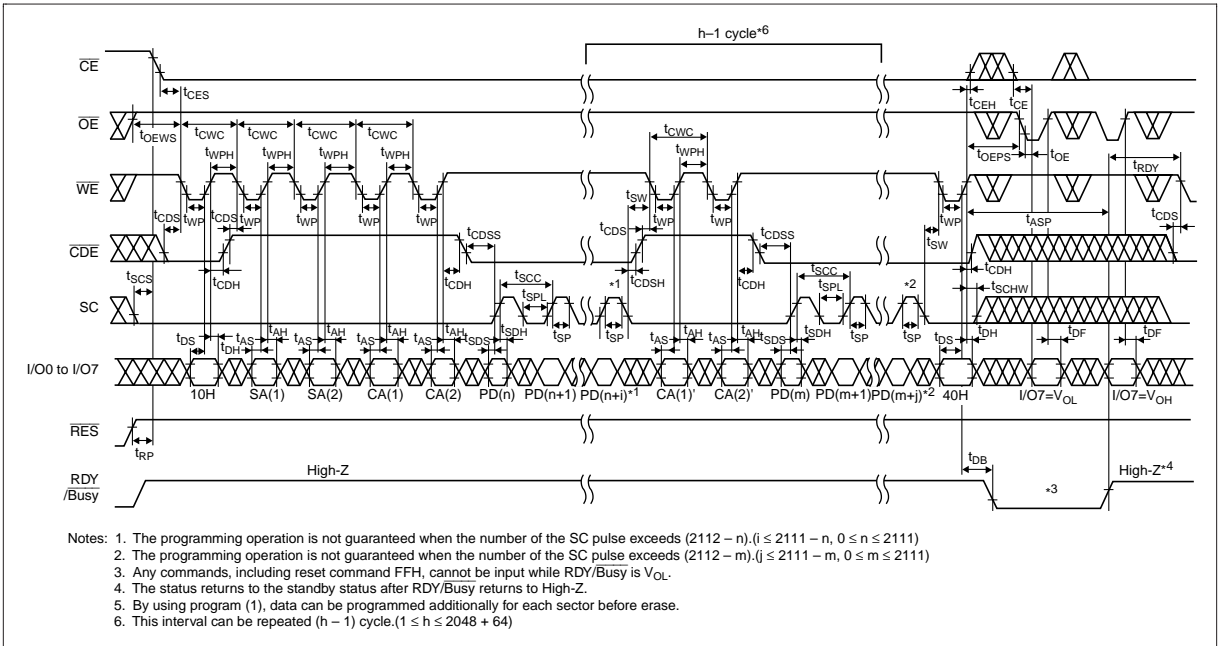


- Notes:
1. Any commands, including reset command FFH, cannot be input while RDY/Busy outputs a V_{OL} .
 2. The status returns to the standby status after RDY/Busy returns to High-Z.

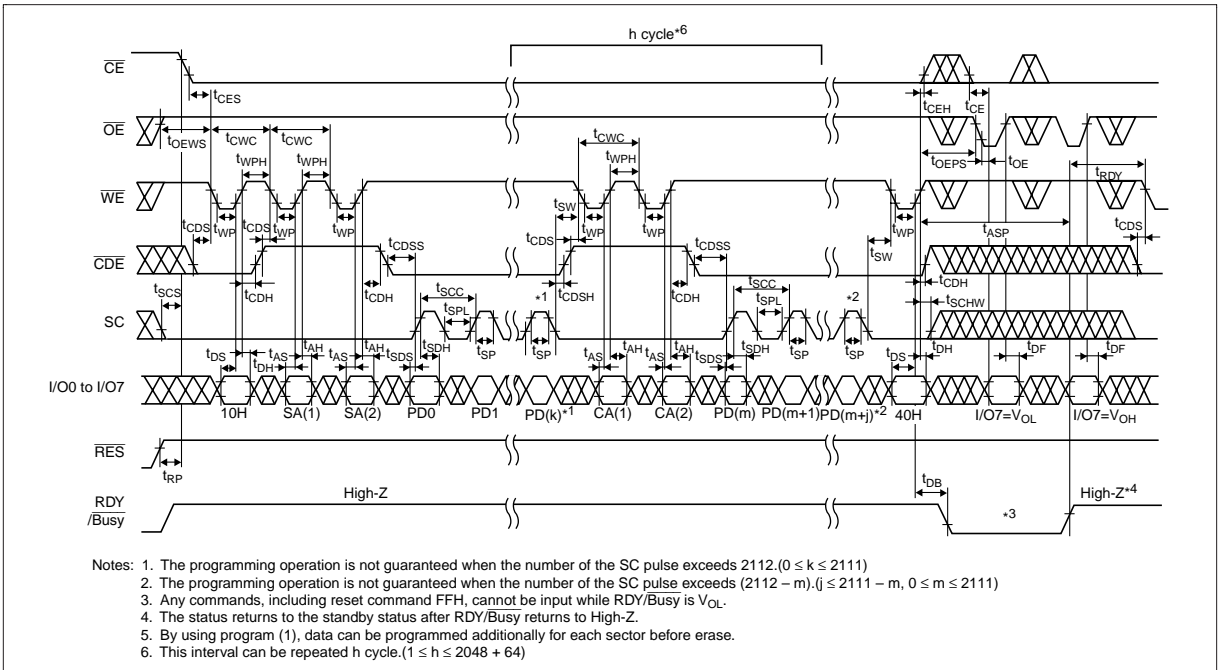
Program (1) and Status Data Polling Timing Waveform



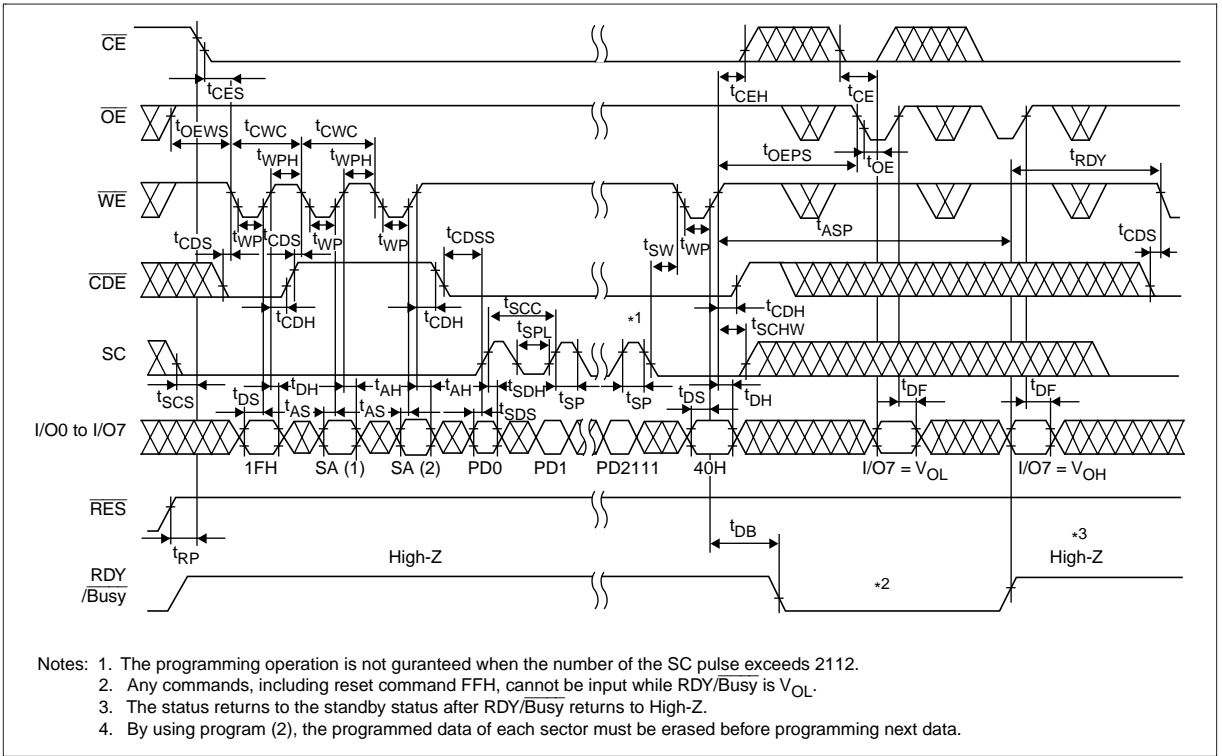
Program (1) with CA before SC and Status Data Polling Timing Waveform



Program (1) with CA after SC and Status Data Polling Timing Waveform

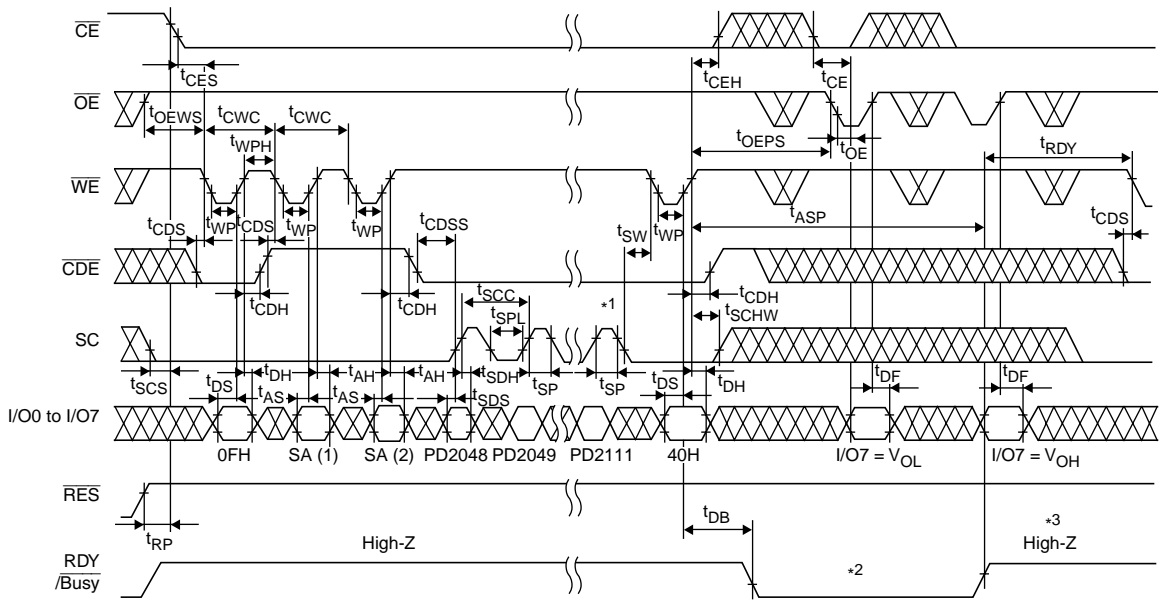


Program (2) and Status Data Polling Timing Waveform



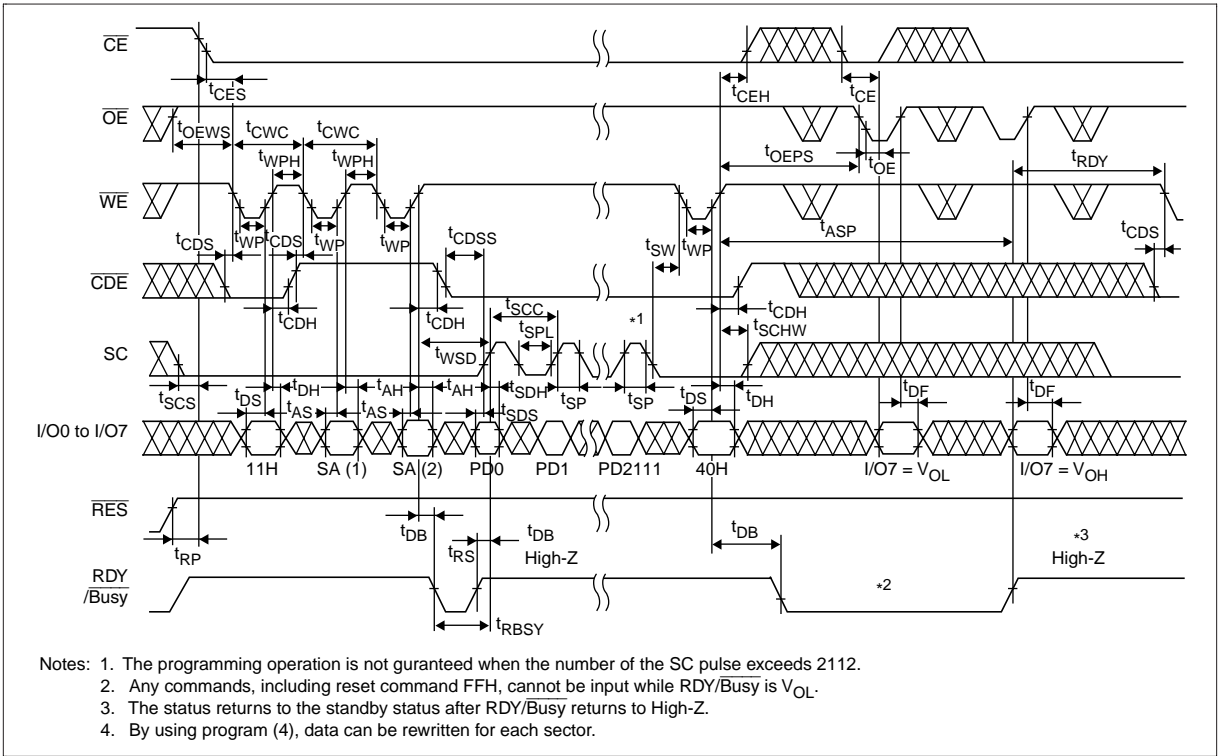
HN29V25611ABP Series

Program (3) and Status Data Polling Timing Waveform

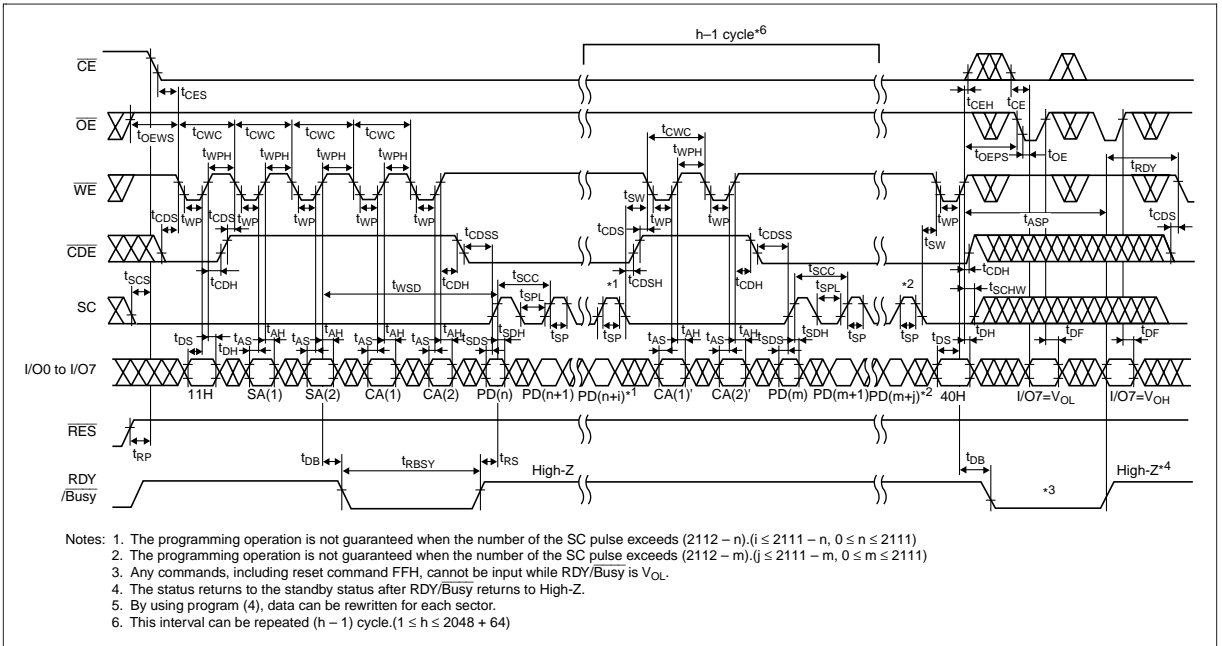


- Notes:
- 1. The programming operation is not guaranteed when the number of the SC pulse exceeds 64.
 - 2. Any commands, including reset command FFH, cannot be input while RDY/Busy is V_{OL} .
 - 3. The status returns to the standby status after RDY/Busy returns to High-Z.
 - 4. By using program (3), the data can be programmed additionally for each sector before erase.

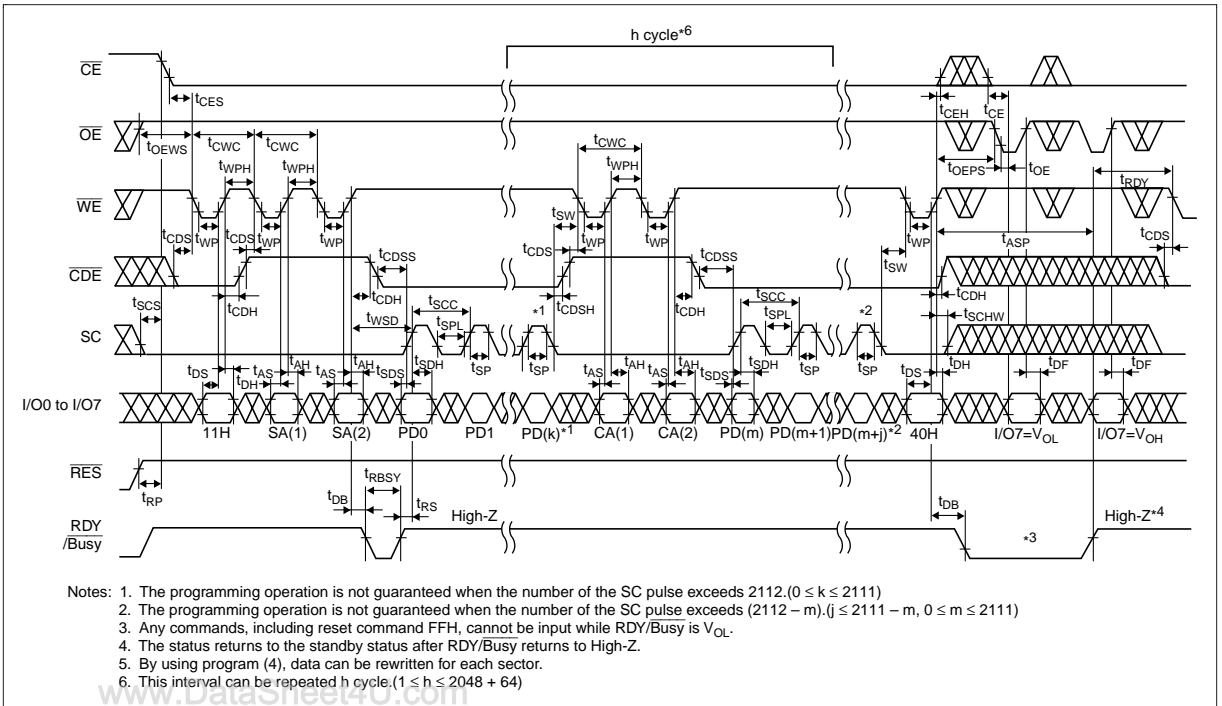
Program (4) and Status Data Polling Timing Waveform



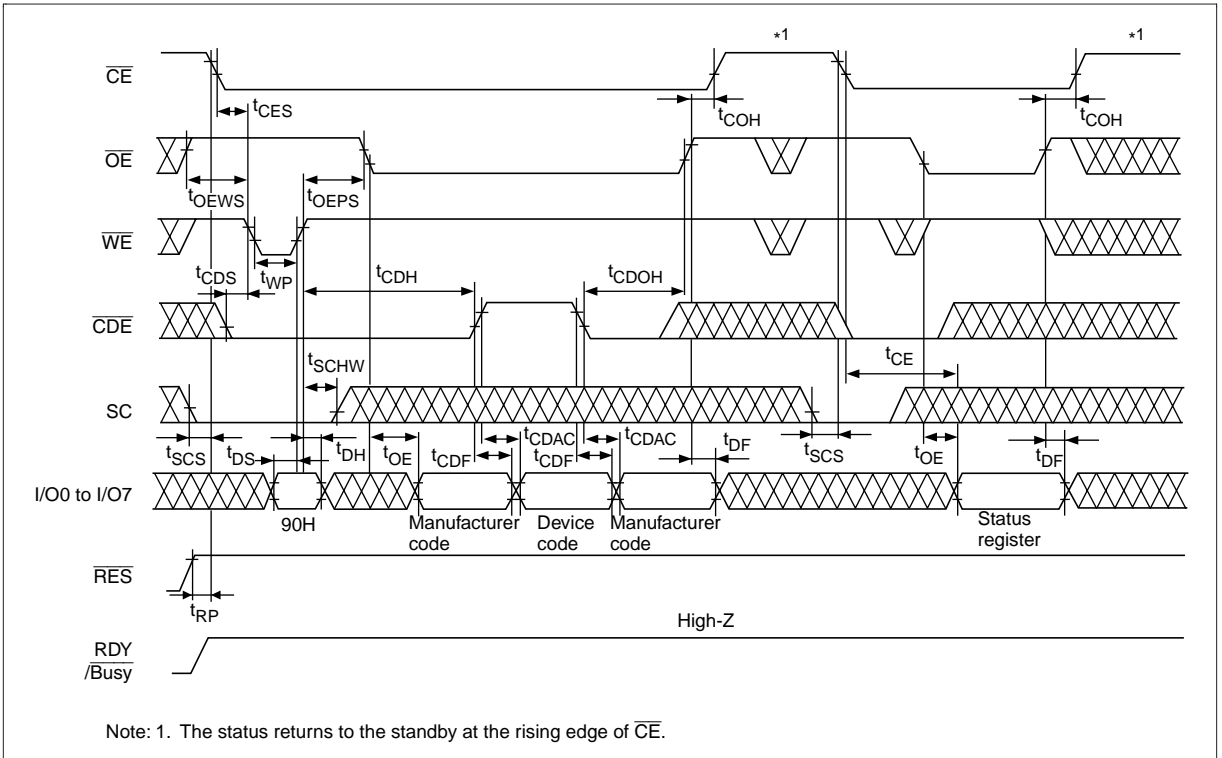
Program (4) with CA before SC and Status Data Polling Timing Waveform



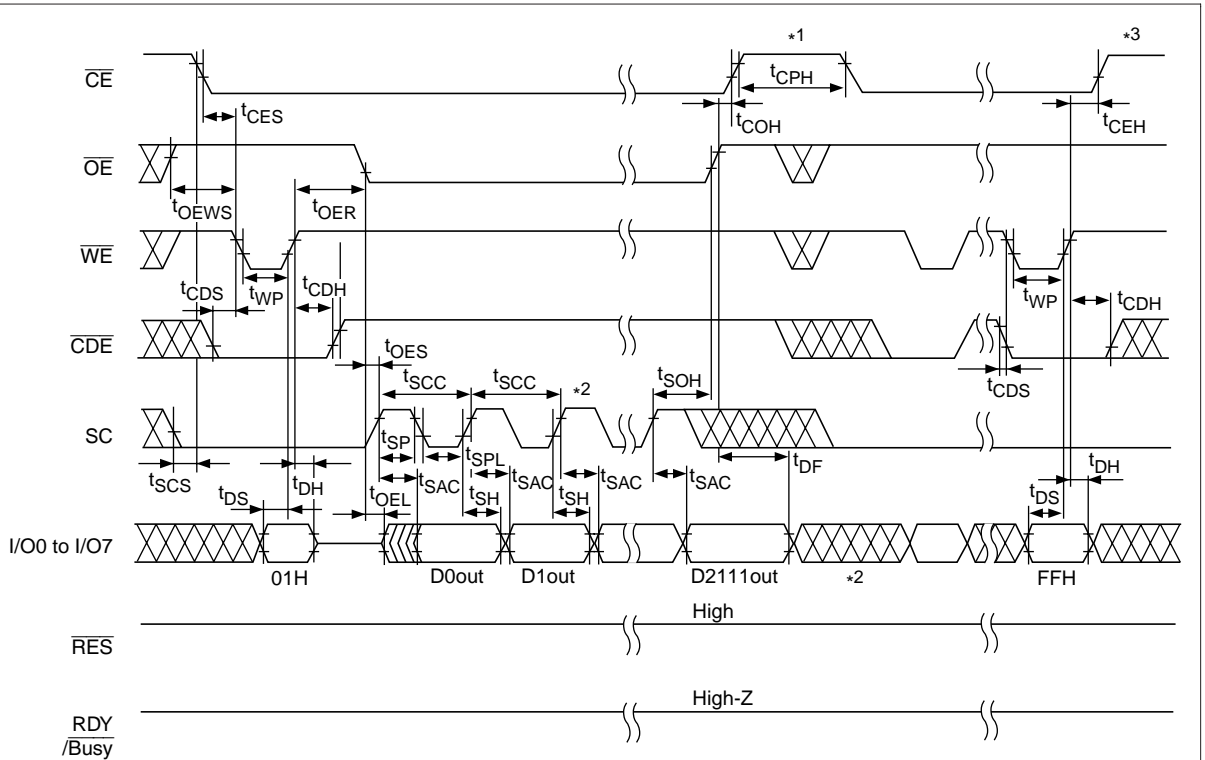
Program (4) with CA after SC and Status Data Polling Timing Waveform



ID and Status Register Read Timing Waveform

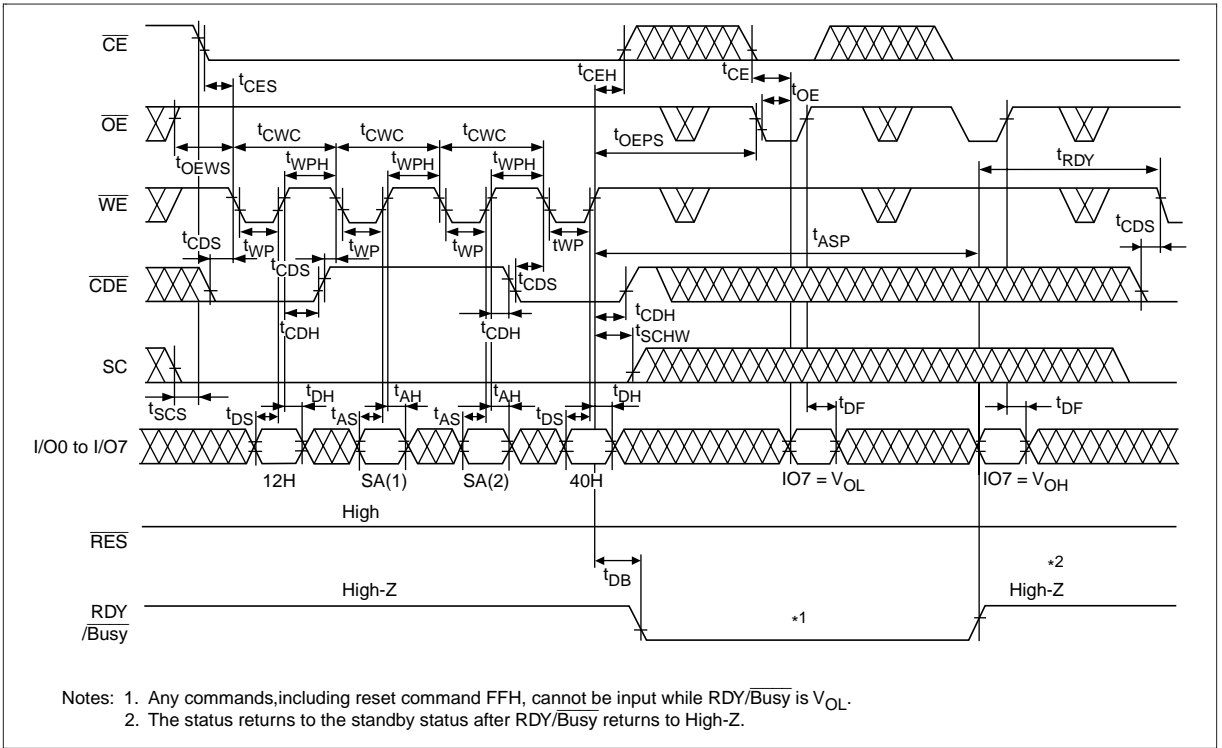


Data Recovery Read Timing Waveform



- Notes:
1. The status returns to the standby at the rising edge of \overline{CE} .
 2. Output data is not valid after the number of the SC pulse exceed 2112 in the recovery data read mode.
 3. After any commands are written, the status can turns to the standby after the command FFH is input and \overline{CE} turns to the V_{IH} level.

Data Recovery Write Timing Waveform



Function Description

Status Register: The HN29V25611A outputs the operation status data as follows: I/O7 pin outputs a V_{OL} to indicate that the memory is in either erase or program operation. The level of I/O7 pin turns to a V_{OH} when the operation finishes. I/O5 and I/O4 pins output V_{OL} s to indicate that the erase and program operations complete in a finite time, respectively. If these pins output V_{OH} s, it indicates that these operations have timed out. If I/O6 pin outputs V_{OH} , it indicates a possibility that can be corrected by ECC, choose data correction by ECC or not by reading out the data. When these pins monitor, I/O7 pin must turn to a V_{OH} . To execute other erase and program operation, the status data must be cleared after a time out occurs. From I/O0 to I/O3 pins are reserved for future use. The pins output V_{OL} s and should be masked out during the status data read mode. The function of the status register is summarized in the following table.

| I/O | Flag definition | Definition |
|------|-------------------------|--|
| I/O7 | Ready/Busy | V_{OH} = Ready, V_{OL} = Busy |
| I/O6 | Program/Erase ECC check | When I/O7 outputs V_{OH} , V_{OH} = ECC available, V_{OL} = ECC not available. |
| I/O5 | Erase check | V_{OH} = Fail, V_{OL} = Pass |
| I/O4 | Program check | V_{OH} = Fail, V_{OL} = Pass |
| I/O3 | Reserved | Outputs a V_{OL} and should be masked out during the status data polling mode. |
| I/O2 | Reserved | |
| I/O1 | Reserved | |
| I/O0 | Reserved | |

ECC Applicability

| I/O7 | I/O6 | I/O5 | I/O4 | System data correction by ECC |
|----------|----------|----------|----------|--------------------------------|
| V_{OH} | V_{OH} | V_{OH} | V_{OL} | Needed |
| V_{OH} | V_{OL} | V_{OH} | V_{OL} | Not needed. Sector replacement |
| V_{OH} | V_{OH} | V_{OL} | V_{OH} | Needed |
| V_{OH} | V_{OL} | V_{OL} | V_{OH} | Not needed. Sector replacement |

This device needs to be corrected failure data by ECC on system or Spare sectors, by reading out again the failure sector data when program/erase error occurs.

Requirement for SystemProgram/Erase Endurance: 10⁵ cycles**Specifications**

| Item | Min | Typ | Max | Unit |
|-----------------------------|------------|------------|------------|-------------|
| Usable sectors (initially) | 16,057 | — | 16,834 | sector |
| Spare sectors | 290 | — | — | sector |
| ECC (Error Correction Code) | 3 | — | — | bit/sector |

Unusable Sector

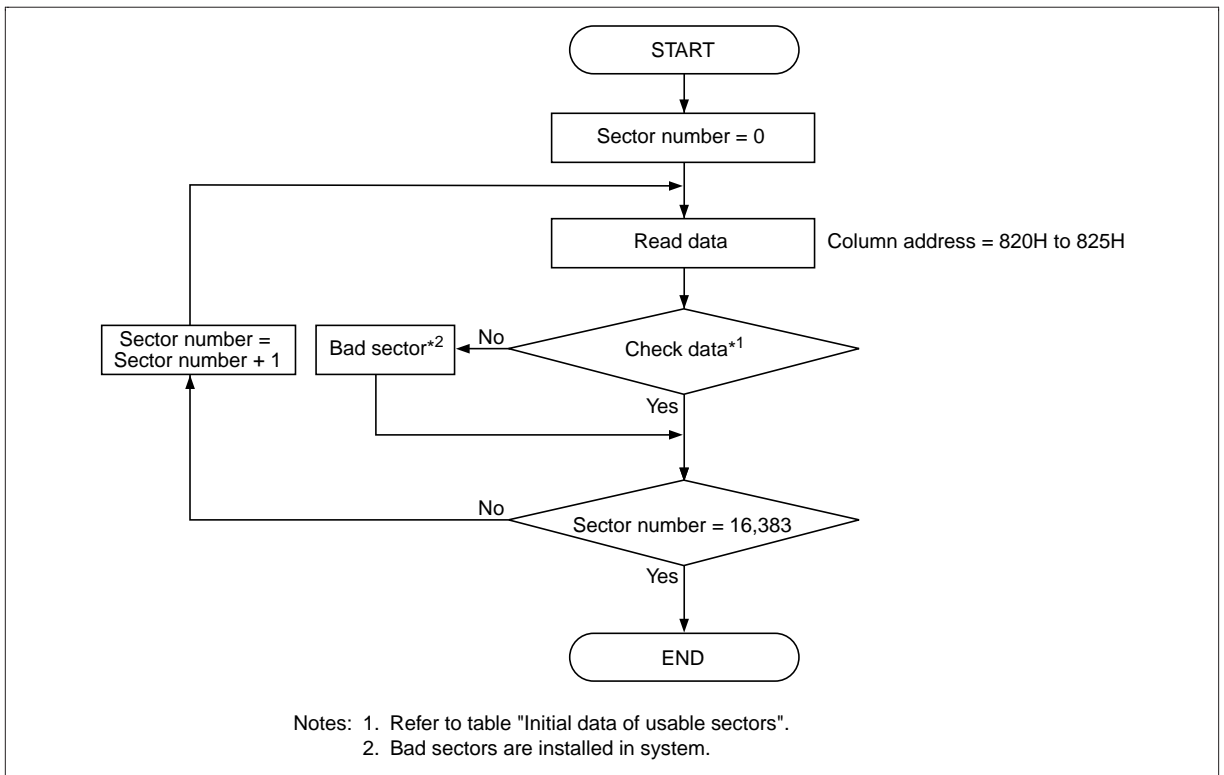
Initially, the HN29V25611A includes unusable sectors. The unusable sectors must be distinguished from the usable sectors by the system as follows.

1. Check the partial invalid sectors in the devices on the system. The usable sectors were programmed the following data. Refer to the flowchart "Indication of unusable sectors".

Initial Data of Usable Sectors

| Column address | 0H to 81FH | 820H | 821H | 822H | 823H | 824H | 825H | 826H to 83FH |
|----------------|------------|------|------|------|------|------|------|--------------|
| Data | FFH | 1CH | 71H | C7H | 1CH | 71H | C7H | FFH |

2. Do not erase and program to the partial invalid sectors by the system.

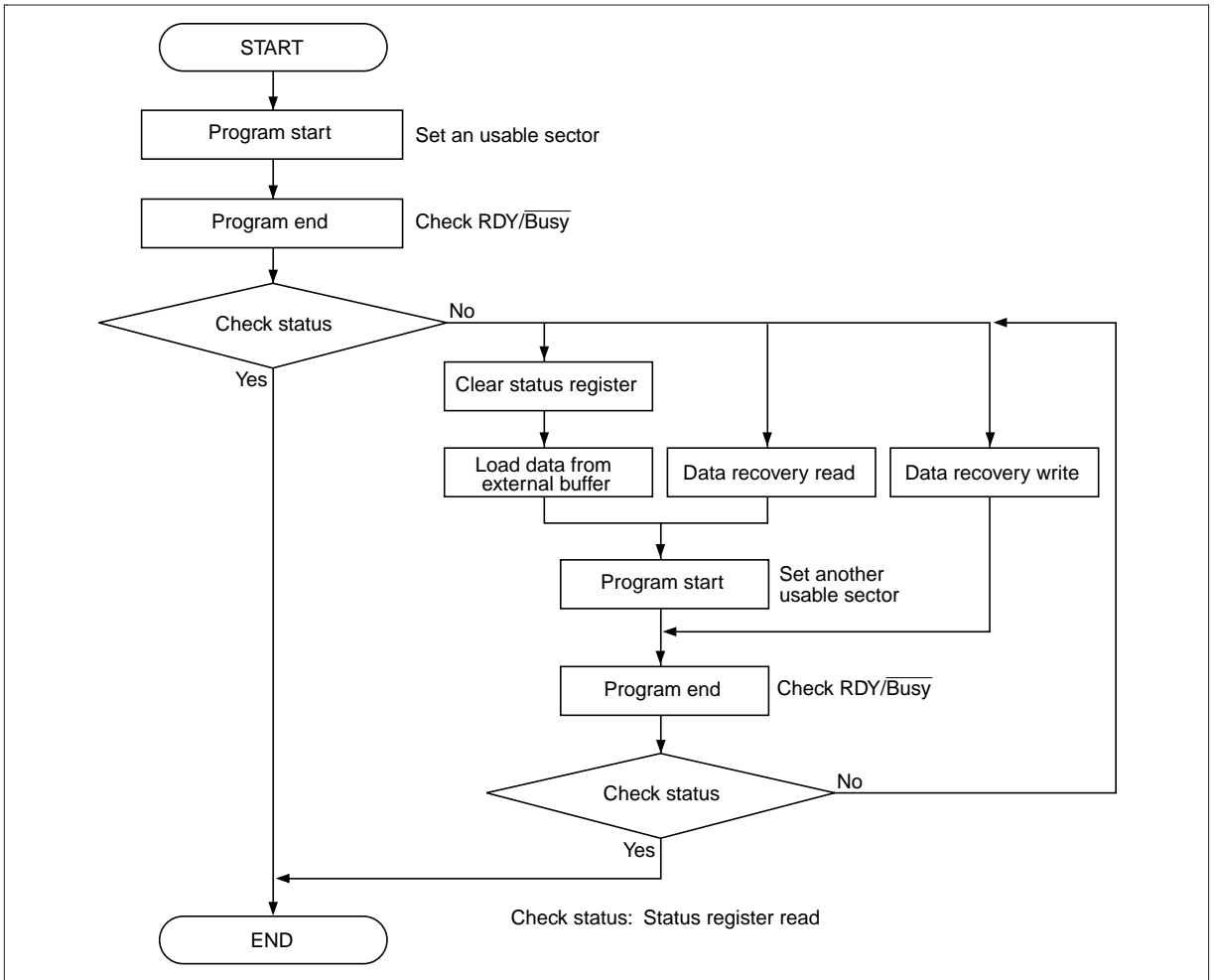


The Unusable Sector Indication Flow

Requirements for High System Reliability

The device may fail during a program, erase or read operation due to write or erase cycles. The following architecture will enable high system reliability if a failure occurs.

1. For an error in read operation: An ECC (Error Correction Code) or a similar function which can correct 3-bits per each sectors is required for data reliability. When error occurs, data must not be corrected by replacing to spare sector.
2. For errors in program or erase operations: The device may fail during a program or erase operation due to write or erase cycles. The status register indicates if the erase and program operation complete in a finite time. When an error occurred in the sector, try to reprogram the data into another sector. Avoid further system access to the sector that error happens. Typically, recommended number of a spare sectors are 1.8% (290 sectors (min.)) of initial usable 16,057 sectors (min) by each device. For the reprogramming, do not use the data from the failed sectors, because the data from the failed sectors are not fixed. So the reprogram data must be the data reloaded from the external buffer, or use the Data recovery read mode or the Data recovery write mode (see the “Mode Description” and under figure “Spare Sectors Replacement Flow after Program Error”). To avoid consecutive sector failures, choose addresses of spare sectors as far as possible from the failed sectors. In this case, 10^5 cycles of program/erase endurance is guaranteed.



Spare Sector Replacement Flow after Program Error

For Errors in program or erase operations

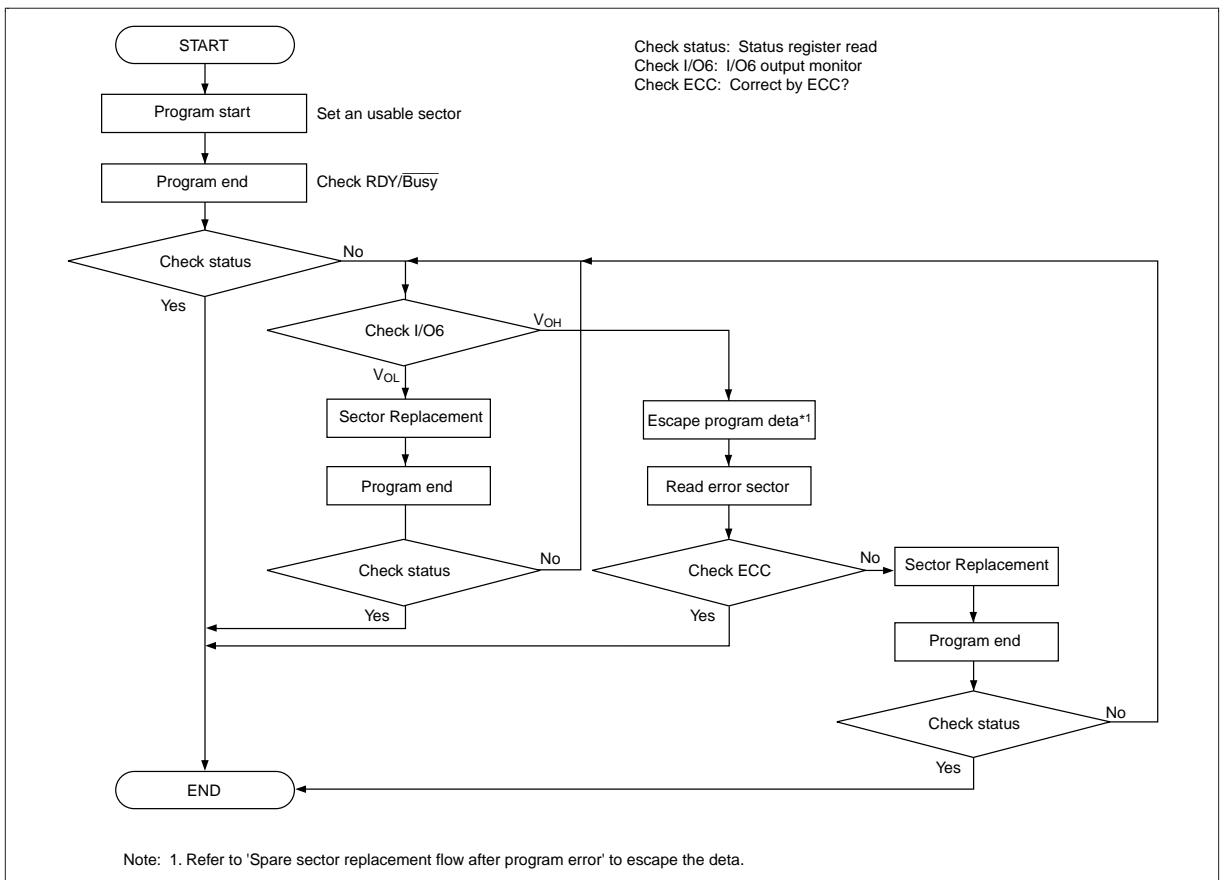
The device may fail during a program or erase operation. Failure mode can be confirmed by read out the status register after complete the erase and program operations. There are two failure modes specified by each codes:

1: Status register error flag: $I/O6 = V_{OL}$

Replace sector under the “Spare Sectors Replacement Flow at Status Register I/O6 Read”. Replacement must be applied to one sector(2k bytes) which contains failure bits.

2: Status register error flag: $I/O6 = V_{OH}$

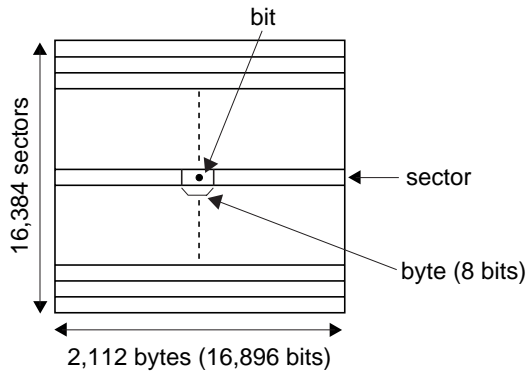
Escape the program data temporary under the “Replacement Flow at Status Register I/O6 Read”. If failure data can be corrected by ECC, do not replace to spare sector. If failure data can not be corrected by ECC, replace to spare sector. Replacement must be applied to one sector(2k bytes) which contains failure bits.



Spare Sectors Replacement Flow at Status Register I/O6 Read

HN29V25611ABP Series

Memory Structure



Bit: Minimum unit of data.

Byte: Input/output data unit in programming and reading. (1 byte = 8 bits)

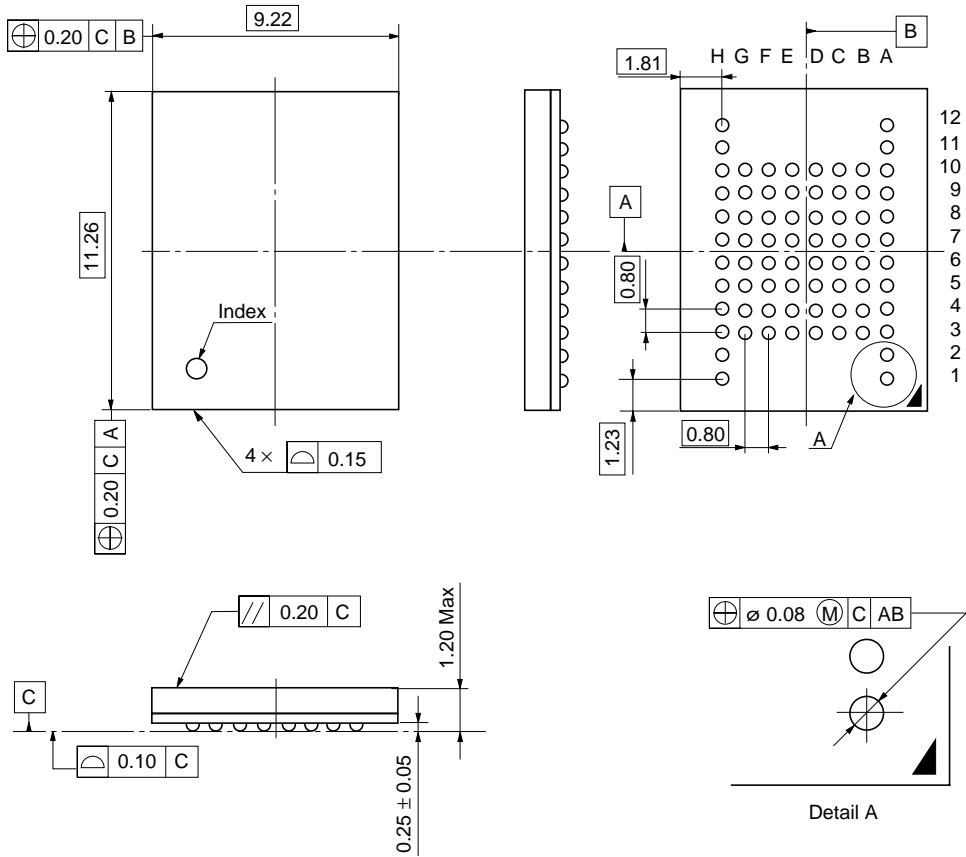
Sector: Page unit in erase, programming and reading. (1 sector = 2,112 bytes = 16,896 bits)

Device: 1 device = 16,384 sectors.

Package Dimensions

HN29V25611ABP Series (TBP-72A)

Unit: mm



| | |
|------------------------|---------|
| Hitachi Code | TBP-72A |
| JEDEC | — |
| EIAJ | — |
| Mass (reference value) | 0.13 g |

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