HN29V2G74WT-30

(128M × 8-bit) ×2 AG-AND Flash Memory

REJ03C0182-0200Z
Rev. 2.00
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Description

The HN29V2G74 is a 2G-bit AG-AND flash memory. It mounts two 1G-bit AG-AND flash memories with multi-level memory cells, which are programmable and erasable automatically with a single 3.0 V power supply. It achieves a write speed of 10 Mbytes/sec, which is 5 times faster than Renesas's previous multi level cell Flash memory, using 0.13µm process technology and AG-AND (Assist Gate-AND) type Flash memory cell using multi level cell technology provides both the most cost effective solution and high speed programming.

Features

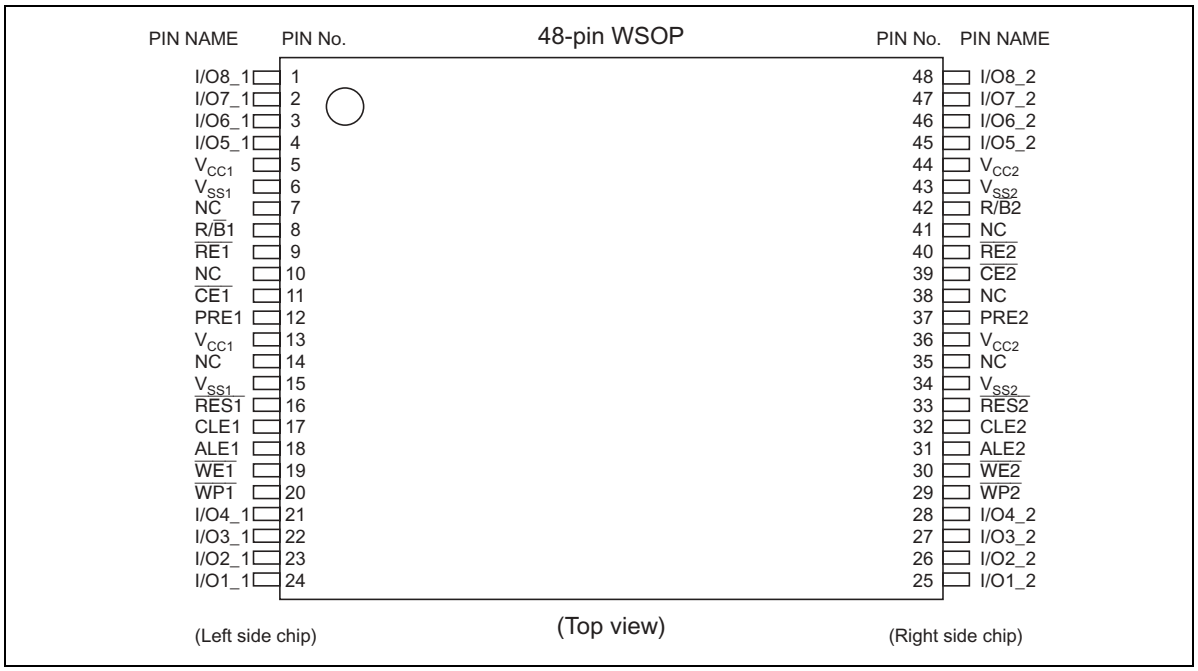
- On-board single power supply: V_{CC} = 2.7 V to 3.6 V
- Operation Temperature range: Ta = 0 to +70°C
- Memory organization
  - Memory array: (2048+64) bytes × 16384 page × 4 Bank × 2
  - Page size: (2048+64) bytes × 2
  - Block size: (2048+64) bytes × 2 page × 2
  - Page Register: (2048+64) bytes × 4 Bank × 2
- Multi level memory cell
  - 2bit/cell
- Automatic program
  - Page program
  - Multi bank program
  - Cache program
  - 2 page cache program
- Automatic Erase
  - Block Erase
  - Multi Bank Block Erase
- Access time
  - Memory array to register (1st access time): 120 µs max
  - Serial access: 35 ns min

- Low power dissipation
  - I_{CC1} = 10 mA (typ) : Read (50 ns cycle) (1-chip operation)
  - I_{CC1} = 20 mA (typ) : Read (50 ns cycle) (2-chip operation)
  - I_{CC2} = 15 mA (typ) : Read (35 ns cycle) (1-chip operation)
  - I_{CC2} = 30 mA (typ) : Read (35 ns cycle) (2-chip operation)
  - I_{CC3} = 10 mA (typ) : Program (single bank) (1-chip operation)
  - I_{CC3} = 20 mA (typ) : Program (single bank) (2-chip operation)
  - I_{CC4} = 20 mA (typ) : Program (Multi bank) (1-chip operation)
  - I_{CC4} = 40 mA (typ) : Program (Multi bank) (2-chip operation)
  - I_{CC5} = 10 mA (typ) : Erase (single bank) (1-chip operation)
  - I_{CC5} = 20 mA (typ) : Erase (single bank) (2-chip operation)
  - I_{CC6} = 15 mA (typ) : Erase (Multi bank) (1-chip operation)
  - I_{CC6} = 30 mA (typ) : Erase (Multi bank) (2-chip operation)
  - I_{sb1} = 1 mA (max) : Standby (TTL) (1-chip operation)
  - I_{sb1} = 2 mA (max) : Standby (TTL) (2-chip operation)
  - I_{sb2} = 50 µA (max) : Standby (CMOS) (1-chip operation)
  - I_{sb2} = 100 µA (max) : Standby (CMOS) (2-chip operation)
  - I_{sb3} = 5 µA (max) : Deep standby (1-chip operation)
  - I_{sb3} = 10 µA (max) : Deep standby (2-chip operation)
- Program time: 600 µs (typ) (Single/Multi bank)
  - transfer rate: 10 MB/s (Multi bank)
- Erase time: 650 µs (typ) (Single/Multi bank)
- The following architecture is required for data reliability
  - Error correction: 3 bit error correction per 512byte are recommended.
  - Block replacement: When an error occurs in program page, block replacement including corresponding page should be done. When an error occurs in erase operation, future access to this bad block is prohibited. It is required to manage it creating a table or using another appropriate scheme by the system (Valid blocks: Initial valid blocks for more than 98% per Bank. Replacement blocks must be ensured more than 1.8% of valid blocks per Bank).
  - Wear leveling: Wear leveling is to level Program and Erase cycles in one block in order to reduce the burden for one block and let the device last for long time. Actually, it does detect the block which is erased and rewritten many times and replace it with less accessed block.
    To secure 10^5 cycles as the program/erase endurance, need to control not to exceed Program and Erase cycles to one block. You should adopt wear leveling once in 5000 Program and Erase cycles. It is better to program it as a variable by software.
- Program/Erase Endurance: 10^5 cycles
- Package line up
  - WSOP: WSOP 48pin package (TFP-48DBV)

Ordering Information

Type No.	Operating voltage (V_{CC})	Organization	Package
HN29V2G74WT-30	2.7 V to 3.6 V	×8	12.0 × 17.0 mm^2 0.5 mm pitch 48-pin plastic WSOP (TFP-48DBV) Lead free

Pin Arrangement

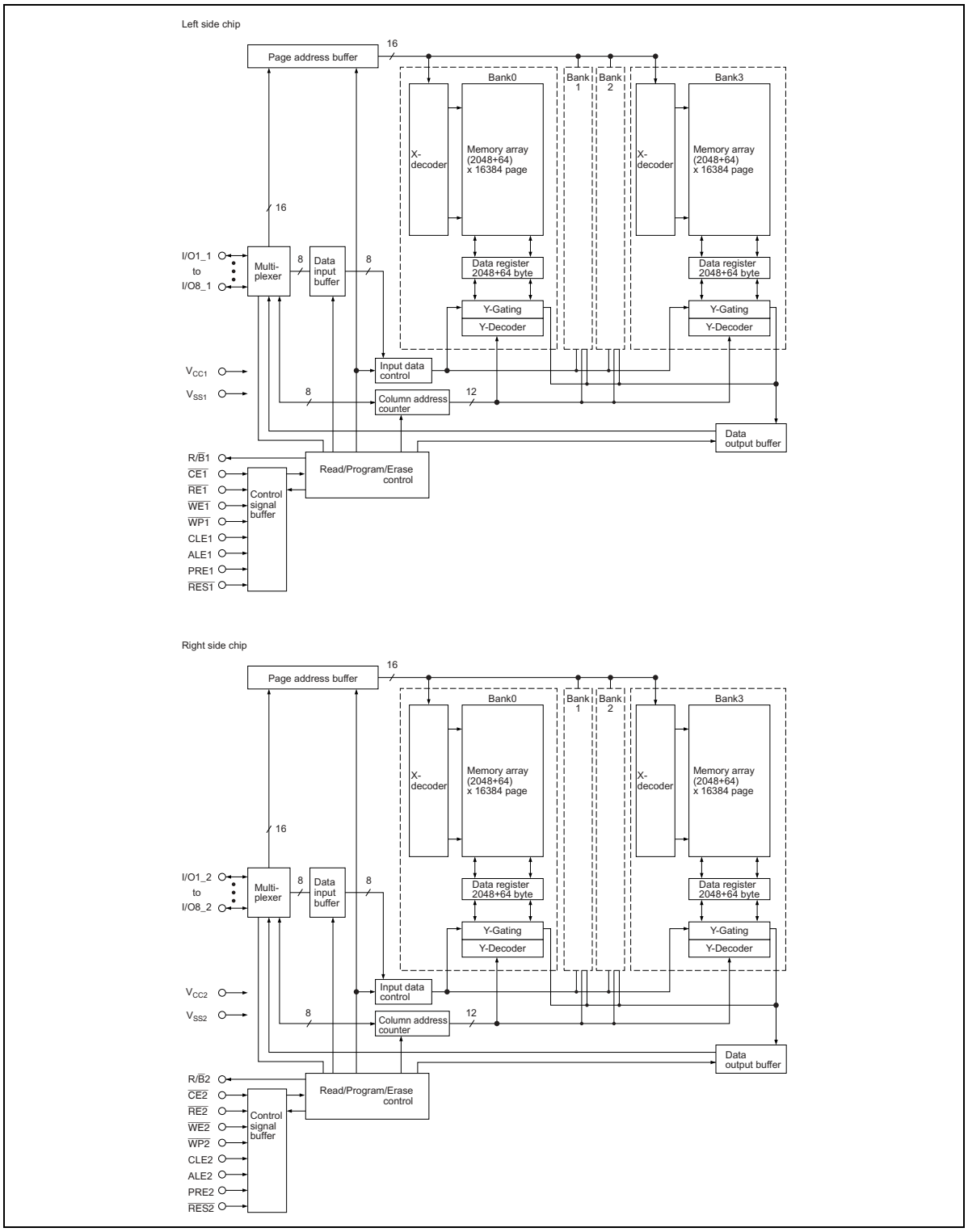


Pin configuration

Pin name	Function
I/O 1_1 to I/O 8_1, I/O 1_2 to I/O 8_2	Command, address, data Input/output
CLE1, CLE2	Command Latch Enable
ALE1, ALE2	Address Latch Enable
$\overline{CE1}$, $\overline{CE2}$	Chip Enable
$\overline{RE1}$, $\overline{RE2}$	Read Enable
$\overline{WE1}$, $\overline{WE2}$	Write Enable
$\overline{WP1}$, $\overline{WP2}$	Write Protect
R/$\overline{B1}$, R/$\overline{B2}$	Ready/$\overline{Busy}$
PRE1, PRE2	Power on Auto Read Enable
$\overline{RES1}$, $\overline{RES2}$	Reset
V_{CC1}, V_{CC2}*1	Power
V_{SS1}, V_{SS2}*2	Ground
NC	No Connection

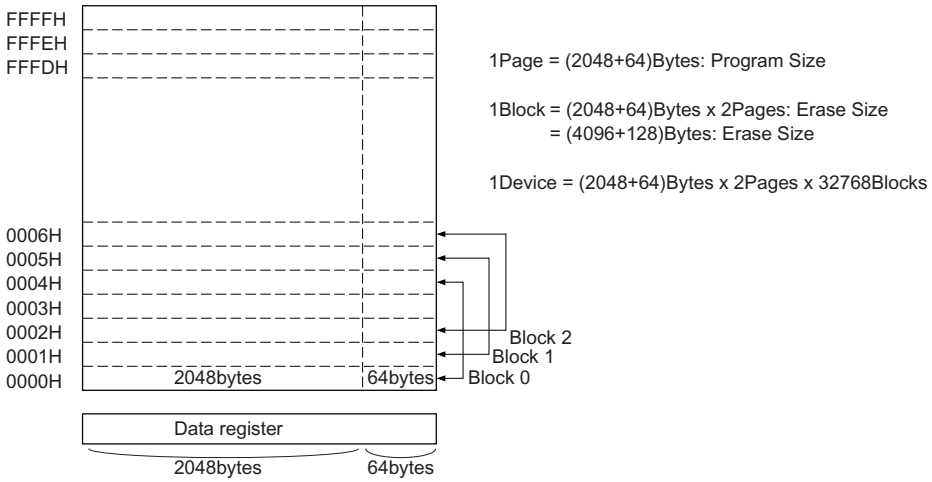
Notes: 1. In this datasheet, V_{CC} means both V_{CC1} and V_{CC2}, unless otherwise noted.
2. In this datasheet, V_{SS} means both V_{SS1} and V_{SS2}, unless otherwise noted.

Block Diagram



Memory map and address

Memory Map

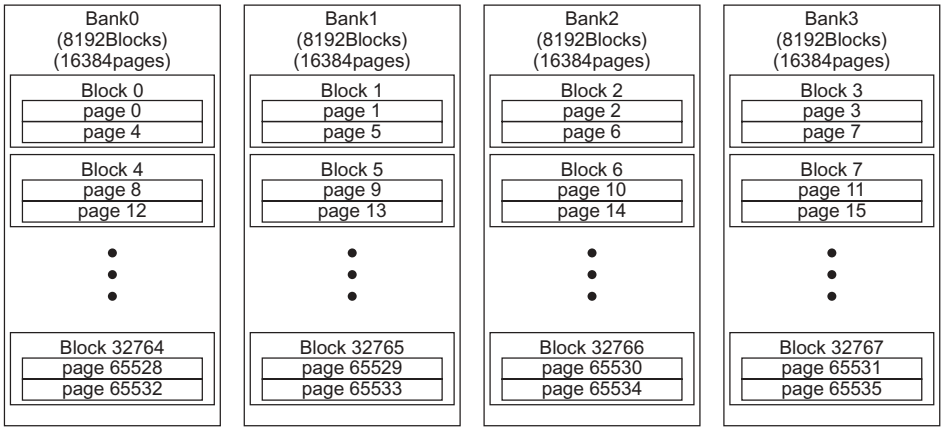


1Page = (2048+64)Bytes: Program Size

1Block = (2048+64)Bytes x 2Pages: Erase Size
= (4096+128)Bytes: Erase Size

1Device = (2048+64)Bytes x 2Pages x 32768Blocks

Bank Organization



Addressing

	Symbol	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	
1st Cycle	CA1	A7	A6	A5	A4	A3	A2	A1	A0	Column address
2nd Cycle	CA2	L	L	L	L	A11	A10	A9	A8	
3rd Cycle	RA1	A19	A18	A17	A16	A15	A14	A13	A12	Row address
4th Cycle	RA2	A27	A26	A25	A24	A23	A22	A21	A20	

A12, A13: Bank select
A14: Page select
A15 to A27: Block select

Pin Functions

Chip Enable: $\overline{CE1}$, $\overline{CE2}$

$\overline{CE1}$ and $\overline{CE2}$ are used, to select the left side chip or the right side chip, respectively, of the device. In this datasheet, $\overline{CE}$ means both $\overline{CE1}$ and $\overline{CE2}$, unless otherwise noted.
It goes to the standby mode when $\overline{CE}$ goes to 'H' level when the device is in the Output disable state.
When the device is in the Busy state during Program or Erase or Read operation, $\overline{CE}$ signal is ignored and the device does not return to the standby mode even if $\overline{CE}$ goes to High.

Read Enable: $\overline{RE1}$, $\overline{RE2}$

The $\overline{RE1}$ and $\overline{RE2}$ signals control, serial data output of the left side chip or the right side chip, respectively. In this datasheet, $\overline{RE}$ means both $\overline{RE1}$ and $\overline{RE2}$, unless otherwise noted. Data is available t_{REA} after the falling edge of $\overline{RE}$.
The internal address counter is also incremented by one (Address = Address + 1) on this falling edge.

Write Enable: $\overline{WE1}$, $\overline{WE2}$

$\overline{WE1}$ and $\overline{WE2}$ are the signals to latch each data from the I/O port, in the left side chip or the right side chip, respectively, of the device. In this datasheet, $\overline{WE}$ means both $\overline{WE1}$ and $\overline{WE2}$, unless otherwise noted. Data are latched in the device on the rising edge of $\overline{WE}$.

Command Latch Enable: CLE1, CLE2

The CLE1 and CLE2 input signals are used to control loading of the operation mode command into the internal register, of the left side chip or the right side chip, respectively. In this datasheet, CLE means both CLE1 and CLE2, unless otherwise noted.
The command is latched into the internal register from the I/O port on the rising edge of $\overline{WE}$ when CLE is high.

Address Latch Enable: ALE1, ALE2

The ALE1 and ALE2 input signals are used to control loading of the input address information or input data into the internal address/data register, of the left side chip or the right side chip, respectively. In this datasheet, ALE means both ALE1 and ALE2, unless otherwise noted.
Address is latched on the rising edge of $\overline{WE}$ with ALE high and Data is latched with ALE low.

I/O port: I/O1_1 to I/O8_1

The I/O1_1 to I/O8_1 and I/O1_2 to I/O8_2 pins are used as a port for transferring address, command and input/output data to and from the device.
I/O1_1 to I/O8_1 are used to the left side chip, I/O1_2 to I/O8_2 are used to the right side chip, respectively. In this datasheet, for example, I/O1 means both I/O1_1 and I/O1_2, unless otherwise noted.

Write Protect: $\overline{WP1}$, $\overline{WP2}$

The $\overline{WP1}$ and $\overline{WP2}$ signals are used to protect, the left side chip or the right side chip of the device, respectively, from accidental programming or erasing. In this datasheet, $\overline{WP}$ means both $\overline{WP1}$ and $\overline{WP2}$, unless otherwise noted.

The $\overline{WP}$ low reset internal program/erase operation. It is usually used for protecting the data with the $\overline{WP}$ low during the power-on/off sequence when input signals are invalid.

Ready Busy: R/$\overline{B}$1, R/$\overline{B}$2

The R/$\overline{B}$ 1 and R/$\overline{B}$2 output signals indicate the status of the device operation, of the left side chip or the right side chip, respectively. In this datasheet, R/$\overline{B}$ means both R/$\overline{B}$ 1 and R/$\overline{B}$ 2, unless otherwise noted. When R/$\overline{B}$ is low, it indicates that the Program, Erase or Read operation is in process. After the operation is completed, R/$\overline{B}$ turns back to the high impedance state.
The output buffer for this signal is an open-drain and has to be pulled up to V_{CC} with appropriate register.

Reset: $\overline{RES1}$, $\overline{RES2}$

The $\overline{RES1}$ and $\overline{RES2}$ signals control reset operation, for the left side chip or the right side chip, respectively, of the device. In this datasheet, $\overline{RES}$ means both $\overline{RES1}$ and $\overline{RES2}$, unless otherwise noted. When power on and power off, keep the $\overline{RES}$ pin V_{ILD} level ($V_{SS} \pm 0.2V$), and keep pin V_{IHD} level ($V_{CC} \pm 0.2V$) during program, erase, read operation.
The transition to deep standby mode is executed when $\overline{RES}$ set V_{ILD} level during standby mode.

Power on auto Read Enable: PRE1, PRE2

The PRE1 and PRE2 control auto read operation executed during power-on, in the left side chip or the right side chip, respectively. In this datasheet, PRE means both PRE1 and PRE2, unless otherwise noted. The power-on auto-read is enabled when PRE pin is tied to V_{CC}. Please contact Renesas Technology's sales office before using the power-on auto-read.

Mode selection

The address input, command input, and data input/output operation of the device are controlled by $\overline{RES}$, $\overline{WP}$, $\overline{WE}$, $\overline{CE}$, CLE, ALE, $\overline{RE}$, PRE signals. The following shows the operation logic table.

Logic Table

Mode		$\overline{RES}$*3	$\overline{WP}$*3	$\overline{CE}$	$\overline{WE}$	CLE	ALE	$\overline{RE}$	PRE*3
Read Mode	Command Input	H	×	L	⌐⌐	H	L	H	×*2
	Address Input (4clock)	H	×	L	⌐⌐	L	H	H	×*2
Write Mode	Command Input	H	H	L	⌐⌐	H	L	H	×*2
	Address Input (4clock)	H	H	L	⌐⌐	L	H	H	×*2
Data Input		H	H	L	⌐⌐	L	L	H	×*2
Data Output		H	×	L	H	L	L	⌐⌐	×*2
During Read (Busy)		H	×	L	H	L	L	H	×*2
During Program (Busy)		H	H	×	×	×	×	×	×*2
During Erase (Busy)		H	H	×	×	×	×	×	×*2
Write Protect		H	L	×	×	×	×	×	×*2
Stand-by		H	$V_{SS} \pm 0.2$ V /$V_{CC} \pm 0.2$ V	H	×	×	×	×	$V_{SS} \pm 0.2$ V /$V_{CC} \pm 0.2$ V
Deep Stand-by		$V_{SS} \pm 0.2$ V	$V_{SS} \pm 0.2$ V /$V_{CC} \pm 0.2$ V	×	×	×	×	×	$V_{SS} \pm 0.2$ V /$V_{CC} \pm 0.2$ V

Notes: 1. H: V_{iH}, L: V_{iL}, ×: V_{iH} or V_{iL}
2. PRE must be “H” fix when using Power On Auto Read and “L” fix when not using it.
3. $\overline{RES}$, $\overline{WP}$, PRE must be set L: V_{iLD}, H: V_{iHD}, ×: V_{iHD} or V_{iLD}

Program/Erase Characteristics

	Symbol	Min	Typ	Max	Unit	Notes
Program Time	t_{PROG}	—	0.6	2.4	ms	
Cache Program Time	t_{CPROG}	—	0.6	4.8	ms	
Dummy Busy for Cache Program	t_{CBSY}	—	3	2400	µs	
Dummy Busy Time	t_{DBSY}	1	—	4	µs	
Number of Partial Program Cycles in a Same Page	N	—	—	8	cycles	
Block Erase Time	t_{BERS}	—	0.65	20	ms	
Page mode Erase Verify Time	t_{PEV}	—	—	50	µs	
Block mode Erase Verify Time	t_{BEV}	—	—	70	µs	

Command Definition

Command Sets	1st. cycle	2nd. cycle	acceptable while Busy
Read	00h	30h	
Multi Bank Read	00h	31h	
Random Data output in a Page	05h	E0h	
Read for copy back	00h	35h	
Copy Back Program	85h	10h	
Page Data output	06h	E0h	
Multi Bank Copy Back Program	85h	11h	
Data Recovery Read	06h	E0h	
Data Recovery Program	85h	10h	
Reset	FFh	—	Acceptable
Page Program	80h	10h	Acceptable*[2]
Random Data Input in a Page	85h	—	Acceptable*[2]
Multi Bank Page Program	80h	11h	Acceptable*[2]
Cache Program	80h	15h	
Block Erase	60h	D0h	
Multi Bank Block Erase	60h–60h	D0h	
Read Status	70h	—	Acceptable
Read Error Status	72h	—	Acceptable
Read Multi Block Status	71h	—	Acceptable
Read Multi Block Error Status*[1]	73h, 74h, 75h, 76h	—	Acceptable
Status mode Reset	7Fh	—	
Page mode Erase Verify	60h	D2h	
Block mode Erase Verify	60h	D3h	
Read ID	90h	—	
Device Recovery	00h	38h	

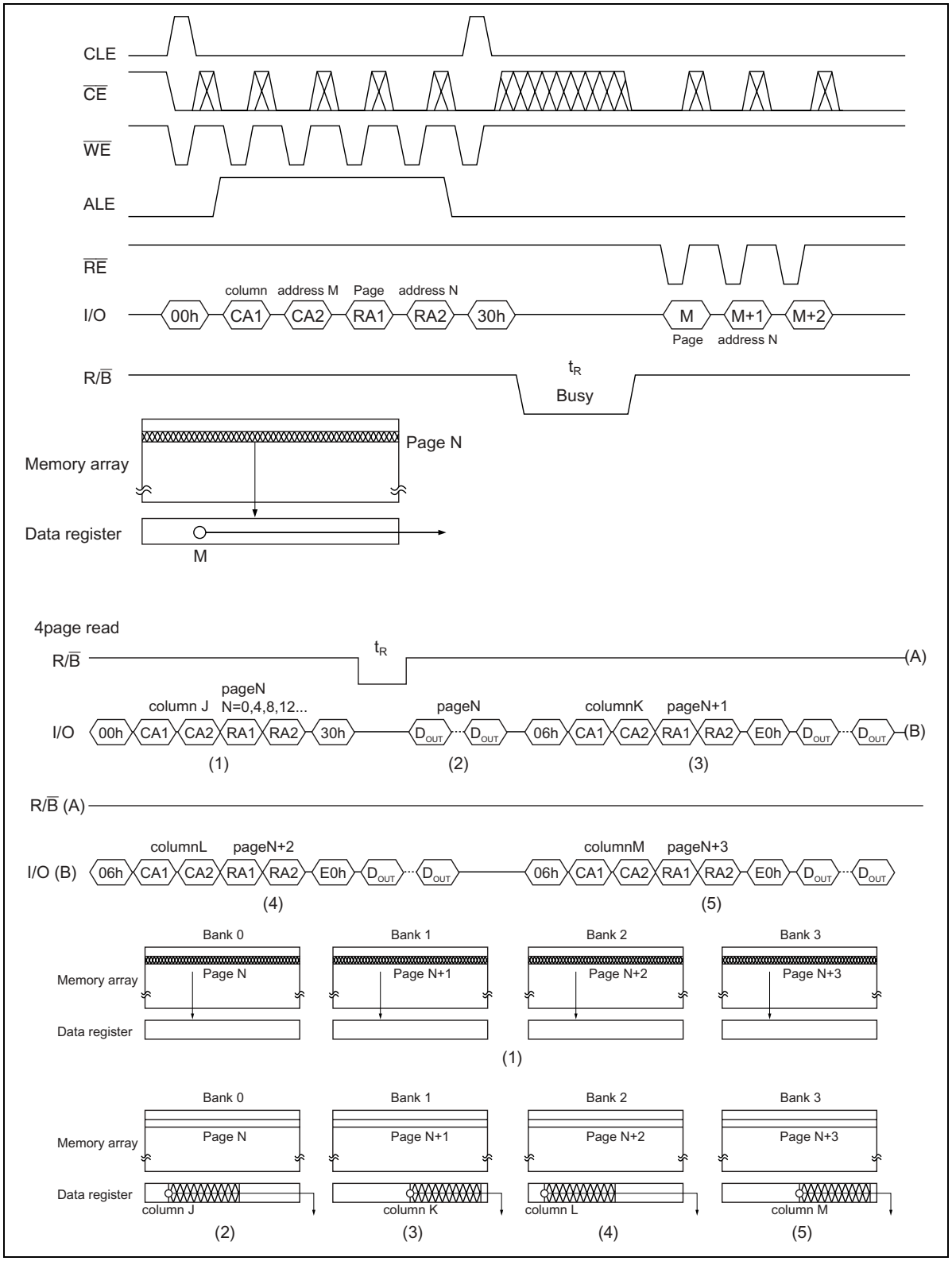
Notes: 1. Read Multi Block Error Status
73h: Bank0 Error Status, 74h: Bank1 Error Status, 75h: Bank2 Error Status, 76h: Bank3 Error Status

2. The input of the program data can be done only in Busy state of Erase operation.

Device Operation

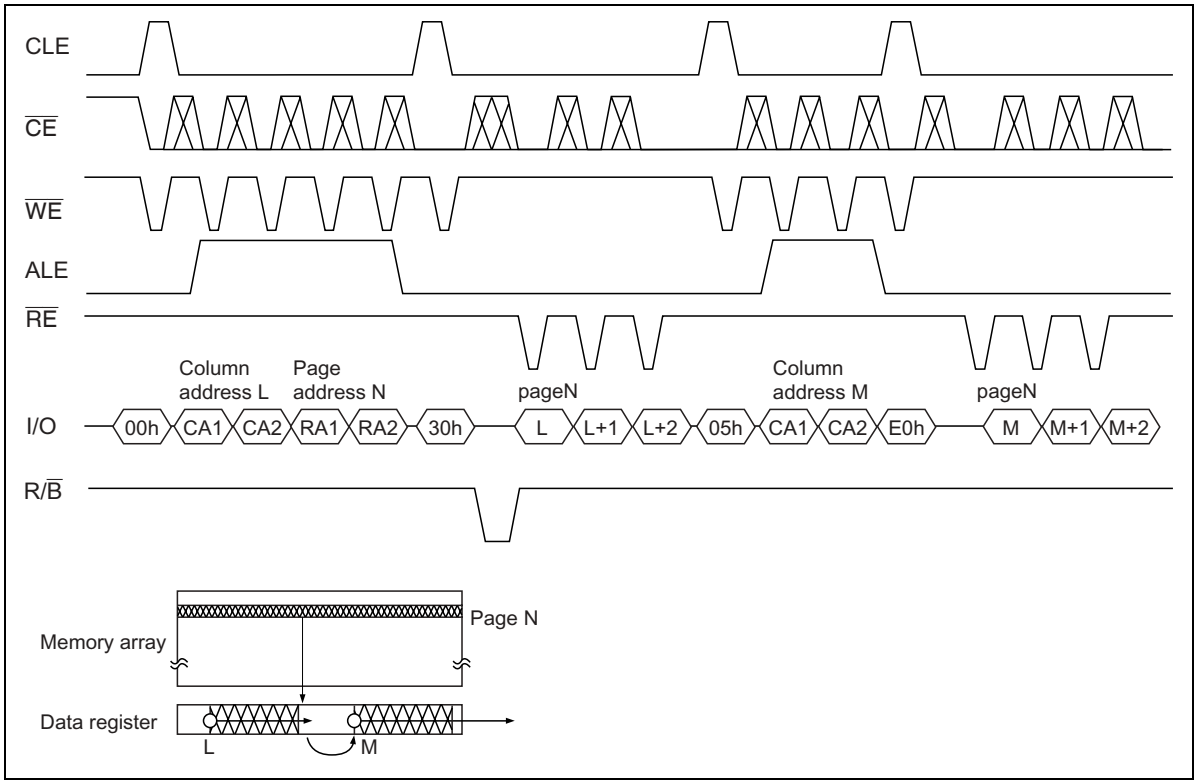
Page Read

It becomes Busy state with $\overline{WE}$ rising edge after writing 00h along with four address cycles and 30h and data transfer starts from memory array to the data register. The device output the data serially from specified column address when inputting address by the repetitive high to low transition of the $\overline{RE}$ clock after it is Ready state.
It is possible to shorten Busy time after the 2nd page when the data of page overlapped to 4 bank consecutively like Page 0, Page1, Page 2, Page 3 is read out (Please see 4 page read below).
The data of Page 1 to Page 3 are transferred to the data register when writing 00h and 30h specifying column address and Page 0.
The device output the data of Page 0 serially by clocking $\overline{RE}$ after transferring it from memory array to the data register.
The data of Page 1, Page 2, Page 3 which are transferred to the data register can be output using Page data out command (06h/E0h) after the data of Page 0 output.


CLE
CE
WE
ALE
RE
I/O
column address M
Page address N
00h
CA1
CA2
RA1
RA2
30h
M
M+1
M+2
Page address N
R/B
tR
Busy
Memory array
Page N
Data register
M
4page read
R/B
tR
(A)
I/O
column J
pageN
N=0,4,8,12...
pageN
columnK
pageN+1
00h
CA1
CA2
RA1
RA2
30h
DOUT
06h
E0h
(B)
(1)
(2)
(3)
R/B (A)
I/O (B)
columnL
pageN+2
columnM
pageN+3
(4)
(5)
Bank 0
Bank 1
Bank 2
Bank 3
Memory array
Page N
Page N+1
Page N+2
Page N+3
Data register
(1)
column J
column K
column L
column M
(2)
(3)
(4)
(5)

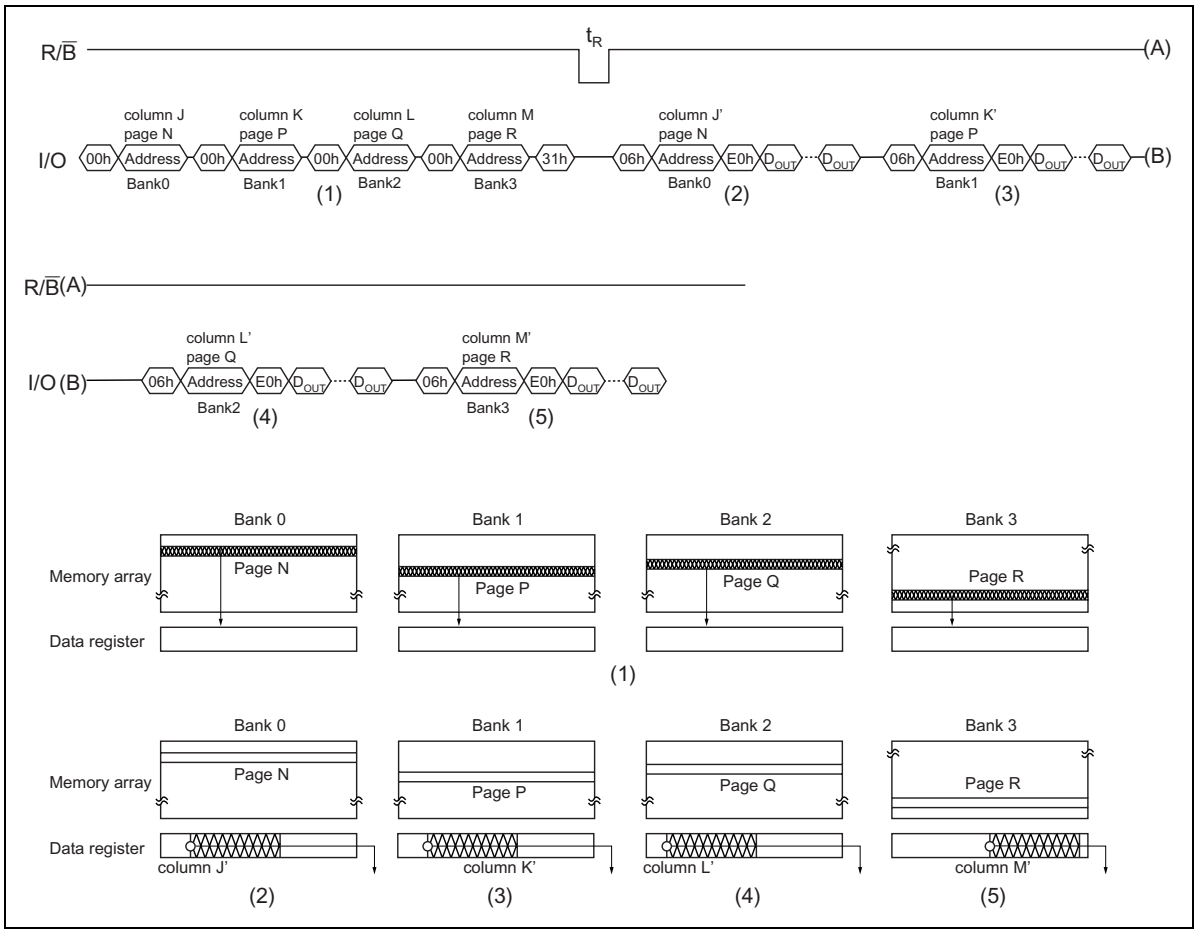
Random Data output in a Page Read

When the device output the data serially in Page read mode operation, the data from any column address in a Page which is reading can be output by writing 05h and E0h with two column address cycles.
There is no restriction on an order of column address which can be specified and it is possible to specify many times including same column address in the same Page address.



Multi Bank Read

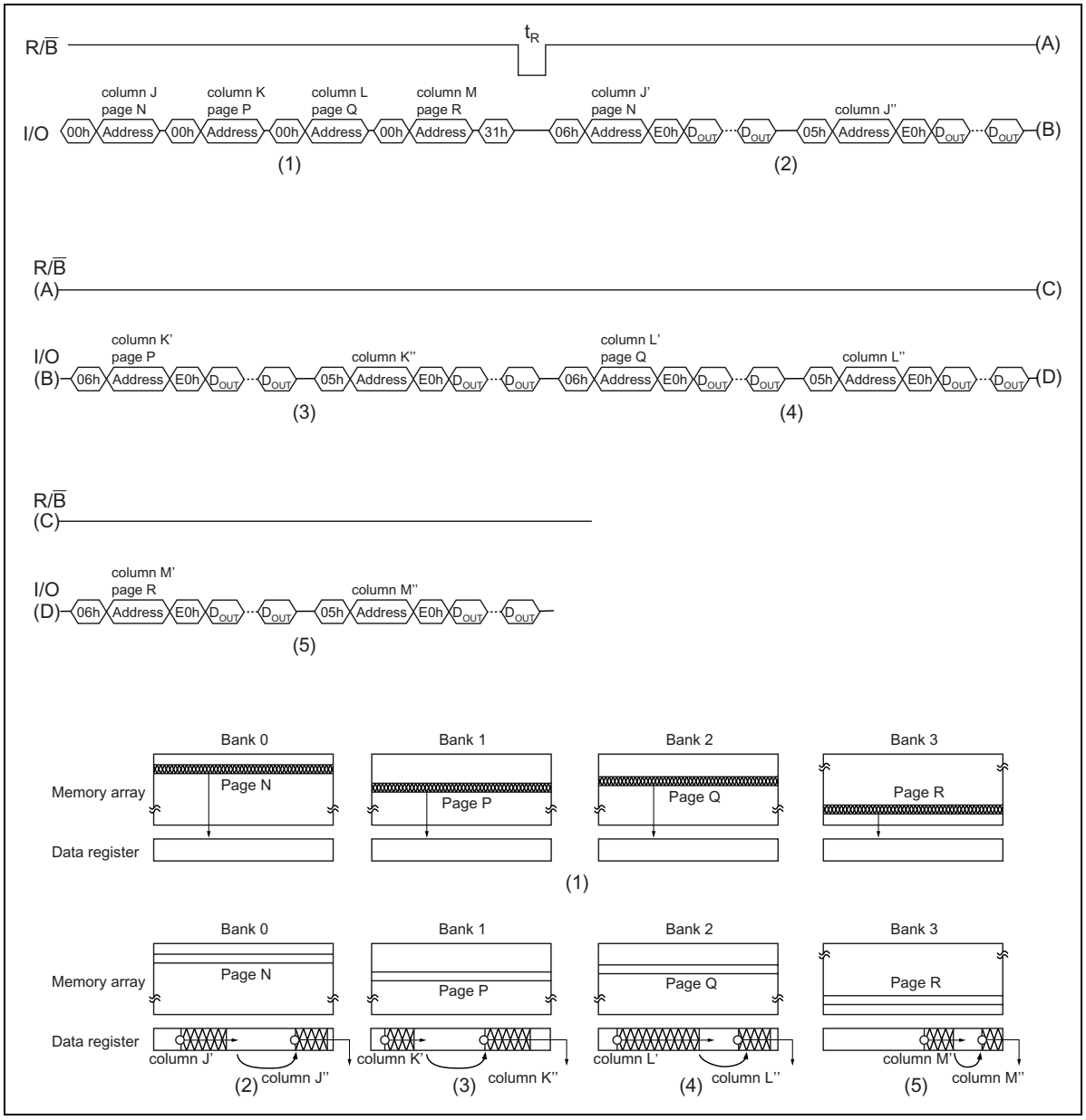
Multi Bank Read operation enables to read the data of any Page address in 4 bank. Writing 00h command with four address cycles can be specified to maximum 4 Bank. There is no restriction on an order of a Bank to specify.
Page address specified later becomes effective when it is specified twice in the same Bank.
The device become Ready state at rising edge of $\overline{WE}$ after writing 31h command with specifying address and the data transfer from the memory array to the data register is started.
After it becomes Ready state, it executes specifying a bank for read and column address for starting read by writing 06h and E0h command with four address cycles. After that the device output the data serially from column address which is specified by clocking $\overline{RE}$. It is possible to specify any bank for read and to read the data which is transferred to the data register repeatedly.



Note: 1. (2) (3) (4) (5): repeatable

Multi Bank Read with Random Data Output

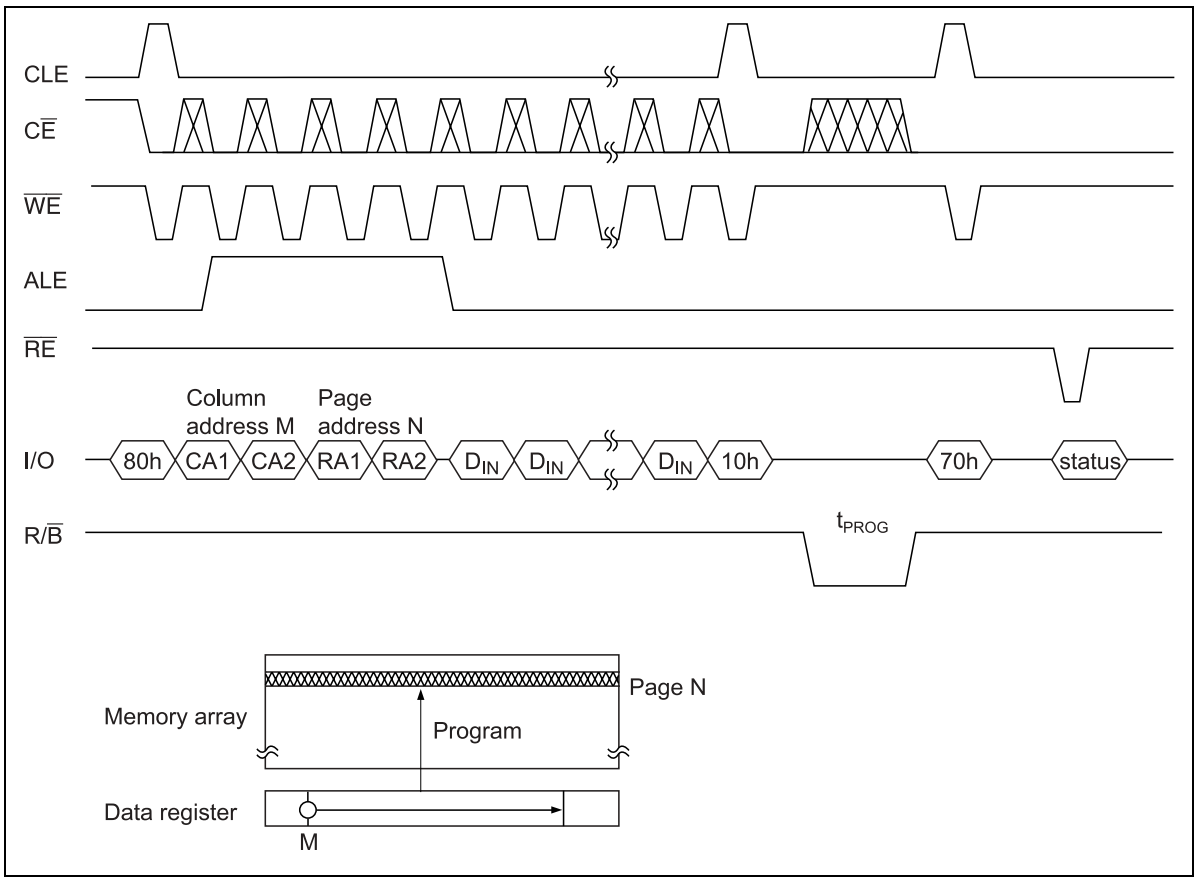
The data can be read out setting column address freely on the way to the read operation of Page address data in each Bank in Multi Bank Read operation. It is possible to read out the data by writing 05h and E0h command with two column address cycles. There is no restriction to specify any column address and it is possible to specify it including same one in the same page address many times.



Note: 1. (2) (3) (4) (5): repeatable

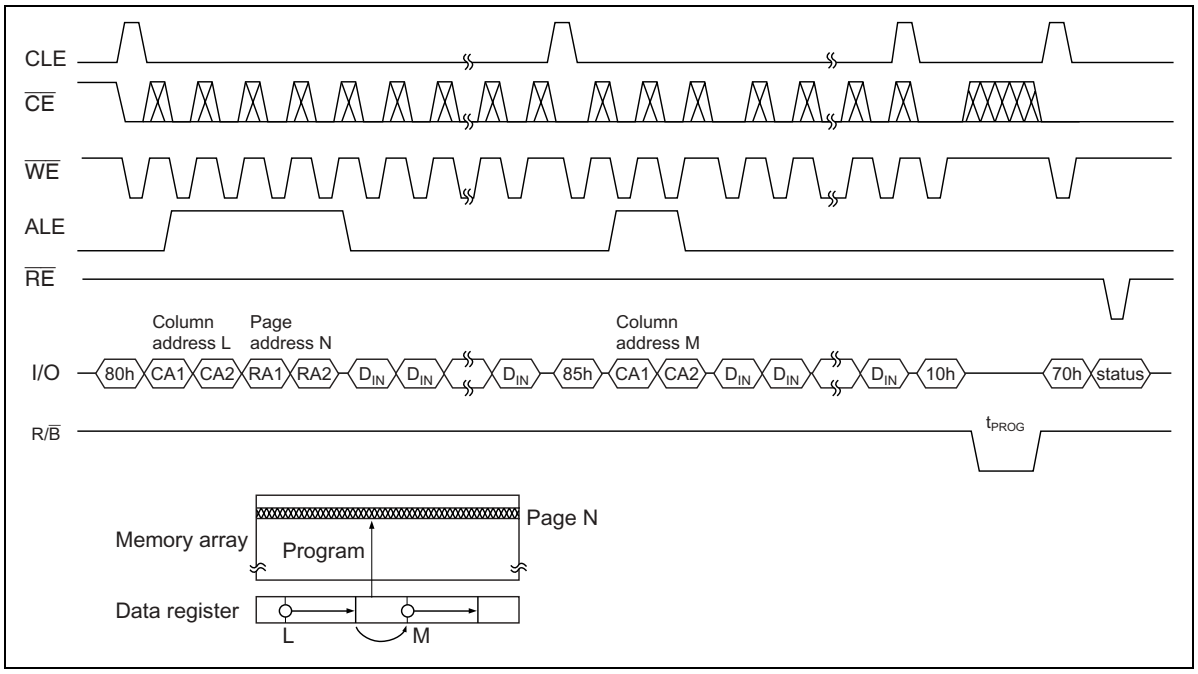
Page Program

Page program operation enables to write the data into one Page address. The data is stored into the data register after writing 80h command with four address input (Column address, Page address) and data input. It is also stored serially from column address which is input and then automatic program operation starts after writing 10h command (Program command). Program operation must be executed to a Page address which the data is erased. A number of additional program in the same Page address is maximum 8 times.



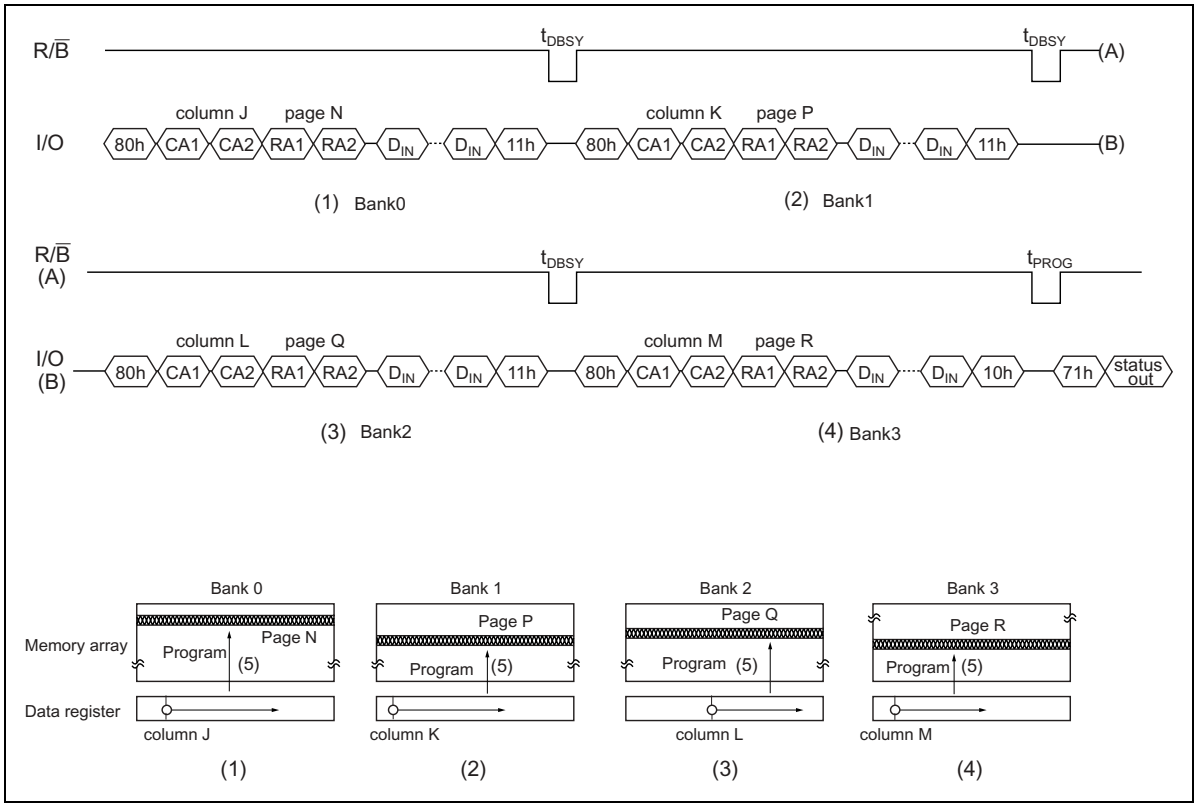
Page Program Random Data input in a Page

This operation enables to input the program data in the Page address randomly writing 85h command with two column address input on the way to the program operation in the Page program mode.
It can input the data by specifying a column address in the same page which you want to program the data using this mode.
After completion of the data input, program it to the specified column address is executed automatically by writing 10h command (Program start command). Program operation must be executed to a Page address which the data is erased.
A number of additional program in the same Page address is maximum 8 times.
The data of 1 byte or more need to be input when it is in random data input.



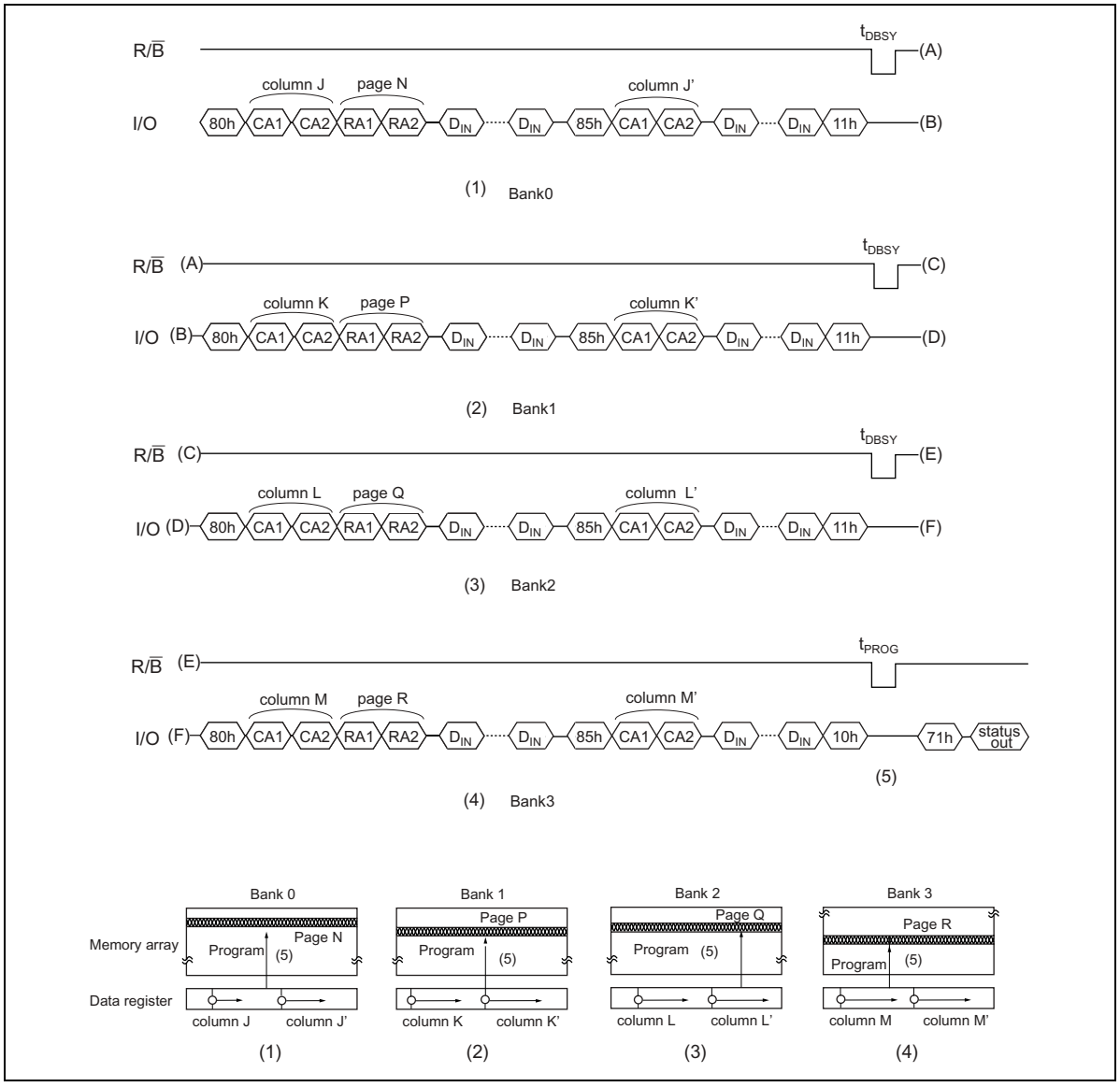
Multi Bank Page Program

It is possible to program the data to any one page address in each bank simultaneously since this device adopts 4 bank structure. The bank to be programmed the data is chosen from 1 bank to maximum 4 bank. Address and data for next bank can be input consecutively by writing 11h command (dummy command) after writing 80h command with column and page address, data as well as usual page program. Program operation to several banks specified automatically are executed simultaneously by writing 10h command (program start command) after data input to the maximum 4 bank completes.



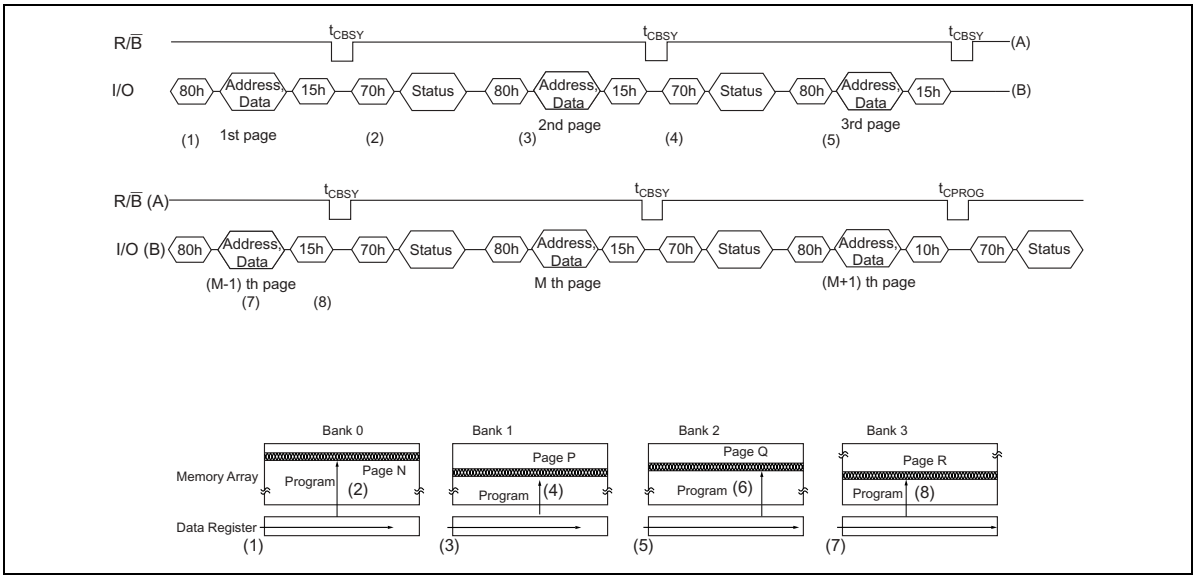
Multi Bank Page Program with Random Data Input in a Page

This mode enables to input program data specifying an address in a page which the data is programmed when it is in Multi Bank Page Program operation. The data can be input serially by writing 85h command with column address to on the way to the data input to the page address to be programmed as well as random data input in page mode. After the data input, program and address/data input to next bank is executed by writing 11h command (dummy command) and then 80h command as well as Multi Bank Page Program.
Program operation to several banks specified automatically is executed simultaneously by writing 10h command (program start command) after the completion of data input to the final bank.
Address of the random data can be set in every page for program freely.



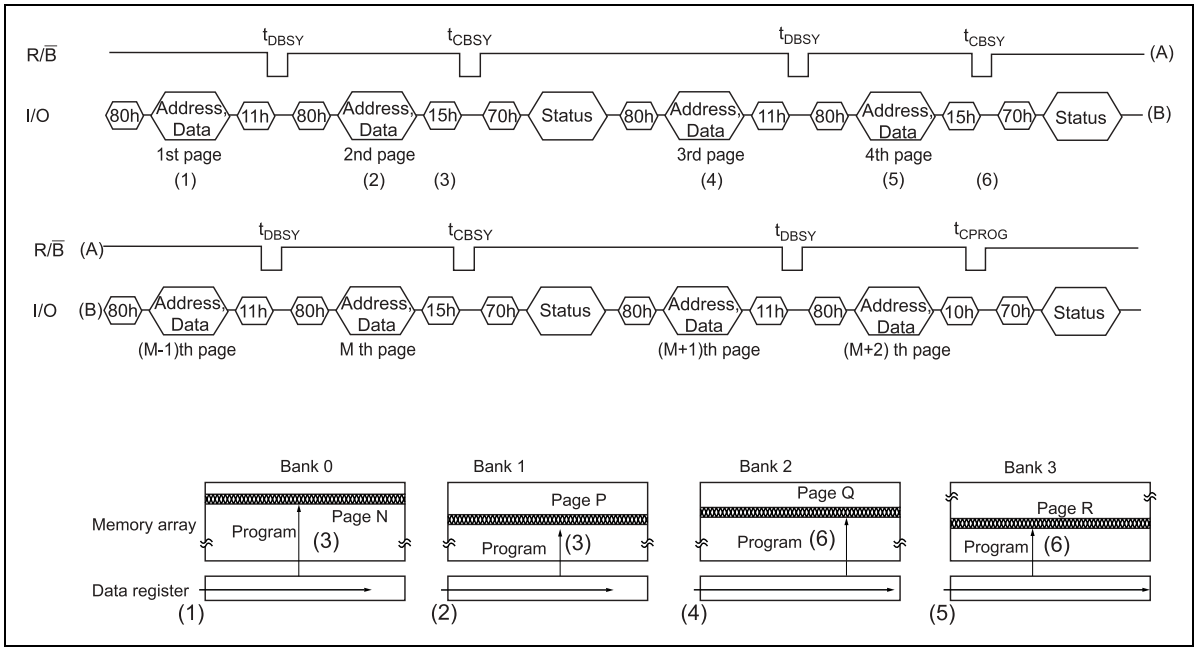
Cache Program

Cache program operation enables to use the data register of the bank which do not program as the cache register.
The program data for next page address is transferred to Flash memory from external data buffer by using the cache register while programming the primary data.
Setup for program starts after writing 15h command following 80h command and program address/data transfer.
After that the device is in the Busy state. The data register of the bank which do not program is cleared when program operation inside the device starts and then it is ready to receive the data of next page address.
In this case next page address must be different page address of the bank with one which programs just before.
It is prohibited to program the data to page address in same bank consecutively using cache program.
Next page address for program should specify one in different bank.
The data of next page address can be transferred to Flash memory by writing 80h command as well as the data transfer of the1st page address and then 15h command (program dummy command) input is required after program address/data input. It becomes Busy state until the program operation to the 1st page address completes and the data of data register is cleared. If the program operation to the 1st page address does not complete, it becomes Busy state until the data of data register except for one of the bank which programs next.
70h command is issued to find out the status in cache program operation after Ready/Busy becomes Ready.
The True Ready/Busy status (I/O5) in cache program becomes busy when CPU is active and shows that the internal program operation is in the process. The True Ready/Busy status (I/O6) should be verified to find out the program completion if 15h command is used for the last programming. Reset operation is required by writing FFh when program operation completes using 15h command and moves to the other operation except for cache program. Reset operation is not required if 10h command (program start command) is used for the last programming.



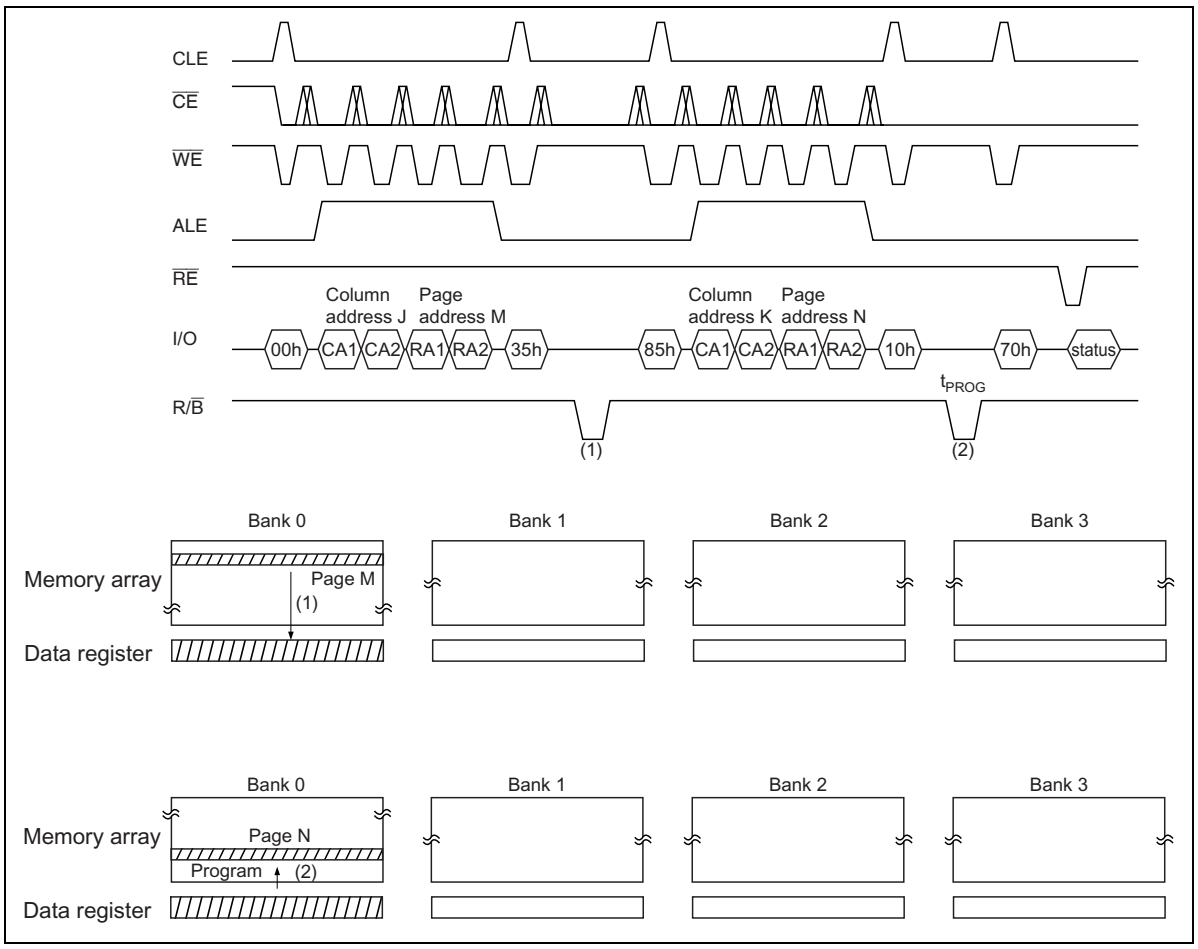
2page Cache Program

2 page cache program operation is available using both Multi Bank Program and Cache Program operation. It enables to input the program data for the address of next bank consecutively by writing 11h command (dummy command) following 80h command and program address/data input. Setup for program starts by writing 15h command after data input and then the device is in the Busy state (t_{CBSY}). The data registers of two banks which do not program are cleared when program operation inside the device starts and then it is ready to receive the data of next two page address.
In this case next two page address must be different page address of the bank with ones which programs just before.



Copy Back Program

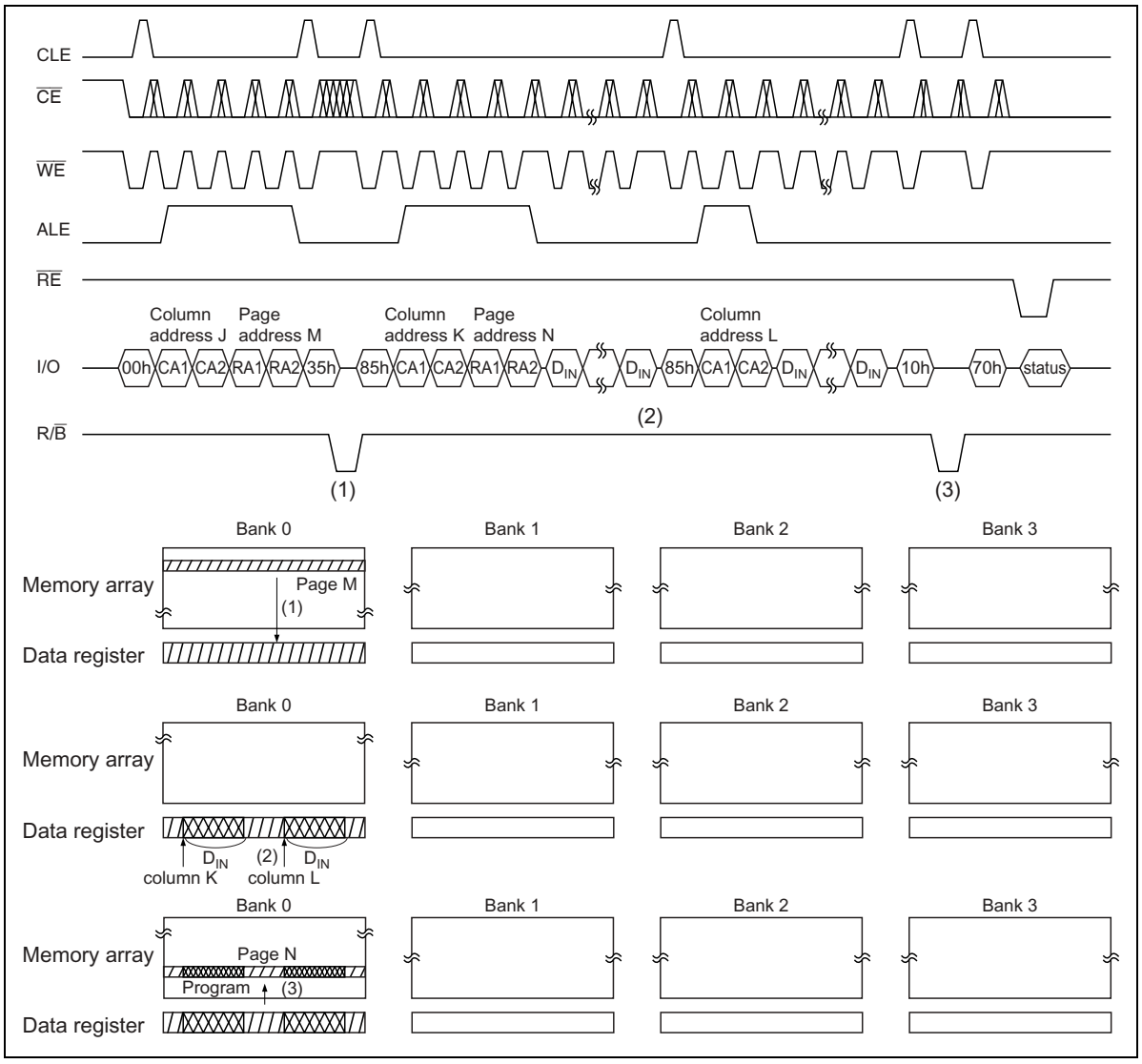
Copy Back Program operation enables to copy the data to different page address of same bank without taking it to external data register. The data transfer to the data register is started to copy memory array data of 1 page address writing 35h command following 00h command and address input with 4 cycles. Then copy of the data is started by writing 10h command following 85h command and address with 4 cycles for post-copy. Address for post-copy must be chosen page address which has erased (FFh).



Note: 1. Post copy address must be specified one in same bank.

Copy Back Program with Random Data Input In a Page

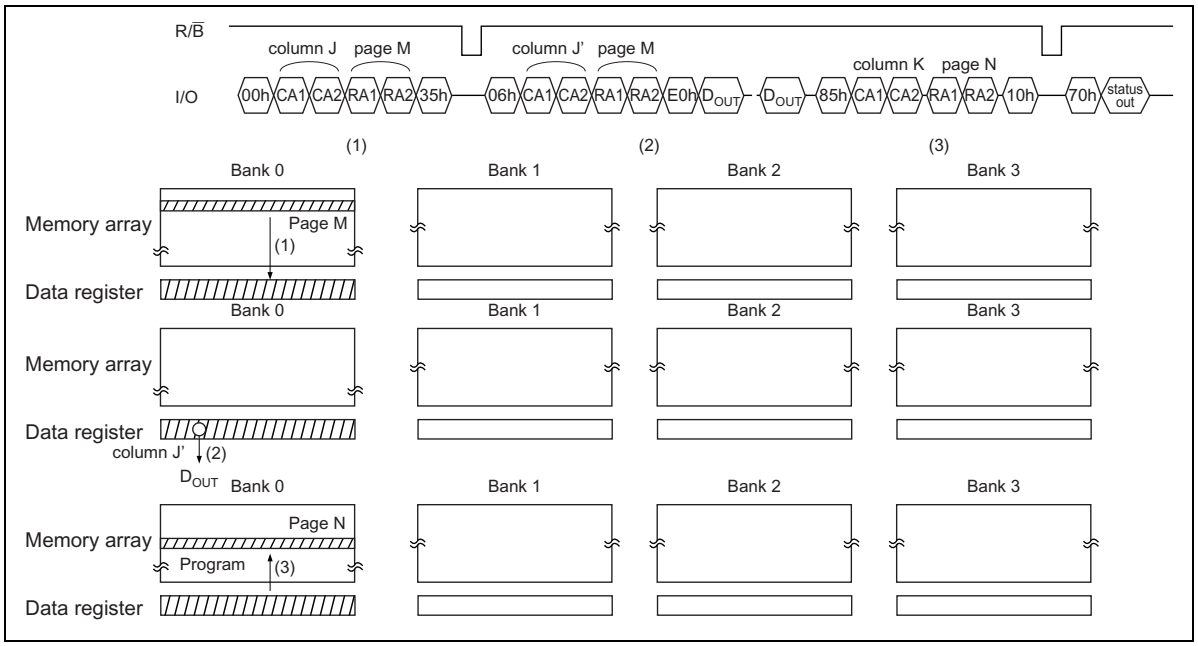
Source copy data which has transferred to the data register can be updated when copy back program operation is executed.
Memory array data which has taken out to the data register is updated to the input data after storing source copy data to the data register and inputting the data following 85h command and 4 address input with 4 cycles. 1 byte data or more must be input when random data input is executed. Program to post-copy page address is executed by writing 10h command after data input.
Address for post-copy must be chosen page address which has erased (FFh).



Note: 1. Post copy address must be specified one in same bank.

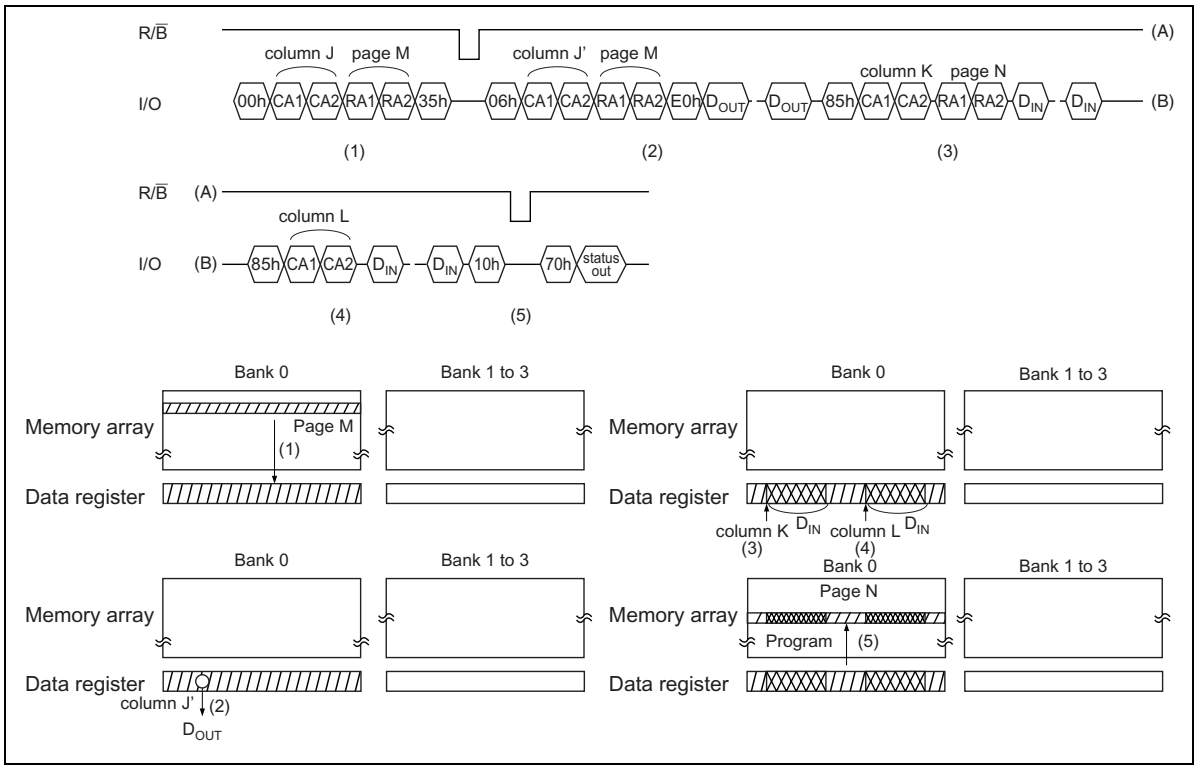
Copy Back Program with Data Output

When copy back program operation is executed, it is possible to confirm the source copy data outputting one which has transferred to the data register to external. It is possible to output the source copy data after storing it to the data register and inputting E0h command following 06h command and address input with 4 cycles. Program to post-copy page address is executed by writing 10h command following 85h command and post copy address input with 4 cycles after data output. Address for post-copy must be chosen page address which has erased (FFh). Copy data can be updated after post copy address input with 4 cycles and the data input.



Note: 1. Post copy address must be specified one in same bank.

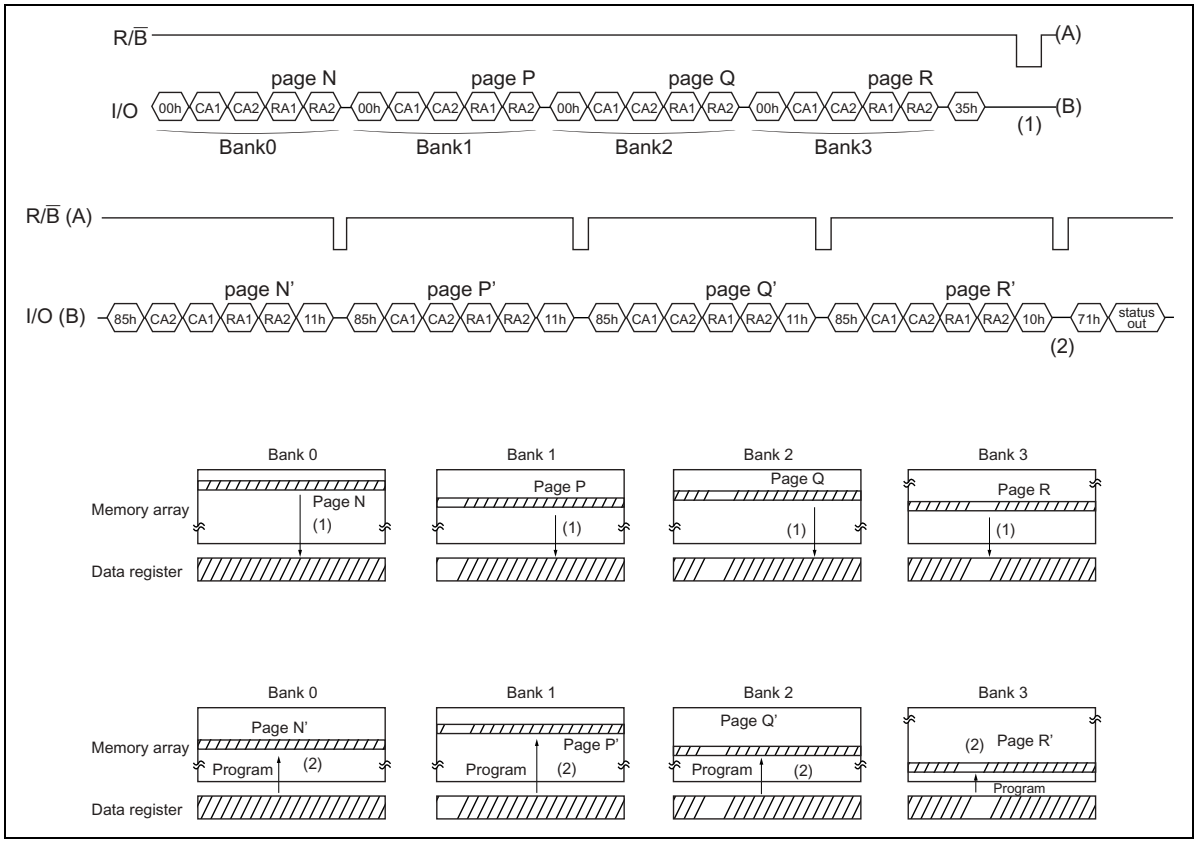
Copy Back Program with Data Output and Random Data Input in a Page



Note: 1. Post copy address must be specified one in same bank.

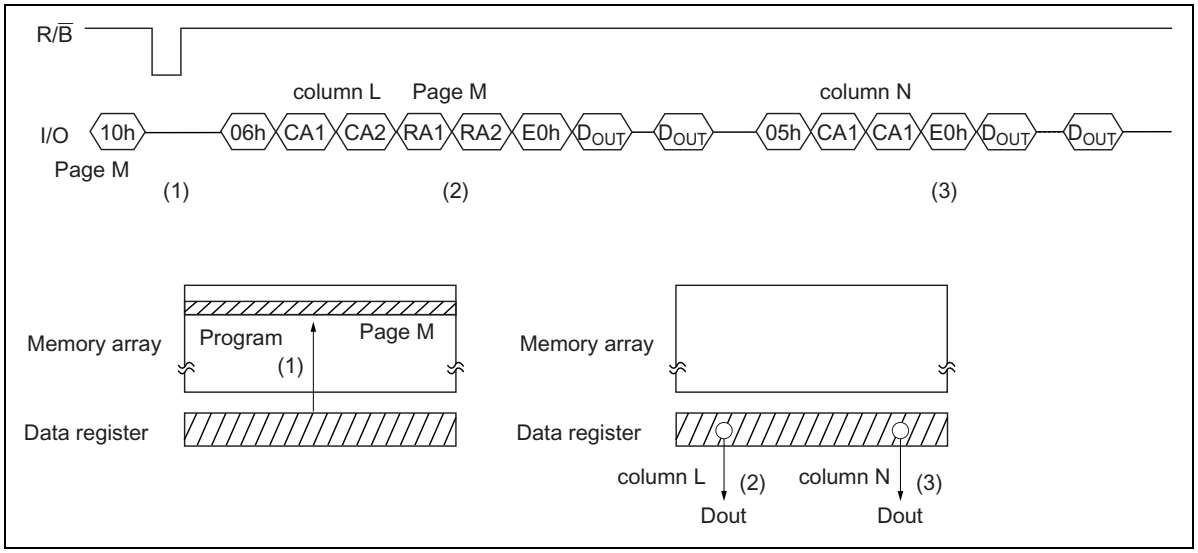
Multi Bank Copy Back Program

Multi Bank Copy Back Program enables to execute copy back program to a multiple bank simultaneously. The data is transferred to the data register from memory array simultaneously by writing 35h command after specifying post copy address consecutively. Data read and update can be executed as well as copy back program.



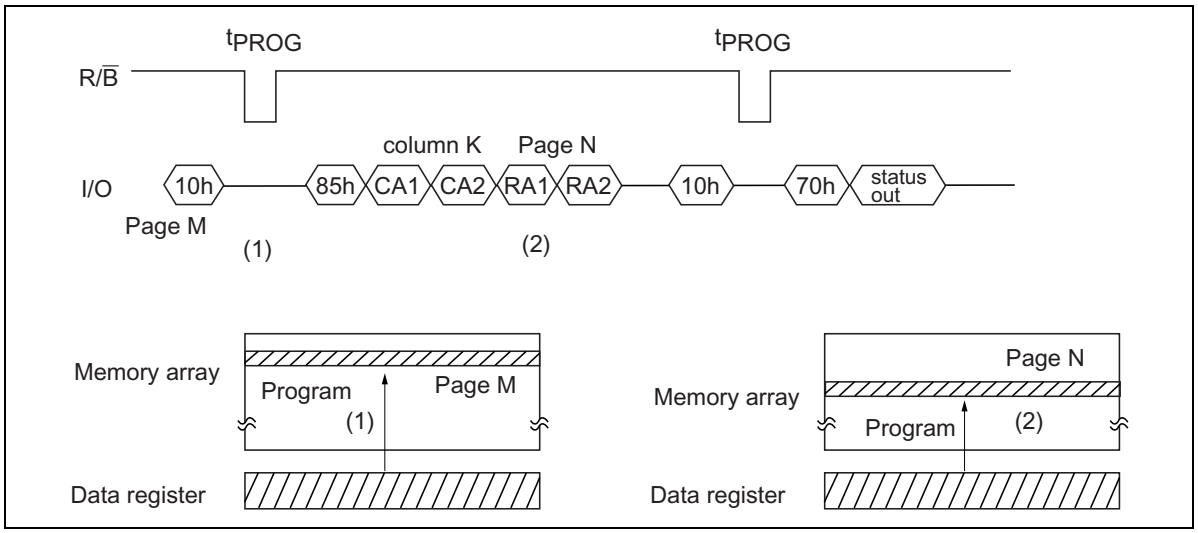
Data Recovery Read

Data recovery read enables to output the data itself which is transferred from external after program completion.
It is possible to read out the data which is programmed by writing E0h command following 06h command and read address input with 4 cycles. It is also possible to read out the data of any column address in same page address by writing E0h command following 05h command and column address input with 2 cycles on the way to outputting the data by clocking $\overline{RE}$.

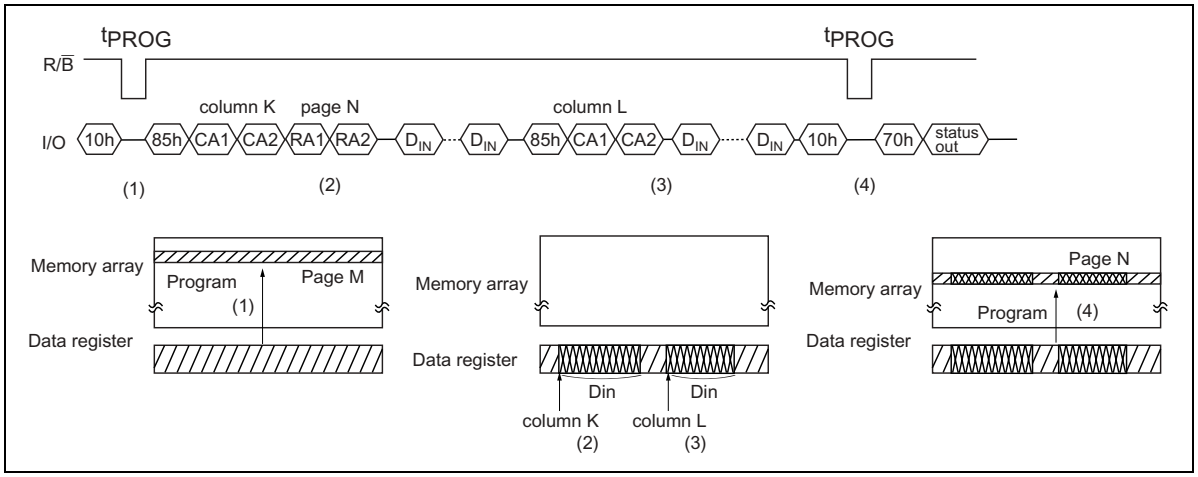


Data Recovery Program

Data recovery program enables to re-program the program data itself which is transferred from external to different page address in same bank. Program to newly specified page address is executed by writing 10h command following 85h command and address for re-programming with 4 cycles as well as copy back program. Same page address cannot be chosen during this operation.
It is possible to update the re-program data by inputting the data after specifying address for re-programming.
Address for re-programming must be chosen page address which has erased (FFh).



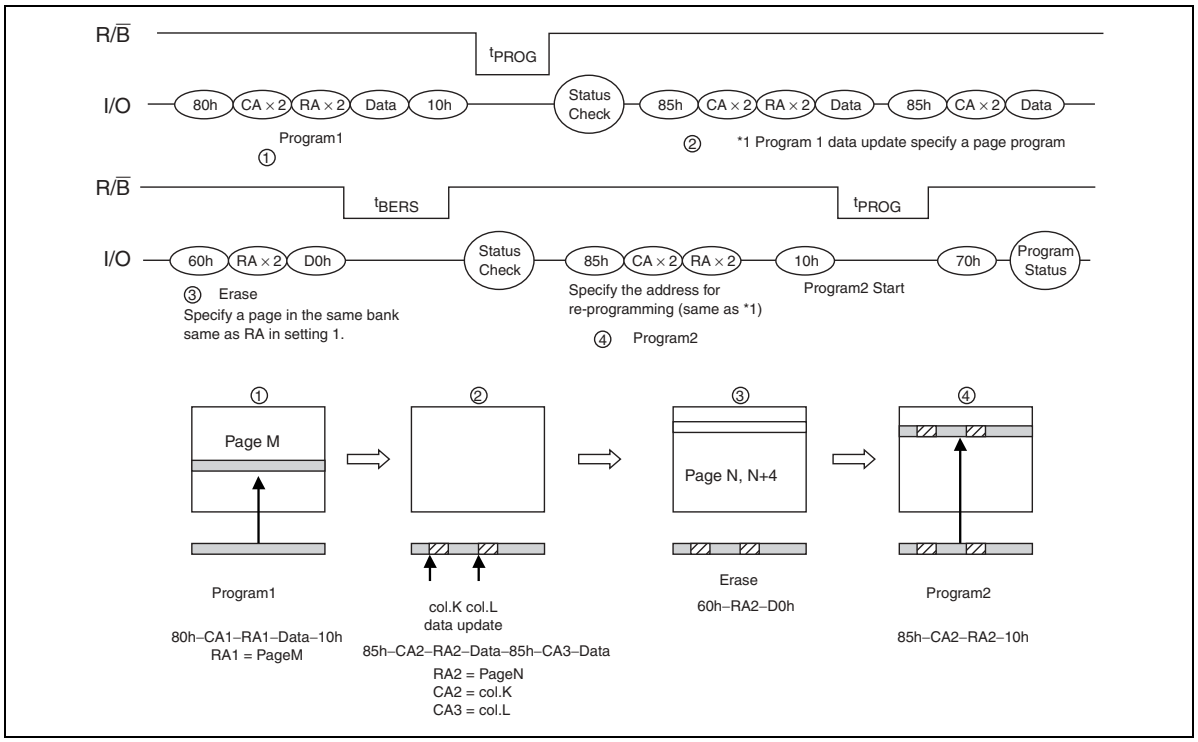
Note: 1. Page M and Page N are different page address.



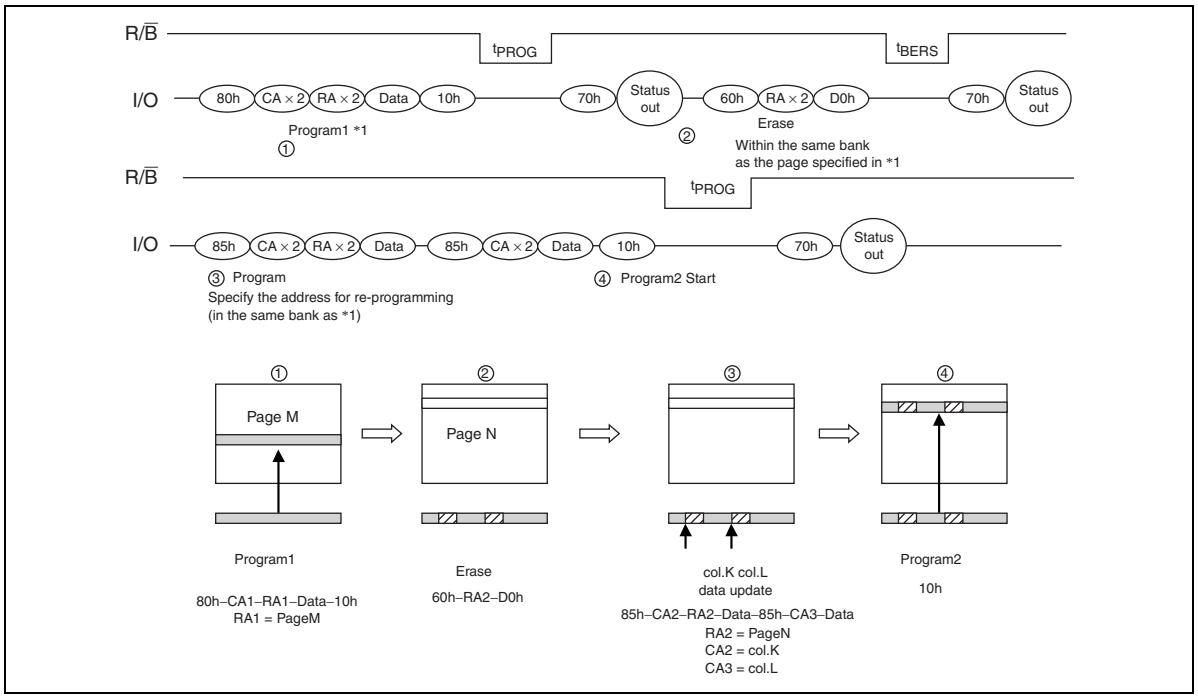
Note: 1. Page M and Page N are different page address.

It is possible to combine erasing the data of the block with re-programming, as shown below, in the data recovery program operation.

To program, update the data next, then erase, and then re-programming.



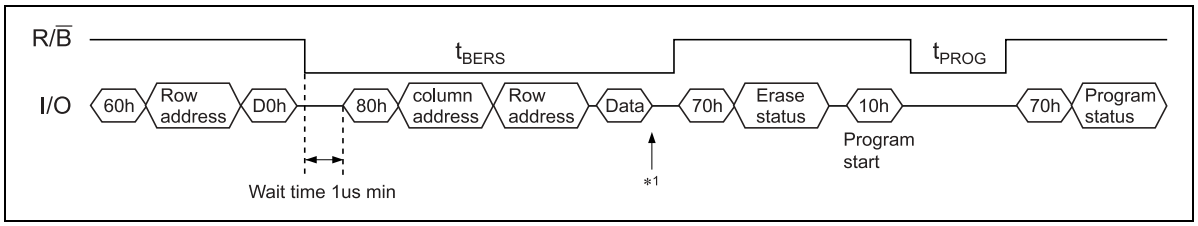
To program, erase next, then update the data, and then re-programming.



Program Data Input in Erase Busy

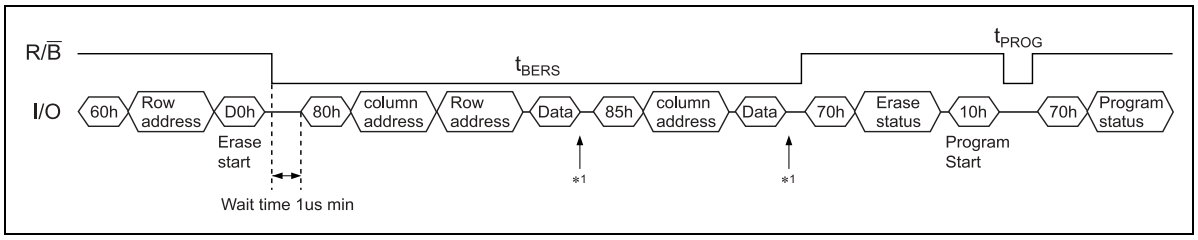
Program Data input in Erase Busy enables to program the data of any page address during busy status in erase operation.
It is possible to program the data in both block erase mode and multi bank block erase mode if they are in busy state.
There is no restriction between page address for programming and block for erase.
It needs 1µs wait time after the erase status becomes busy to write 80h command for program address and data input.
It can confirm the status by writing 70h or 71h command after program data input.
The input data is possible to input in both single bank and multi bank mode and corresponds to the data input mode specifying column address in same page address. It needs to keep 4µs or more from writing 11h command to writing 80h command when the data to a multiple bank is programmed. 10h command (program start command) must be issued after completion of erase operation.

Program data input in single bank



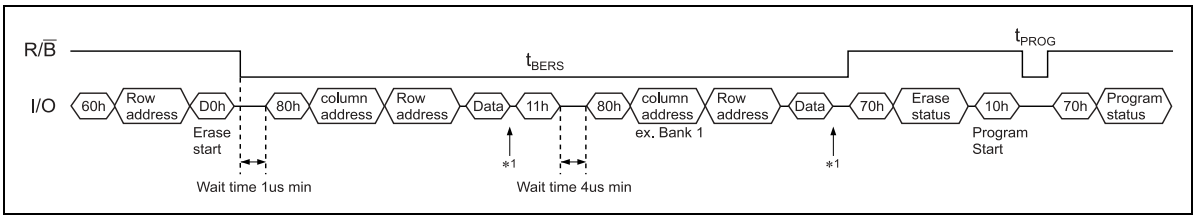
Note: 1. Status command available

Program data input with random data mode in single bank mode



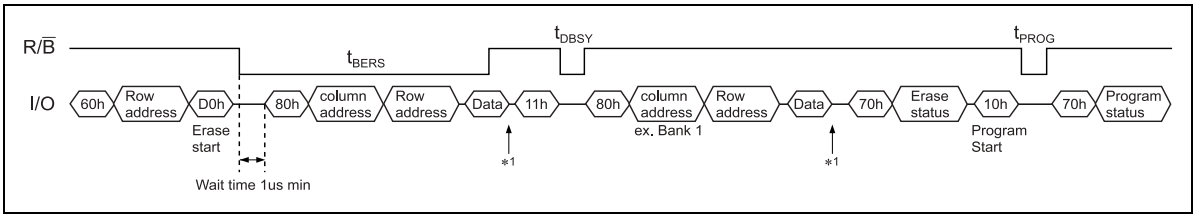
Note: 1. Status command available

Program data input in multi bank program mode (In case of completing data input during busy status)



Note: 1. Status command available

Program data input in multi bank program mode (In case of not completing data input during busy status)

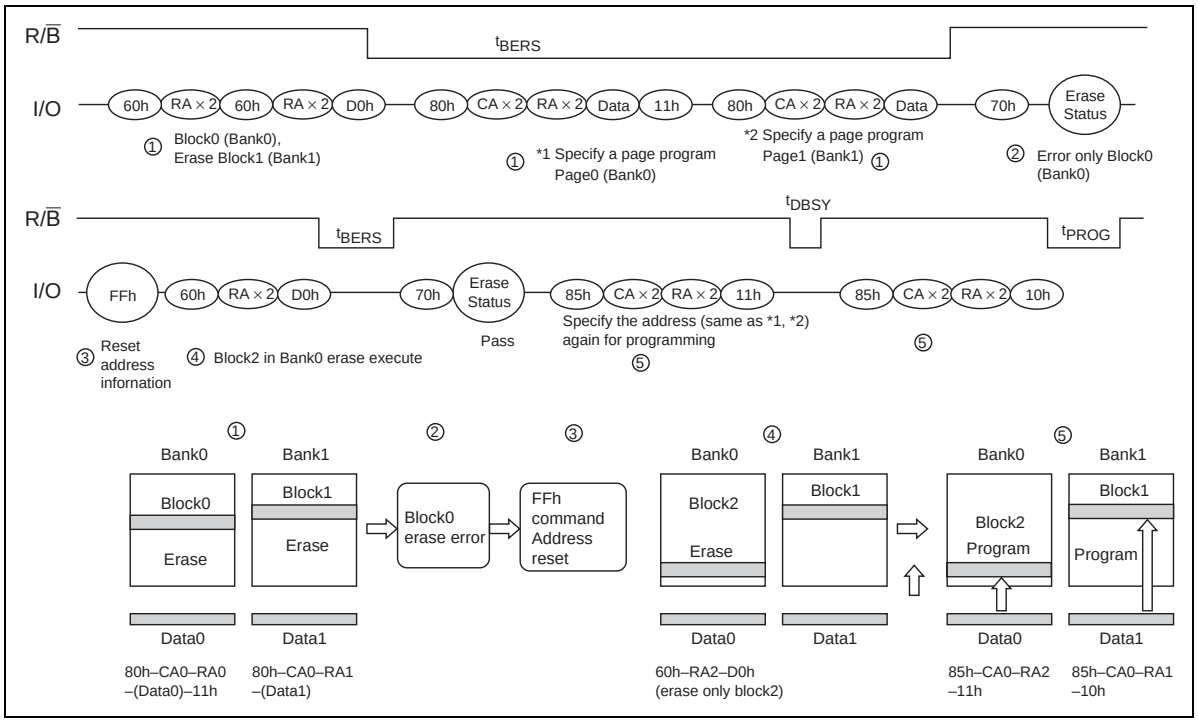


Note: 1. Status command available

The correspondence when the erase error occurred in Program Data Input in Erase Busy mode.

In the Program Data Input in Erase Busy mode, after an erase error occurred in one block at a two-blocks simultaneous erase operation, a certain operation is needed in a particular case. In case of an erase operation of one block in the same bank as the error-occurred block, the reset command FFh is needed just before, as shown in Figure 1.
Otherwise, an illegal two-blocks erase operation will be executed, because the address data of two pages to program remains.
After the one-block erase operation succeed, it is possible to program by specifying the address to program again with the command 85h, because the data to be programmed stored in the buffer is maintained.

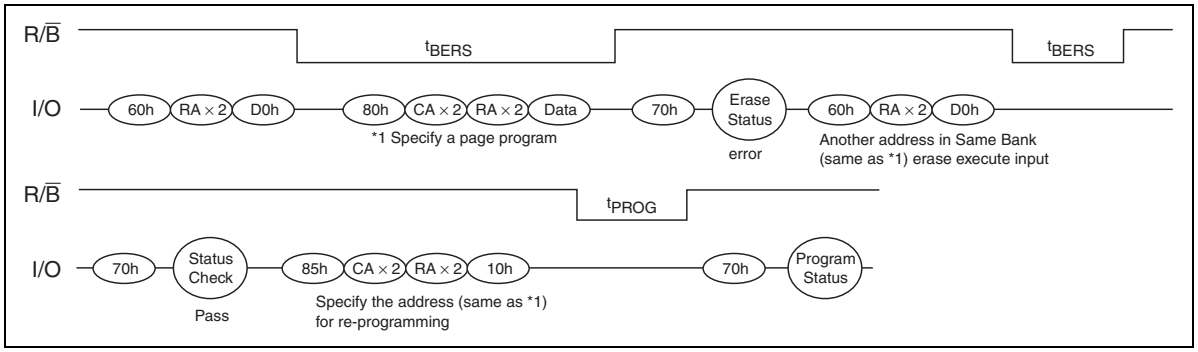
Program Data Input in Erase Busy (recommend pattern when error occurred) Multi Bank Mode



It is not necessary to reset by command FFh, when transmit the writing data in erase block and 1 page in same bank, and execute writing during erasing 1 block data, or erasing error occurs and erasing another block in same bank. But in this case, as shown in following figure, it is necessary to specify the address for re-programming, after erasing another block address.

Write address specifying it by command 85h at the address for re-programming in the same bank, when writing it as shown in following figure.

Program Data Input in Erase Busy (recommend pattern when error occurred) Single Bank Mode



Block Erase

Erase operation for one block which is consisted of 2 page can be executed. One block is consisted of pageN and page(N+4)
(Ex: page0 and page4, page1 and page5).

Input page address (A14 = V_{IL}) in lower side, when erase block address input.

Multi Block Erase

Erase operation for one block in maximum 4 bank is executed simultaneously. Any block in a bank can be chosen. Input page address (A14 = V_{IL}) in lower side, when erase block address input.

Page mode Erase Verify

Whether any one page address is erased or not is verified in this mode. Verification starts internally inside the device after writing D2h command after 60h command and row address input. It can be verified whether the page address is erased or not after by writing 70h command (status read command) after it becomes ready.

Block mode Erase Verify

Whether any one block is erased or not is verified in this mode. Verification starts internally inside the device after writing D3h command after 60h command and row address input. It can be verified whether the block is erased or not after by writing 70h command (status read command) after it becomes ready.

Multi Bank Page mode Erase Verify

Page mode erase verify for each page in maximum 4bank is executed. It can be verified whether page address in each bank is erased or not by writing 71h command (status read command) after it becomes ready.

Multi Bank Block mode Erase Verify

Block mode erase verify for each block in maximum 4bank is executed. It can be verified whether the block in each bank is erased or not by writing 71h command (status read command) after it becomes ready.

Read ID

ID code can be read out by inputting the address (00h) after writing 90h command.
Manufacturer code (07h) and Device code (01h) can be read out serially by clocking $\overline{RE}$.

Power on Auto Read

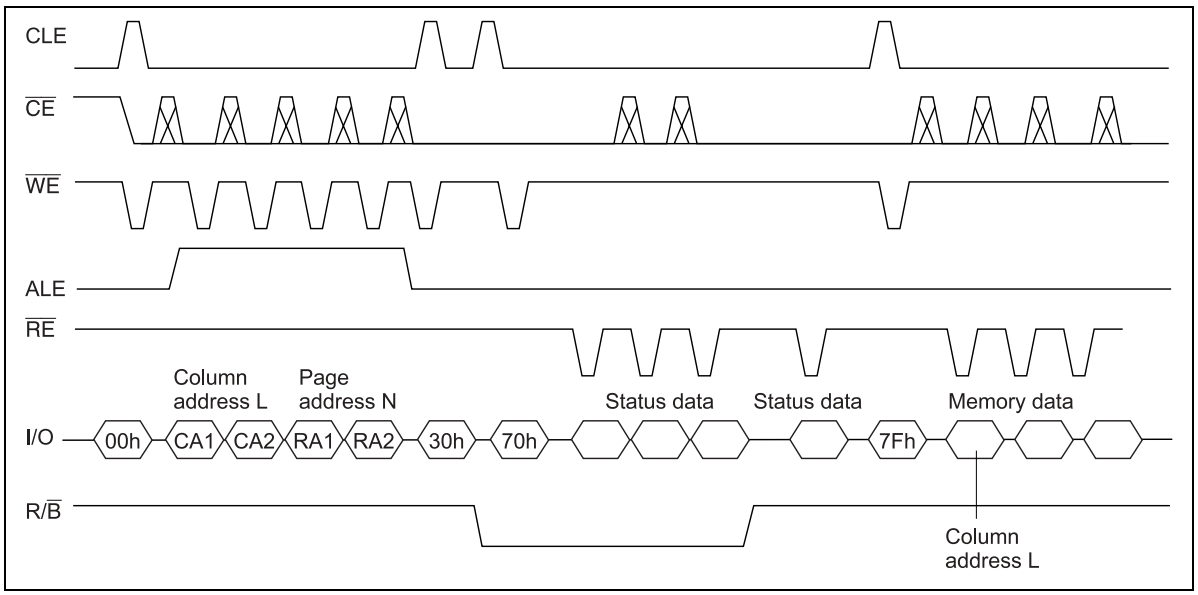
The data of the lowest page address can be read out serially without command and address input after power is on.
Power on auto read mode is activated when V_{CC} reaches about 2.7V. It is enabled only when PRE pin is tied to V_{CC}.
PRE pin must be connected to V_{CC} when using power on auto read and V_{SS} when not using it.

After power on auto read is executed, reset operation is required by reading out 1 page (2112 byte) data or writing FFh command.

Note: Please contact Renesas Technology's sales office before using this mode.

Status Read at Read mode

The content of status register can be read out writing 70h command (status read command) and by clocking $\overline{RE}$ in read operation. The data of memory array cannot be read out even by clocking $\overline{RE}$ since status read mode is set after the device becomes ready. 7Fh command needs to be written in case of releasing status read mode in read operation.
The data of memory array can be read out without address input in this operation.

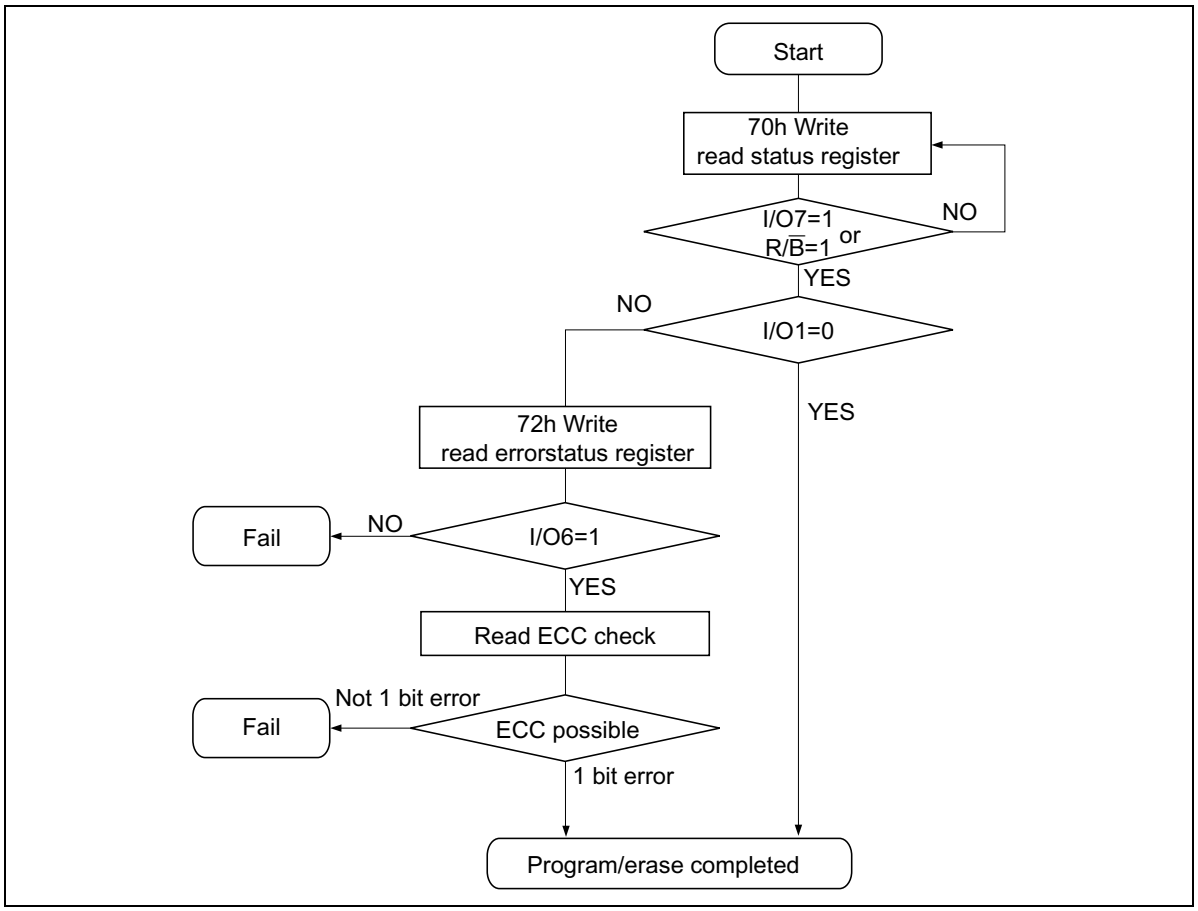


Operation status of status register

Operation status can be output by status read.

Command	Output
70h	Single bank operation status
71h	Multi bank operation status
72h	Single bank operation error status
73h	Multi bank operation bank0 error status
74h	Multi bank operation bank1 error status
75h	Multi bank operation bank2 error status
76h	Multi bank operation bank3 error status

Status Register check flow (single bank operation)



70h command status in single bank operation

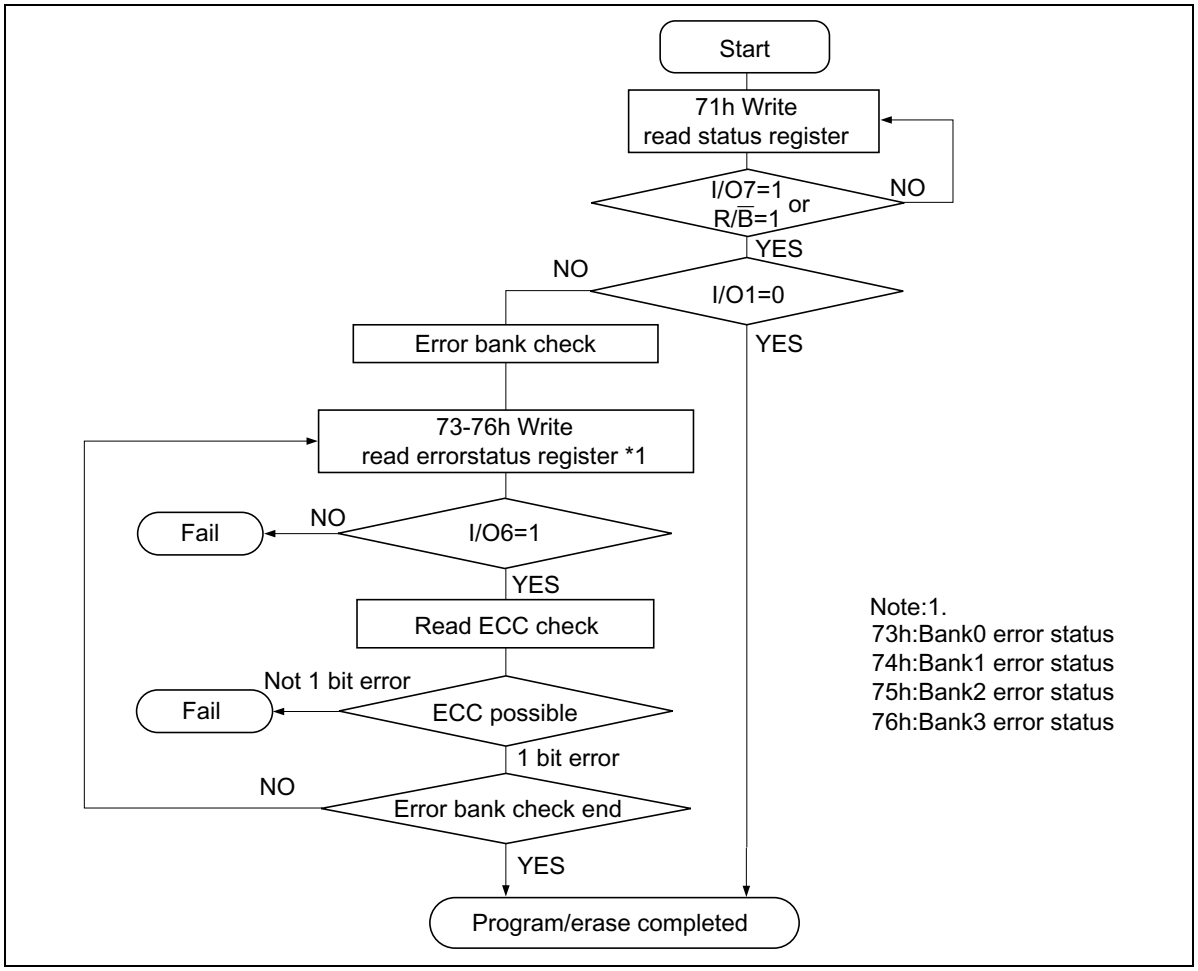
	status		
	Program/Erase	**Cache Program**	**Output**
I/O 8	Write protect	Write protect	Protect: 0 Not Protect: 1
I/O 7	Ready/$\overline{\text{Busy}}$	Ready/Busy	Ready: 1 Busy: 0
I/O 6	Ready/$\overline{\text{Busy}}$	True Ready/$\overline{\text{Busy}}$*[1]	Ready: 1 Busy: 0
I/O 5	Not Used	Not Used	0
I/O 4	Not Used	Not Used	0
I/O 3	Not Used	Not Used	0
I/O 2	Not Used	Pass/Fail (N-1)	0 / Pass: 0 Fail: 1 (cache program)
I/O 1	Pass/Fail	Pass/Fail (N)	Pass: 0 Fail: 1

Note: 1. True Ready/$\overline{\text{Busy}}$ shows Ready/$\overline{\text{Busy}}$ status of CPU
(R/$\overline{\text{B}}$ output status is same as I/O7).

72h command status in single bank operation

	status	Output
I/O 8	Write protect	Protect: 0 Not Protect: 1
I/O 7	Ready/$\overline{\text{Busy}}$	Ready: 1 Busy: 0
I/O 6	Program/Erase ECC check	Ecc available: 1 Ecc Not available: 0
I/O 5	Erase check	Pass: 0 Fail: 1
I/O 4	Program check	Pass: 0 Fail: 1
I/O 3	Not Used	0
I/O 2	Not Used	0
I/O 1	Pass/Fail	Pass: 0 Fail: 1

Status Register check flow (Multi bank program/erase)



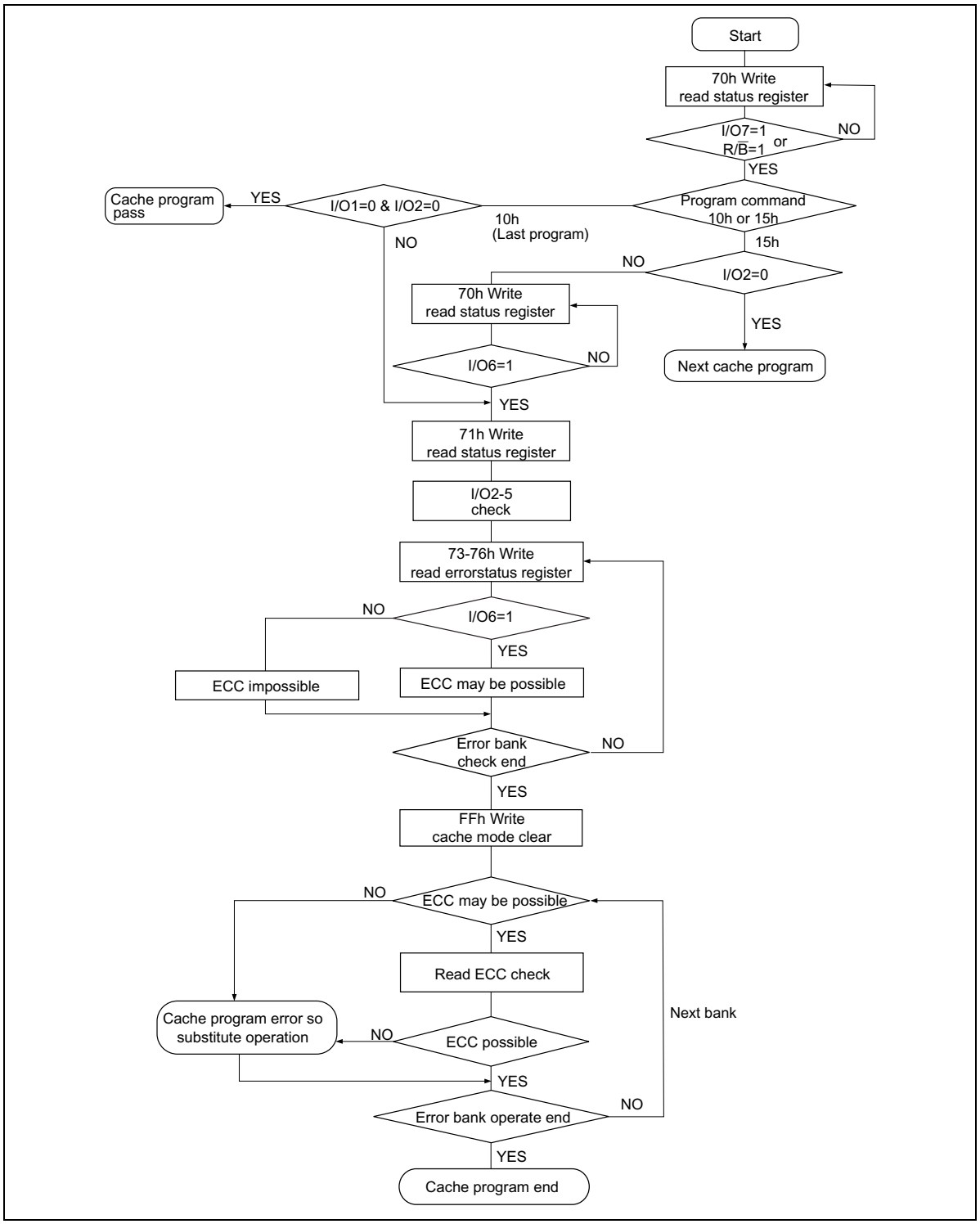
71h Command Status in Multi Bank Operation

	status	Output
I/O 8	Write protect	Protect: 0 Not Protect: 1
I/O 7	Ready/$\overline{\text{Busy}}$	Ready: 1 Busy: 0
I/O 6	Ready/$\overline{\text{Busy}}$	Ready: 1 Busy: 0
I/O 5	Bank3 Pass/Fail	Pass: 0 Fail: 1
I/O 4	Bank2 Pass/Fail	Pass: 0 Fail: 1
I/O 3	Bank1 Pass/Fail	Pass: 0 Fail: 1
I/O 2	Bank0 Pass/Fail	Pass: 0 Fail: 1
I/O 1	All Pass/Fail	Pass: 0 Fail: 1

73h, 74h, 75h, 76h Command Status in Multi Bank Operation / Cache program / 2page cache program

	status	Output
I/O 8	Write protect	Protect: 0 Not Protect: 1
I/O 7	Ready/$\overline{\text{Busy}}$	Ready: 1 Busy: 0
I/O 6	Program/Erase ECC check	Ecc available: 1 Ecc Not available: 0
I/O 5	Erase check	Pass: 0 Fail: 1
I/O 4	Program check	Pass: 0 Fail: 1
I/O 3	Not Used	0 (Don't care)
I/O 2	Not Used	0 (Don't care)
I/O 1	Pass/Fail	Pass: 0 Fail: 1

Status Register check flow (Cache program operation)



Status Register (Cache program operation)

The status is output by writing 70h command in cache program / 2 page cache program operation.
I/O1, 2 which shows pass/fail and I/O6, 7 which shows Ready/$\overline{\text{Busy}}$ is output OR data of 2 page address which programs simultaneously. In other words, if either 2 page address is Busy status, I/O6 or I/O7 outputs "0". If either 2 page address fails, I/O1 or I/O2 outputs "1".
It verifies the status writing 70h command in cache program operation and verification of detail error code which page address fails in program is executed by writing 73h-76h command which output error content corresponding to bank address.
It can also verify the status writing 70h in 2 page cache program operation and if either 2 page address which programs simultaneously fails with program error, it outputs fail status. We recommend verifying page address writing 71h command.
If error occurs in (N-1) page address, error management of (N-1) page (taking the data to replacement page address) address needs to be executed after program completion of N page address.

70h command status in Cache program / 2page cache program operation

	status	**Output**
I/O 8	Write protect	Protect: 0 Not Protect: 1
I/O 7	Ready/$\overline{\text{Busy}}$	Ready: 1 Busy: 0
I/O 6	True Ready/$\overline{\text{Busy}}$*[1]	Ready: 1 Busy: 0
I/O 5	Not Used	0
I/O 4	Not Used	0
I/O 3	Not Used	0
I/O 2	Pass/Fail (N-1)	Pass: 0 Fail: 1
I/O 1	Pass/Fail (N)	Pass: 0 Fail: 1

Note: 1. True Ready/$\overline{\text{Busy}}$ shows Ready/$\overline{\text{Busy}}$ status of CPU.

71h command status in 2page cache program operation

	status	**Output**
I/O 8	Write protect	Protect: 0 Not Protect: 1
I/O 7	Ready/$\overline{\text{Busy}}$	Ready: 1 Busy: 0
I/O 6	Ready/$\overline{\text{Busy}}$	Ready: 1 Busy: 0
I/O 5	Bank3 Pass/Fail (N or N-1)	Pass: 0 Fail: 1
I/O 4	Bank2 Pass/Fail (N or N-1)	Pass: 0 Fail: 1
I/O 3	Bank1 Pass/Fail (N or N-1)	Pass: 0 Fail: 1
I/O 2	Bank0 Pass/Fail (N or N-1)	Pass: 0 Fail: 1
I/O 1	Pass/Fail (N or N-1)	Pass: 0 Fail: 1

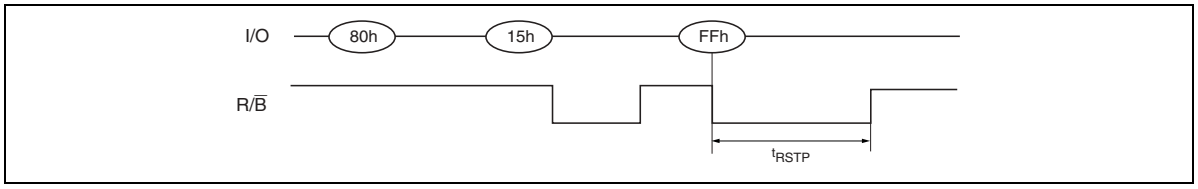
73h, 74h, 75h, 76h command status in Cache program / 2page cache program operation

	status	Output
I/O 8	Write protect	Protect: 0 Not Protect: 1
I/O 7	Ready/$\overline{\text{Busy}}$	Ready: 1 Busy: 0
I/O 6	Program/Erase ECC check (N or N-1)	Ecc available: 1 Ecc Not available: 0
I/O 5	Erase check (N or N-1)	Pass: 0 Fail: 1
I/O 4	Program check (N or N-1)	Pass: 0 Fail: 1
I/O 3	Not Used	0
I/O 2	Pass/Fail (N-1)	Pass: 0 Fail: 1
I/O 1	Pass/Fail (N)	Pass: 0 Fail: 1

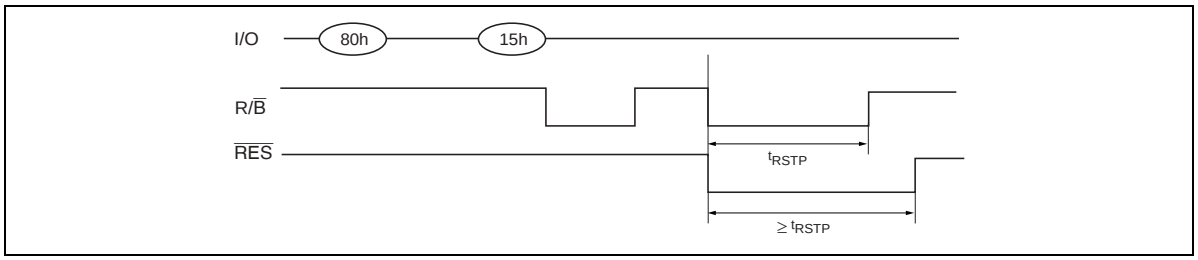
Reset operation

This device can enter standby mode interrupting each operation mode by writing FFh command (reset command) during each operation. Page address data during program operation, block data during erase operation are not guaranteed after completing reset operation.

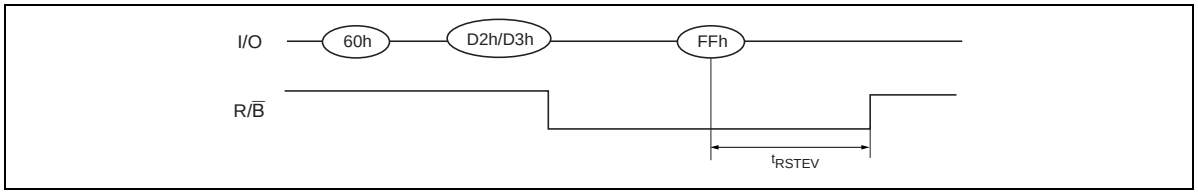
Reset operation in the Cache program (R/$\overline{B}$ = Ready, True R/$\overline{B}$ = Busy)



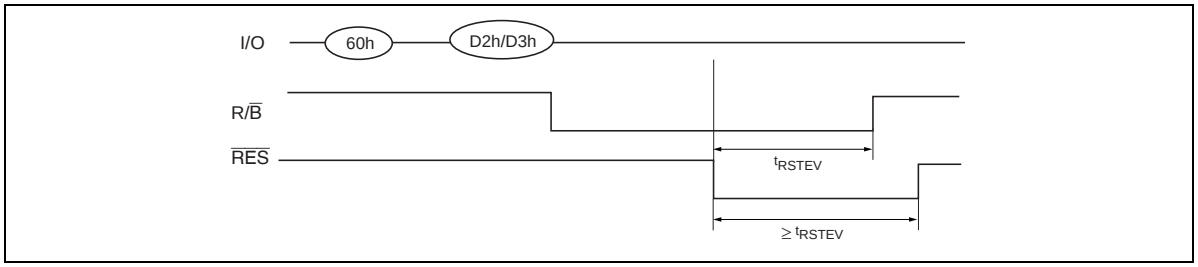
Reset operation in the Cache program (R/$\overline{B}$ = Ready, True R/$\overline{B}$ = Busy)



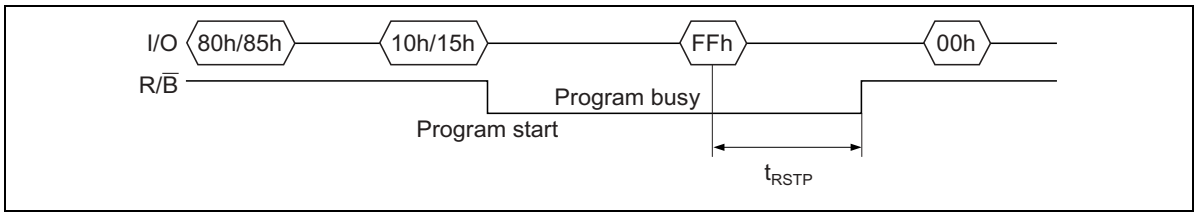
Reset operation in the Erase Verify



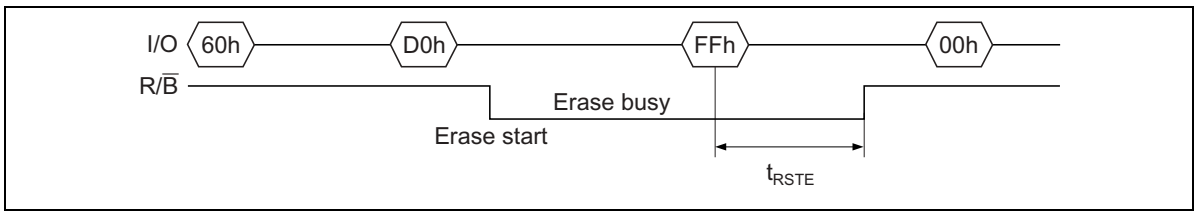
Reset operation in the Erase Verify



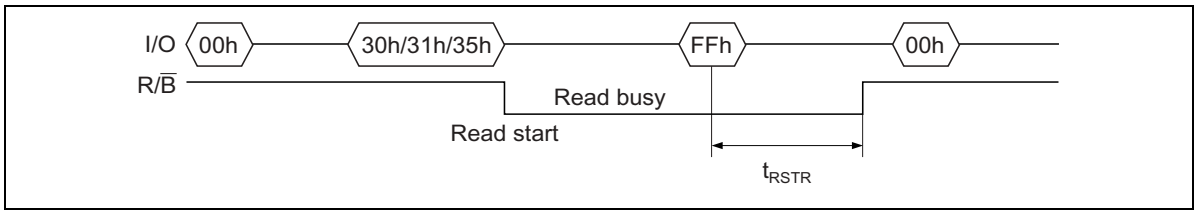
Reset operation in the Program



Reset operation in the Erase

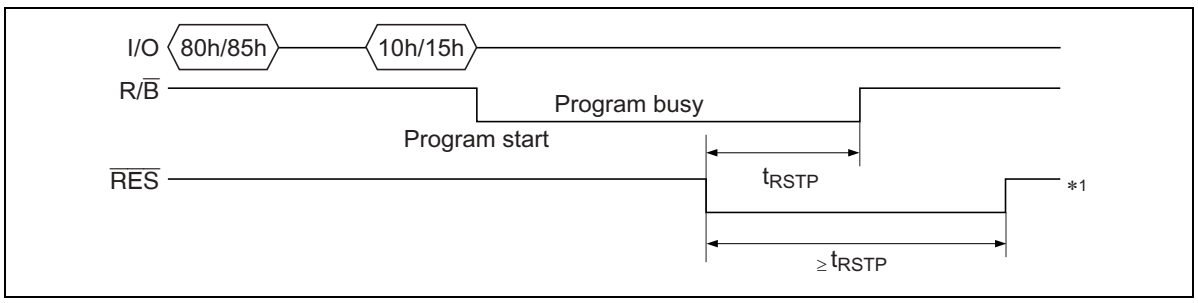


Reset operation in the Read



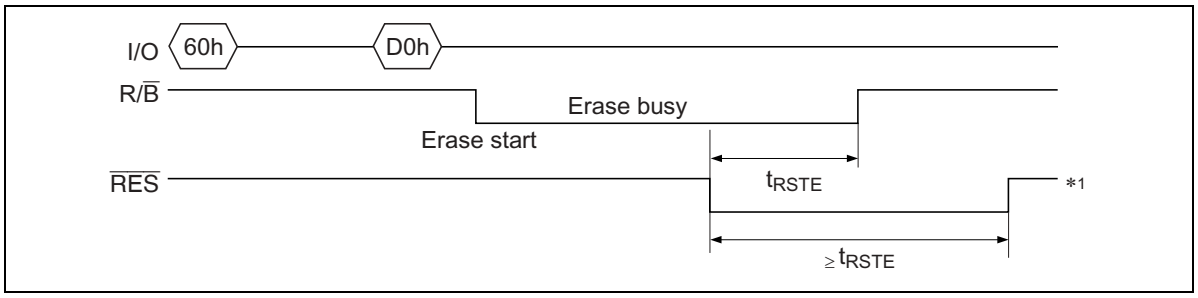
This device can enter deep standby mode interrupting each operation mode by making $\overline{RES}$ pin low during each operation.
Page address data during program operation, block data during erase operation are not guaranteed after completing reset operation.

Reset operation in the Program



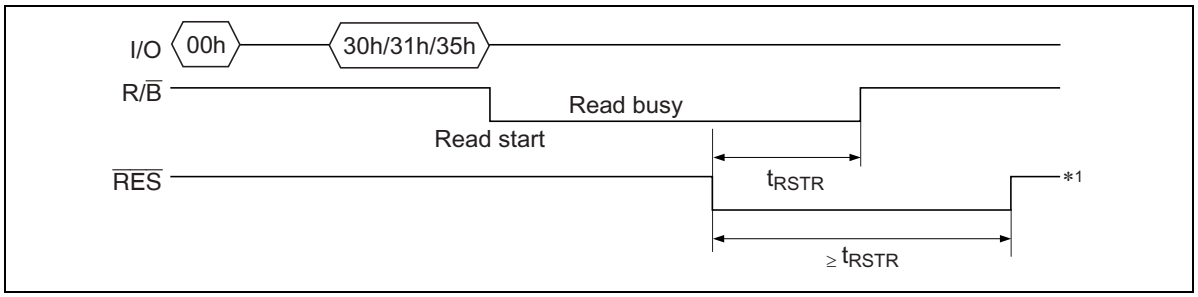
Note: 1. Power on sequence.

Reset operation in the Erase



Note: 1. Power on sequence.

Reset operation in the Read

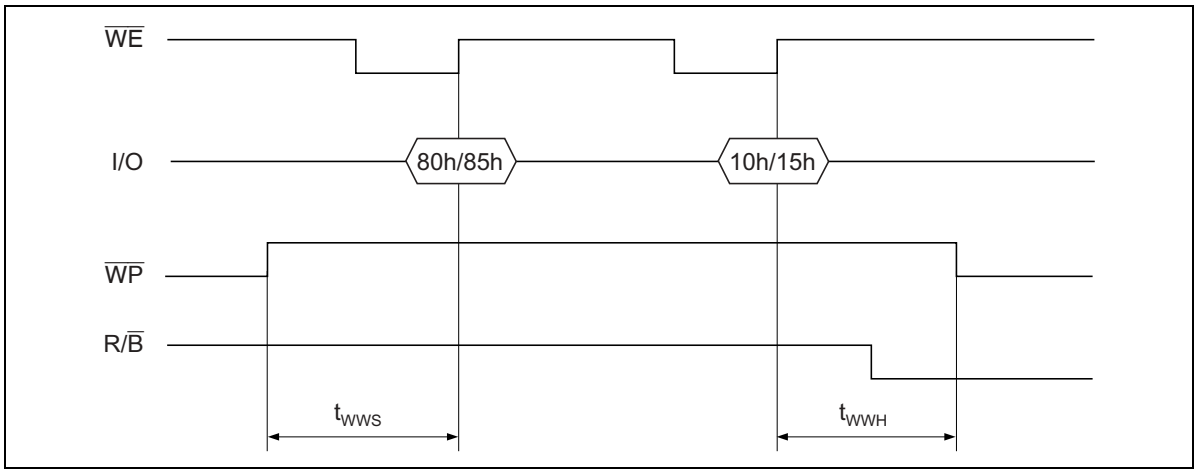


Note: 1. Power on sequence.

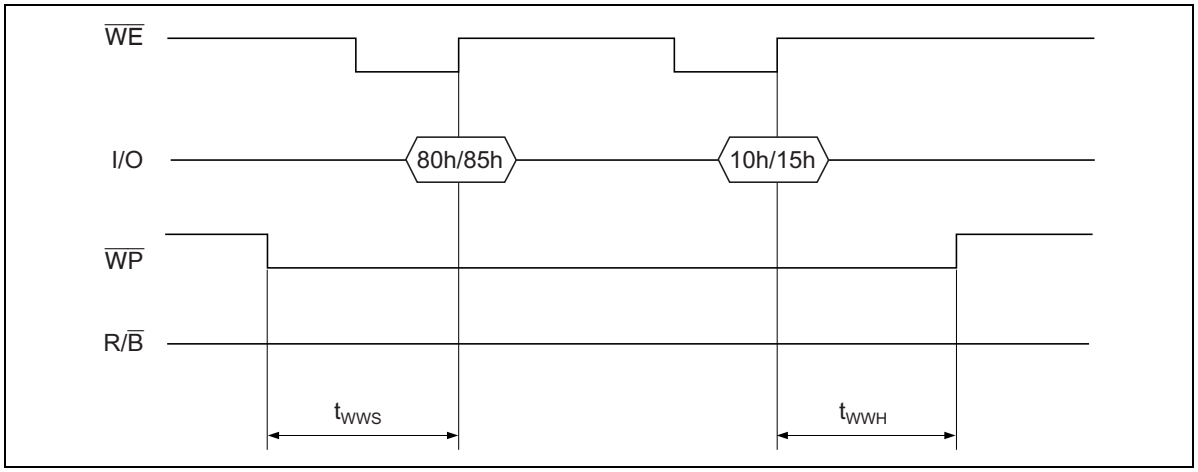
Usage for $\overline{WP}$

$\overline{WP}$ at the low level prohibits the erase operation and the program operation. When use $\overline{WP}$, use it as follows.

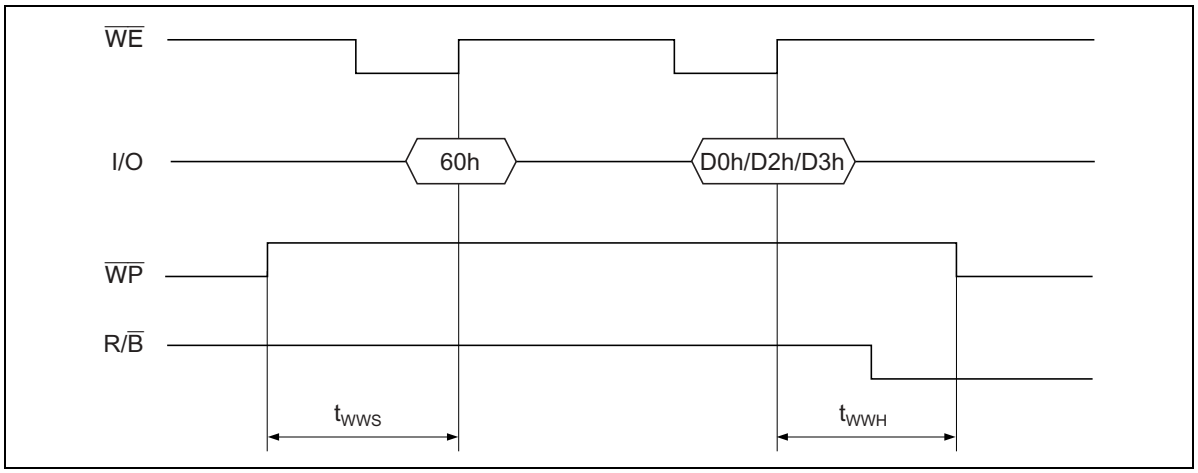
Program operation



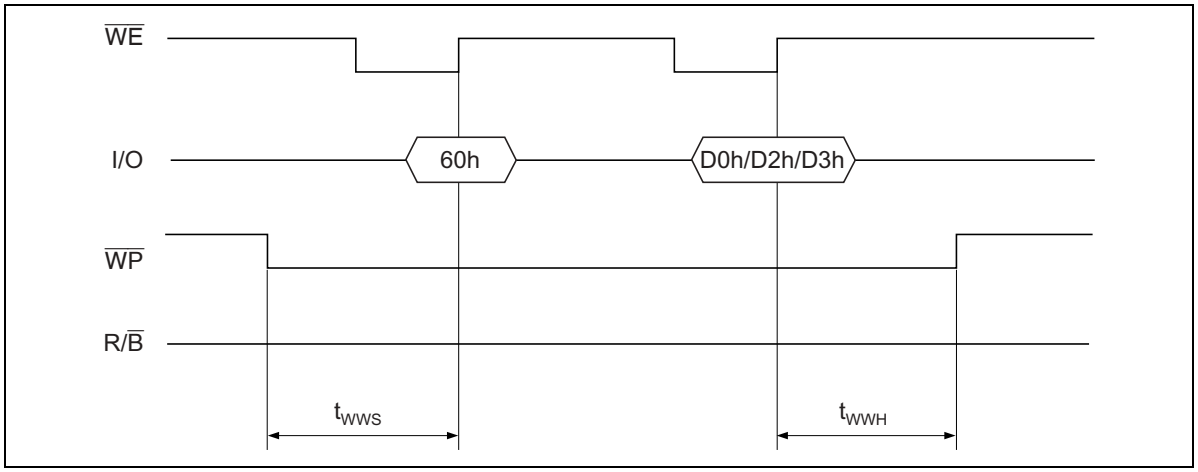
Prohibition of the Program operation



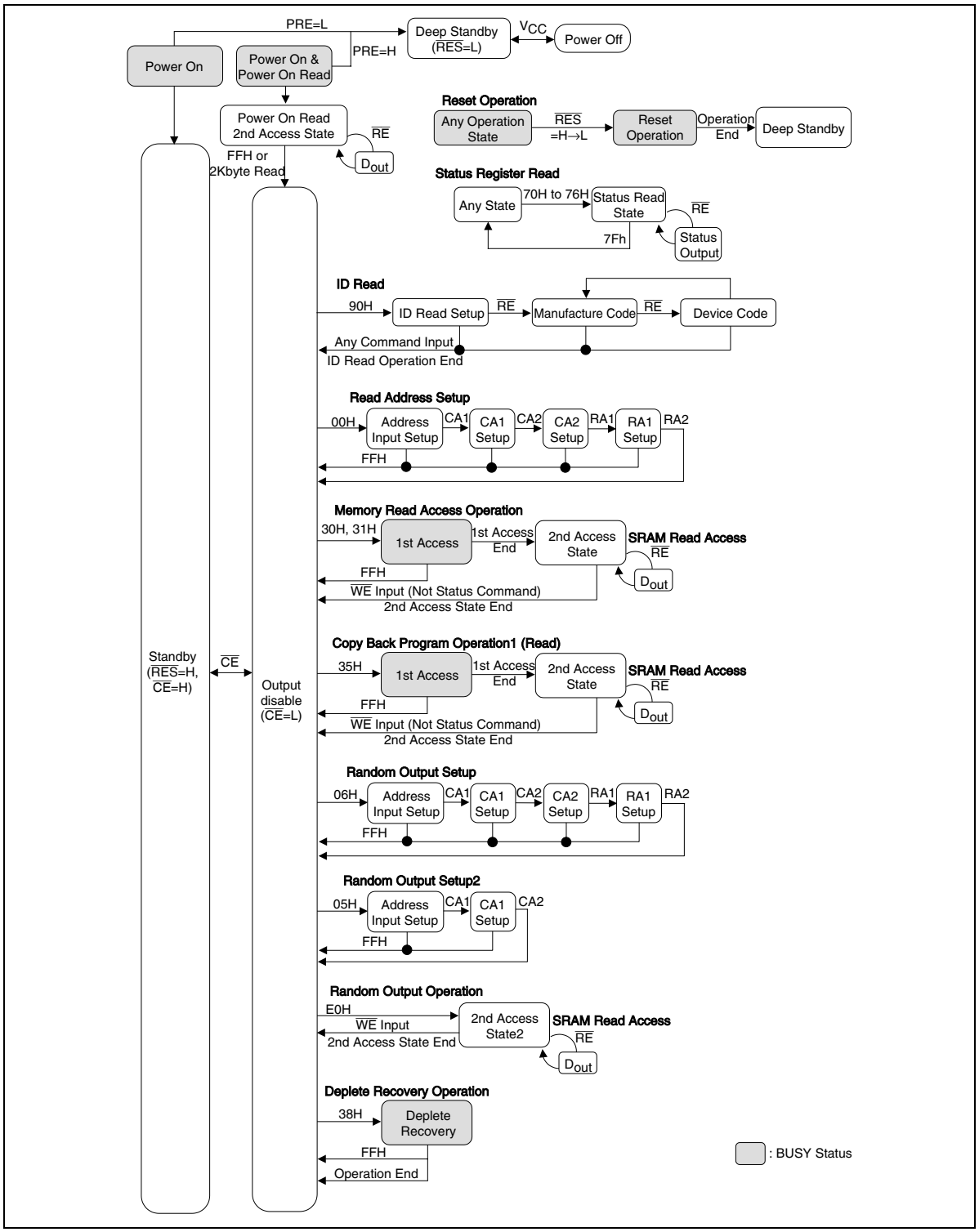
Erase operation

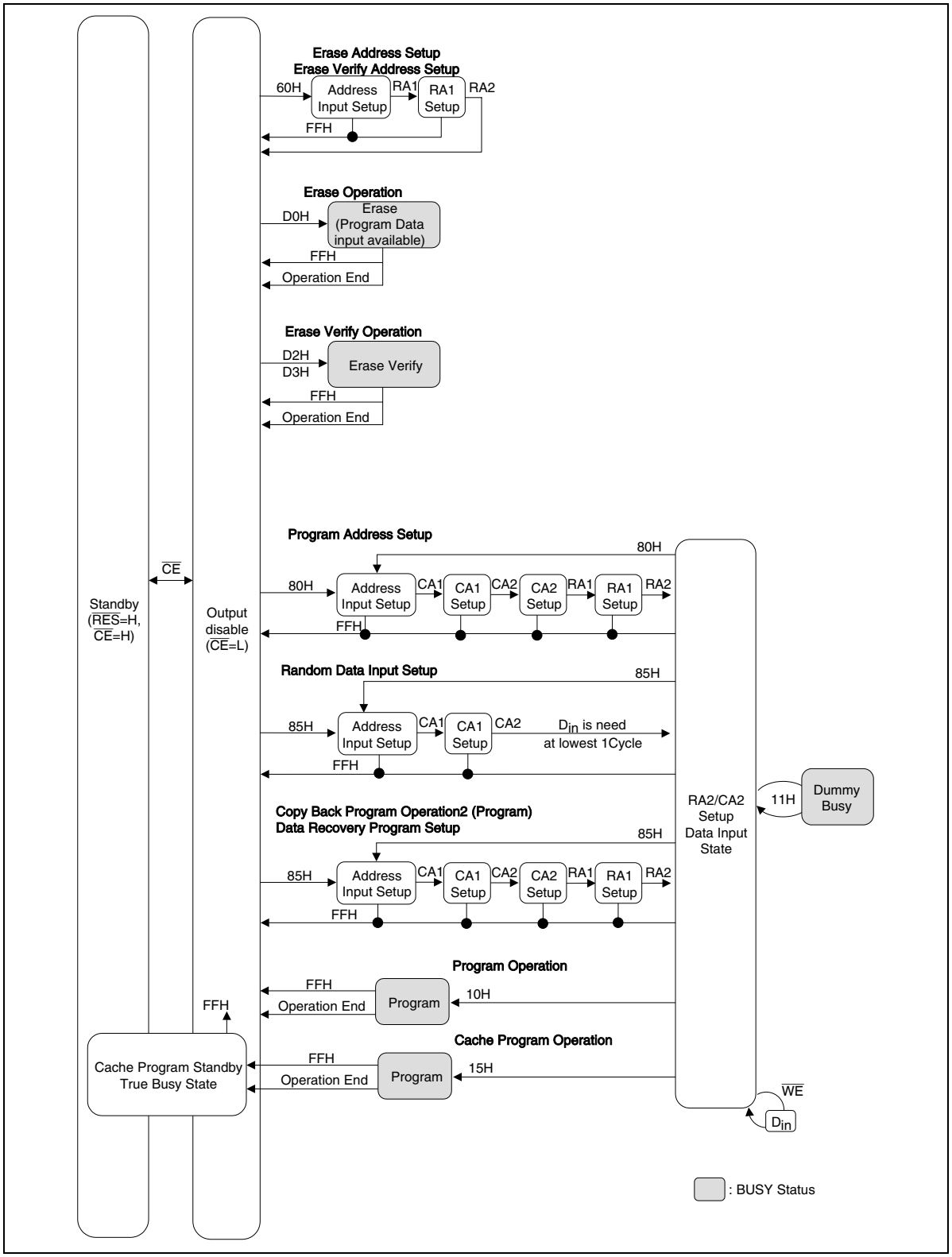


Prohibition of the Erase operation



Status Transition




Erase Address Setup
Erase Verify Address Setup
60H
Address Input Setup
RA1
RA1 Setup
RA2
FFH
Erase Operation
D0H
Erase (Program Data input available)
FFH
Operation End
Erase Verify Operation
D2H
D3H
Erase Verify
FFH
Operation End
Program Address Setup
80H
80H
Address Input Setup
CA1
CA1 Setup
CA2
CA2 Setup
RA1
RA1 Setup
RA2
FFH
CE
Standby (RES=H, CE=H)
Output disable (CE=L)
Random Data Input Setup
85H
85H
Address Input Setup
CA1
CA1 Setup
CA2
Din is need at lowest 1Cycle
FFH
Copy Back Program Operation2 (Program)
Data Recovery Program Setup
85H
85H
Address Input Setup
CA1
CA1 Setup
CA2
CA2 Setup
RA1
RA1 Setup
RA2
FFH
RA2/CA2 Setup Data Input State
11H
Dummy Busy
Program Operation
FFH
Operation End
Program
10H
FFH
Cache Program Operation
Cache Program Standby True Busy State
FFH
Operation End
Program
15H
WE
Din
: BUSY Status

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
V_{CC} voltage	V_{CC}	–0.6 to +4.6	V	1
V_{SS} voltage	V_{SS}	0	V	
All input and output voltage	V_{in}, V_{out}	–0.6 to +4.6	V	1, 2
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–25 to +85	°C	3

Notes: 1. Relative to V_{SS}.
2. V_{in}/V_{out} = –2.0 V for pulse width with 20ns or less.
3. Device Storage temperature before programming.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	C_{in}	—	—	6	pF	V_{in} = 0 V, Ta = +25°C, f = 1 MHz
Output capacitance	C_{out}	—	—	10	pF	V_{out} = 0 V, Ta = +25°C, f = 1 MHz

Valid Block (Left side chip)

Parameter		Symbol	Min	Typ	Max	Unit
Valid Block Number	Bank0	N_{VB0}	8029	—	8192	blocks
	Bank1	N_{VB1}	8029	—	8192	blocks
	Bank2	N_{VB2}	8029	—	8192	blocks
	Bank3	N_{VB3}	8029	—	8192	blocks

Spare Block (Left side chip)

Parameter		Symbol	Min	Typ	Max	Unit
Spare Block Number	Bank0	N_{SB0}	145	—	—	blocks
	Bank1	N_{SB1}	145	—	—	blocks
	Bank2	N_{SB2}	145	—	—	blocks
	Bank3	N_{SB3}	145	—	—	blocks

Valid Block (Right side chip)

Parameter		Symbol	Min	Typ	Max	Unit
Valid Block Number	Bank0	N_{VB0}	8029	—	8192	blocks
	Bank1	N_{VB1}	8029	—	8192	blocks
	Bank2	N_{VB2}	8029	—	8192	blocks
	Bank3	N_{VB3}	8029	—	8192	blocks

Spare Block (Right side chip)

Parameter		Symbol	Min	Typ	Max	Unit
Spare Block Number	Bank0	N_{SB0}	145	—	—	blocks
	Bank1	N_{SB1}	145	—	—	blocks
	Bank2	N_{SB2}	145	—	—	blocks
	Bank3	N_{SB3}	145	—	—	blocks

DC Characteristics

(V_{CC} = 2.7 V to 3.6 V, Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Operating V_{CC} voltage		V_{CC}	2.7	3.3	3.6	V	
Operating V_{CC} current	(1-chip operation)	I_{CC1}	—	10	20	mA	t_{RC} = 50ns, $\overline{CE}$ = V_{iL}, Iout = 0mA
(Read)	(2-chip operation)	I_{CC1}	—	20	40	mA	
Operating V_{CC} current	(1-chip operation)	I_{CC2}	—	15	30	mA	t_{RC} = 35ns, $\overline{CE}$ = V_{iL}, Iout = 0mA
(Read)	(2-chip operation)	I_{CC2}	—	30	60	mA	
Operating V_{CC} current	(1-chip operation)	I_{CC3}	—	10	20	mA	Single Bank Operation
(Program)	(2-chip operation)	I_{CC3}	—	20	40	mA	
Operating V_{CC} current	(1-chip operation)	I_{CC4}	—	20	30	mA	Multi Bank Operation
(Program)	(2-chip operation)	I_{CC4}	—	40	60	mA	
Operating V_{CC} current	(1-chip operation)	I_{CC5}	—	10	20	mA	Single Bank Operation
(Erase)	(2-chip operation)	I_{CC5}	—	20	40	mA	
Operating V_{CC} current	(1-chip operation)	I_{CC6}	—	15	30	mA	Multi Bank Operation
(Erase)	(2-chip operation)	I_{CC6}	—	30	60	mA	
Standby current	(1-chip operation)	I_{SB1}	—	—	1	mA	
(TTL)	(2-chip operation)	I_{SB1}	—	—	2	mA	
Standby current	(1-chip operation)	I_{SB2}	—	10	50	µA	
(CMOS)	(2-chip operation)	I_{SB2}	—	20	100	µA	
Deep standby current	(1-chip operation)	I_{SB3}	—	—	5	µA	
(CMOS)	(2-chip operation)	I_{SB3}	—	—	10	µA	
Input Leakage Current		I_{Li}	—	—	±10	µA	V_{in} = 0 to 3.6 V
Output Leakage Current		I_{Lo}	—	—	±10	µA	V_{in} = 0 to 3.6 V
Input voltage		V_{iH}	2.0	—	V_{CC} + 0.3	V	
		V_{iL}	–0.3	—	0.8	V	
Input voltage ($\overline{RES}$, $\overline{WP}$, PRE)		V_{iHD}	V_{CC} – 0.2	—	V_{CC} + 0.2	V	
		V_{iLD}	–0.2	—	+0.2	V	
Output High voltage Level		V_{oH}	2.4	—	—	V	I_{OH} = –400 µA
Output Low voltage Level		V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output Low Current (R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	5	8	—	mA	V_{OL} = 0.4 V

AC Characteristics

(V_{CC} = 2.7 V to 3.6 V, Ta = 0 to +70°C)

Test Conditions

- Input pulse levels: 0.4 to 2.4 V
- Input rise and fall time: 3 ns
- Input and output timing levels: 1.5 V / 1.5 V
- Output load: 1TTL GATE and 50 pF (3.0 V ± 10%)
  1TTL GATE and 100 pF (3.3 V ± 10%)

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Typ	Max	Unit	Note
CLE Setup Time	t_{CLS}	0	—	—	ns	
CLE Hold Time	t_{CLH}	9	—	—	ns	
$\overline{CE}$ Setup Time	t_{CS}	0	—	—	ns	
$\overline{CE}$ Hold Time	t_{CH}	6	—	—	ns	
$\overline{WE}$ Pulse Width	t_{WP}	15	—	—	ns	1
ALE Setup Time	t_{ALS}	0	—	—	ns	
ALE Hold Time	t_{ALH}	6	—	—	ns	
Data Setup Time	t_{DS}	9	—	—	ns	
Data Hold Time	t_{DH}	9	—	—	ns	
Write cycle Time	t_{WC}	33	—	—	ns	
$\overline{WE}$ High Hole Time	t_{WH}	12	—	—	ns	
$\overline{CE}$ High to $\overline{WE}$ low setup time	t_{CHWS}	5	—	—	ns	
$\overline{WE}$ High to $\overline{CE}$ low hold time	t_{WHCH}	5	—	—	ns	
$\overline{CE}$ High to $\overline{RE}$ low setup time	t_{CHRS}	5	—	—	ns	
$\overline{RE}$ High to $\overline{CE}$ low hold time	t_{RHCH}	5	—	—	ns	

Note: 1. If t_{CS} is set less than 5 ns, t_{WP} must be minimum 20 ns. Otherwise, t_{WP} is minimum 15 ns.

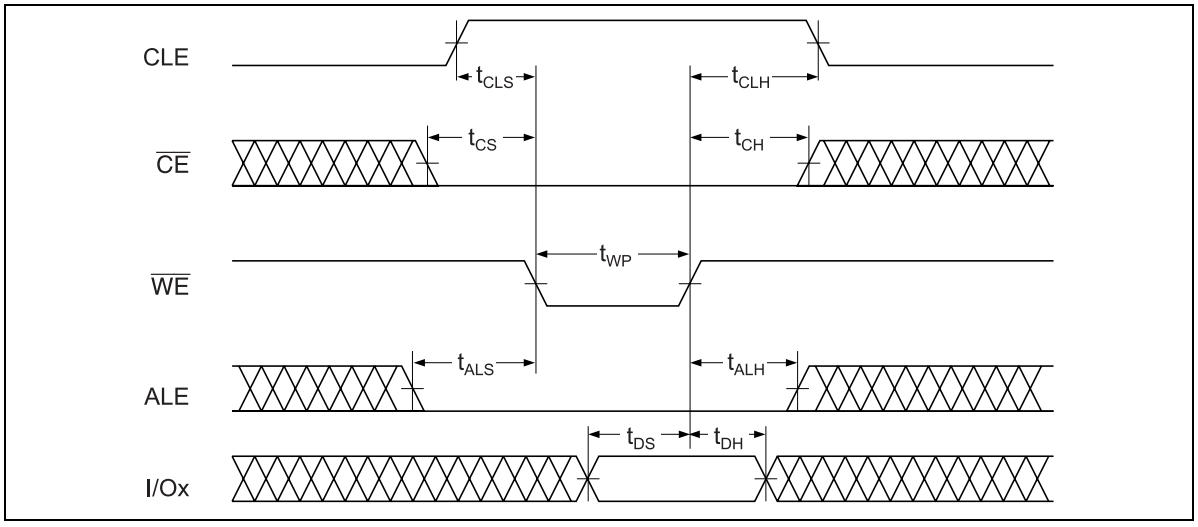
AC Timing Characteristics for Operation

Parameter		Symbol	Min	Typ	Max	Unit	Note
Data Transfer from Cell to Register		t_R	—	—	120	µs	
ALE to $\overline{RE}$ Delay (ID Read)		t_{AR1}	20	—	—	ns	
ALE to $\overline{RE}$ Delay (Read cycle)		t_{AR2}	30	—	—	ns	
CLE to $\overline{RE}$ Delay (Read cycle)		t_{CLR}	6	—	—	ns	
Ready to $\overline{RE}$ Low		t_{RR}	20	—	—	ns	
$\overline{RE}$ Pulse Width		t_{RP}	20	—	—	ns	
$\overline{WE}$ High to Busy		t_{WB}	—	—	100	ns	
Read cycle time		t_{RC}	35	—	—	ns	
$\overline{RE}$ Access Time		t_{REA}	—	—	20	ns	
$\overline{CE}$ Access Time		t_{CEA}	—	—	25	ns	
$\overline{RE}$ High to Output Hi-Z		t_{RHZ}	10	—	20	ns	1
$\overline{CE}$ High to Output Hi-Z		t_{CHZ}	0	—	20	ns	1
$\overline{RE}$ High Hold Time		t_{REH}	10	—	—	ns	
Output Hi-Z to $\overline{RE}$ Low		t_{IR}	0	—	—	ns	
$\overline{WE}$ High to $\overline{RE}$ Low		t_{WHR}	50	—	—	ns	
Device Resetting Time	Read	t_{RSTR}	—	—	20	µs	
	Program	t_{RSTP}	—	—	70	µs	
	Erase	t_{RSTE}	—	—	400	µs	
	Erase Verify	t_{RSTEV}	—	—	30	µs	
	Device recovery	t_{RSTDR}	—	—	350	µs	
Power on busy Time		t_{PON}	—	—	200	µs	
V_{CC} Setup time to Reset		t_{VRS}	100	—	—	µs	
V_{CC} to Ready		t_{VRDY}	—	—	100	µs	
Reset to Busy		t_{BSY}	—	—	100	ns	
$\overline{WP}$ setup time to $\overline{WE}$ High		t_{WWS}	15	—	—	ns	
$\overline{WP}$ hold time to $\overline{WE}$ High		t_{WWH}	15	—	—	ns	
$\overline{CE}$ setup time to Deep standby		t_{CSD}	100	—	—	ns	

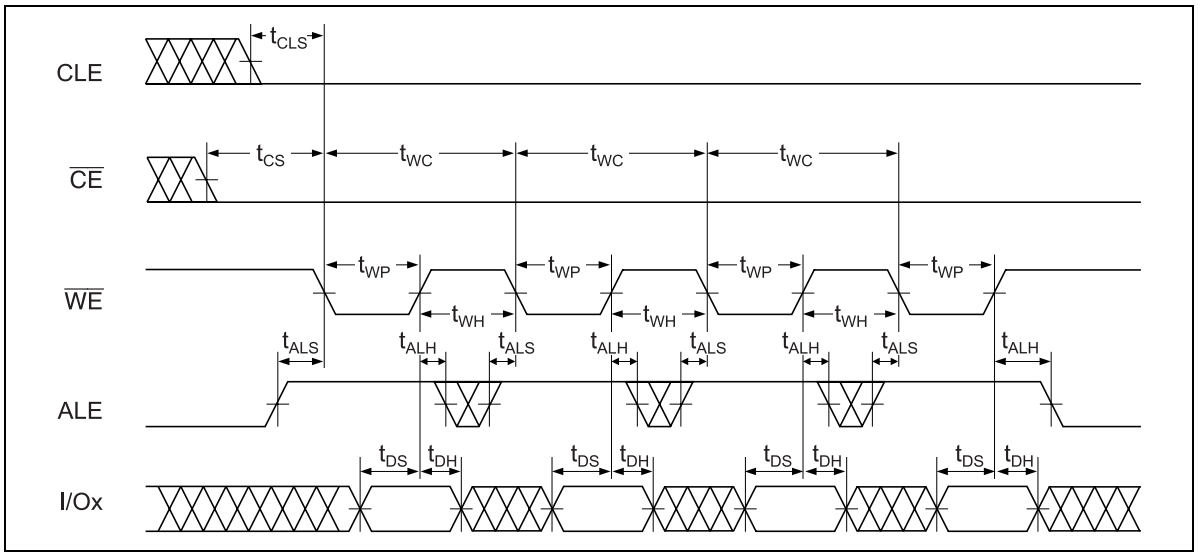
Note: 1. The time until it becomes Hi-Z depends on the earliest signal which $\overline{CE}$ and $\overline{RE}$ go to high.

Timing Waveform

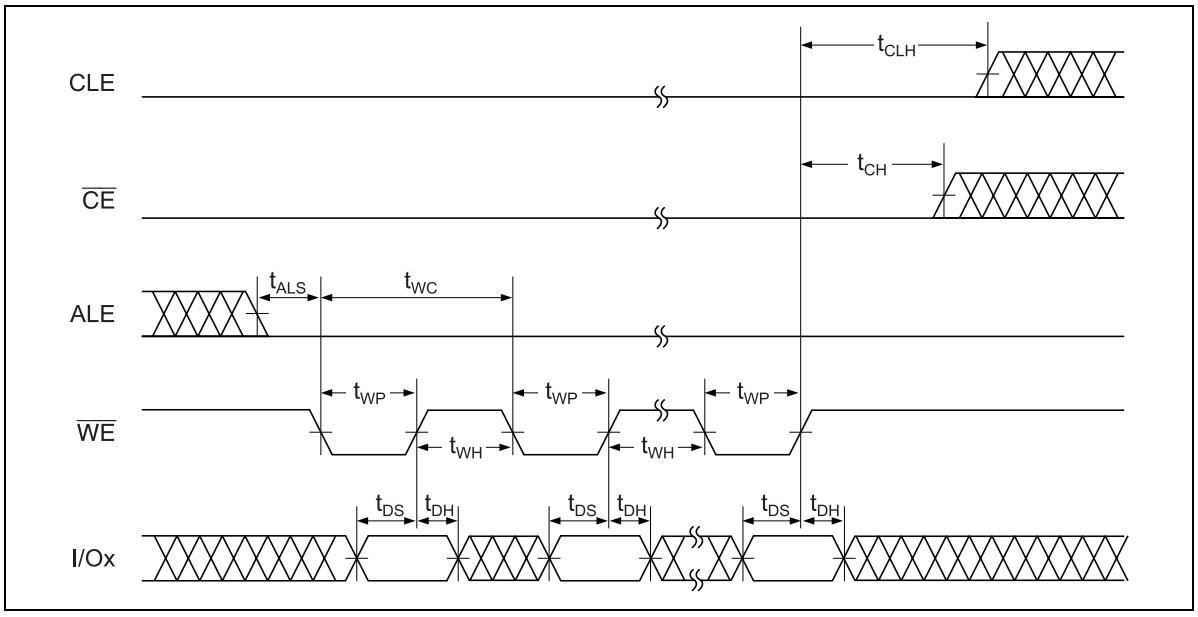
Command Latch Cycle



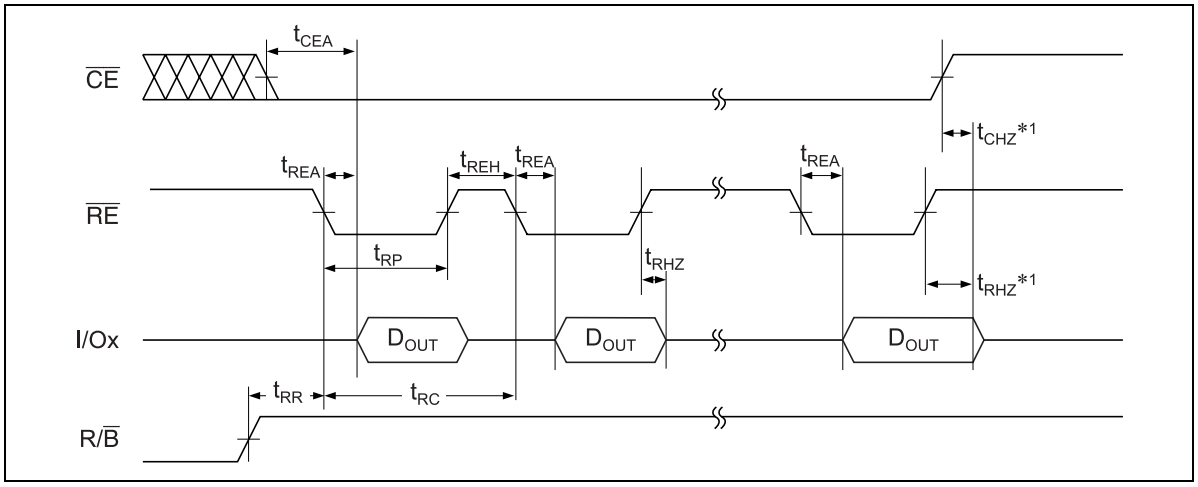
Address Latch Cycle



Input Data Latch Cycle

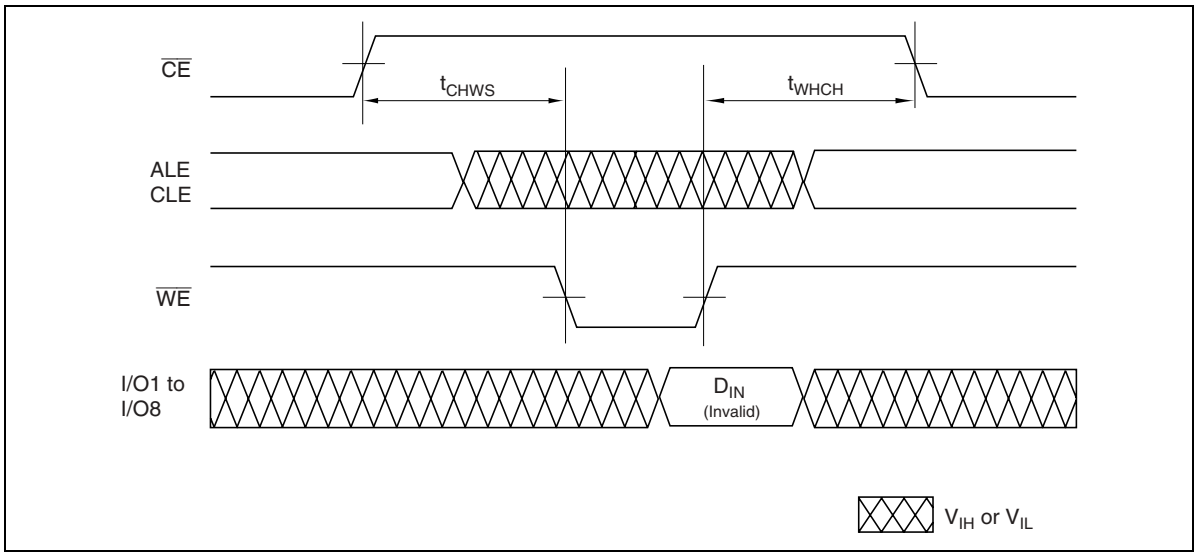


Serial Access Cycle after Read (CLE = L, $\overline{WE}$ = H, ALE = L)

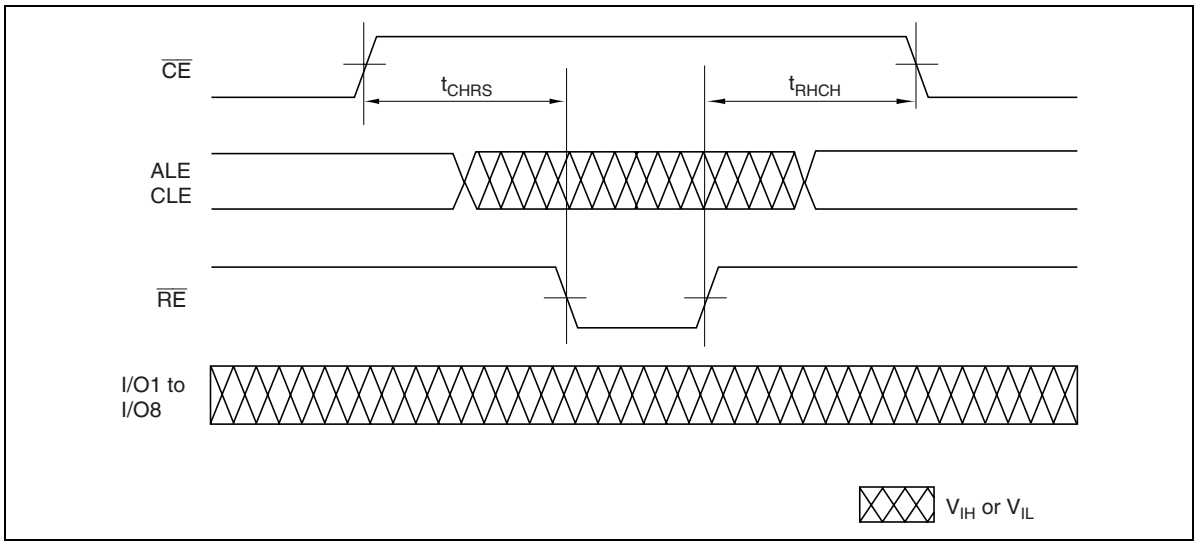


Note: 1. The time until it becomes Hi-Z depends on the earliest signal which $\overline{CE}$ and $\overline{RE}$ go to high.

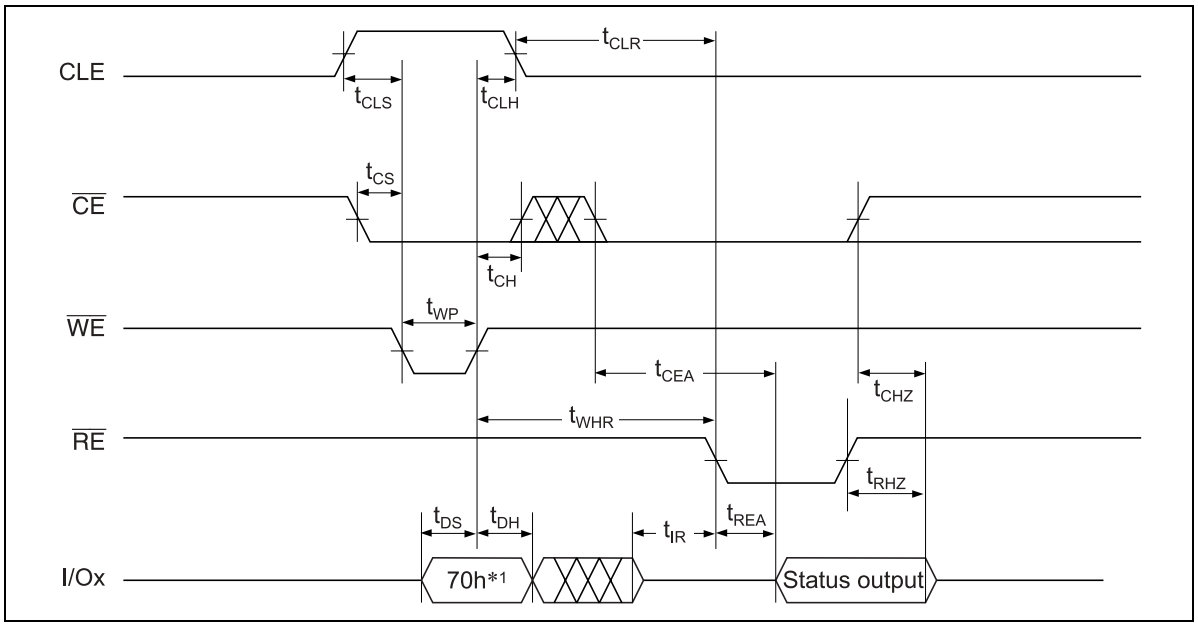
Invalid input cycle



Invalid output cycle

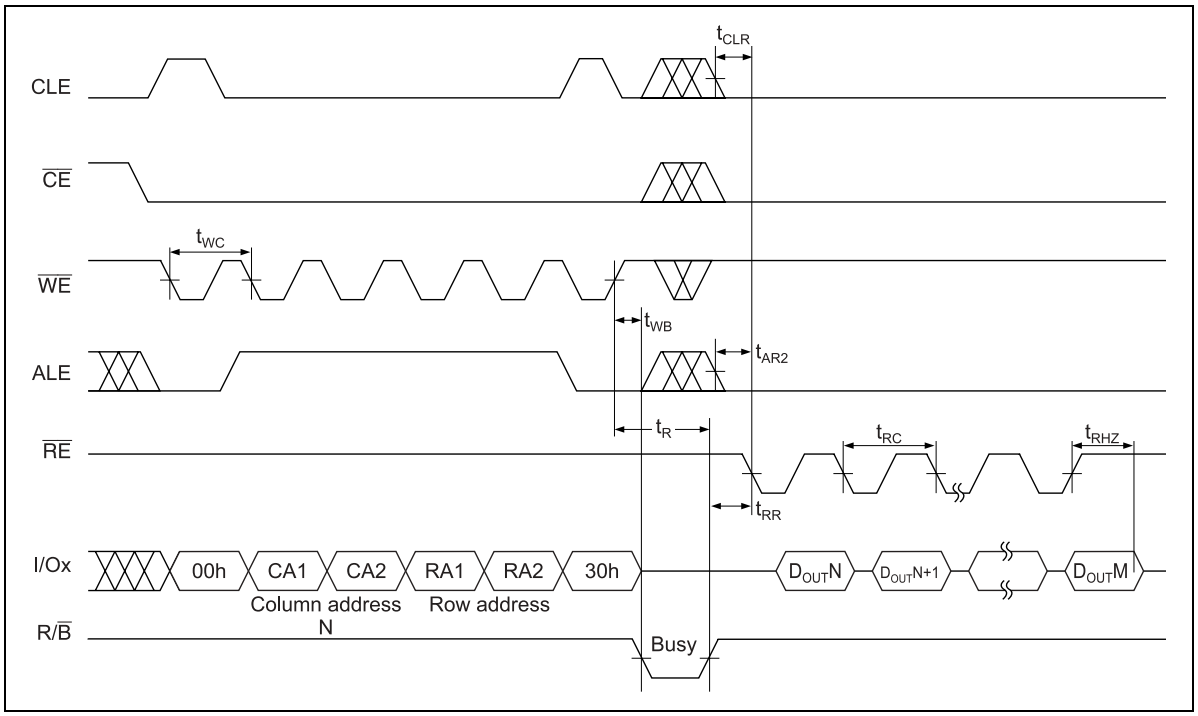


Status Read Cycle

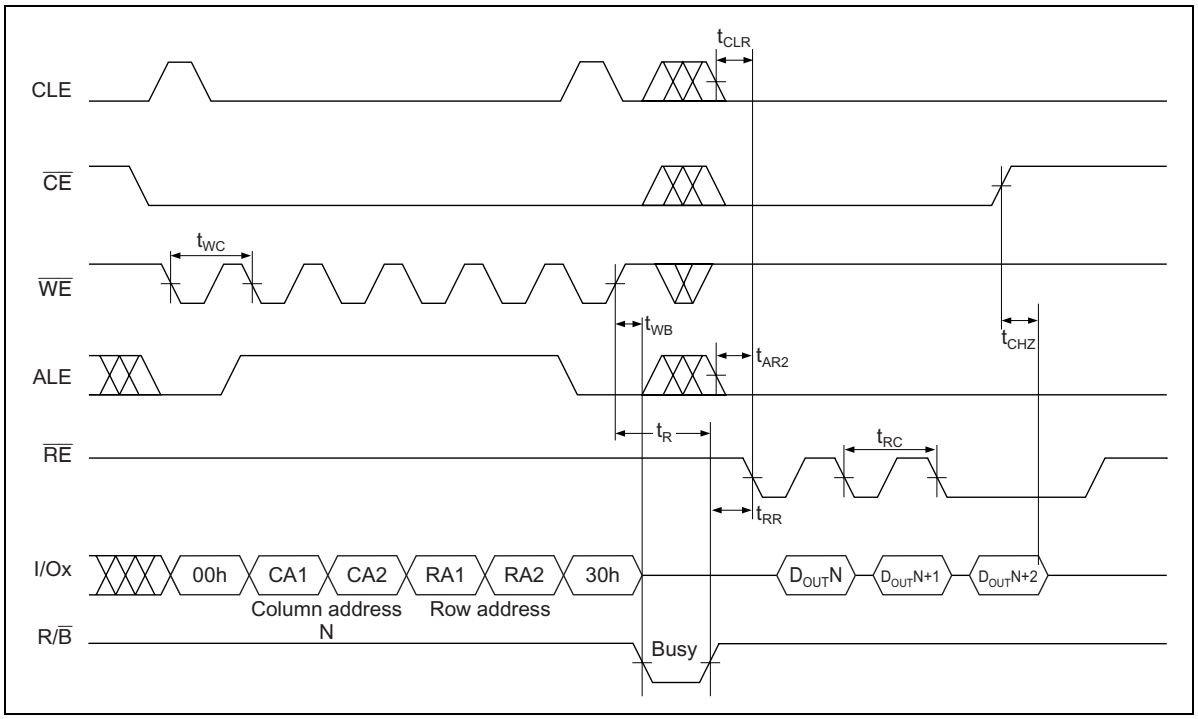


Note: 1. 70h: Single Bank operation Status
72h: Single Bank operation Error Status
71h: Multi Bank operation Status
73h: Multi Bank operation / Bank0 Error Status
74h: Multi Bank operation / Bank1 Error Status
75h: Multi Bank operation / Bank2 Error Status
76h: Multi Bank operation / Bank3 Error Status

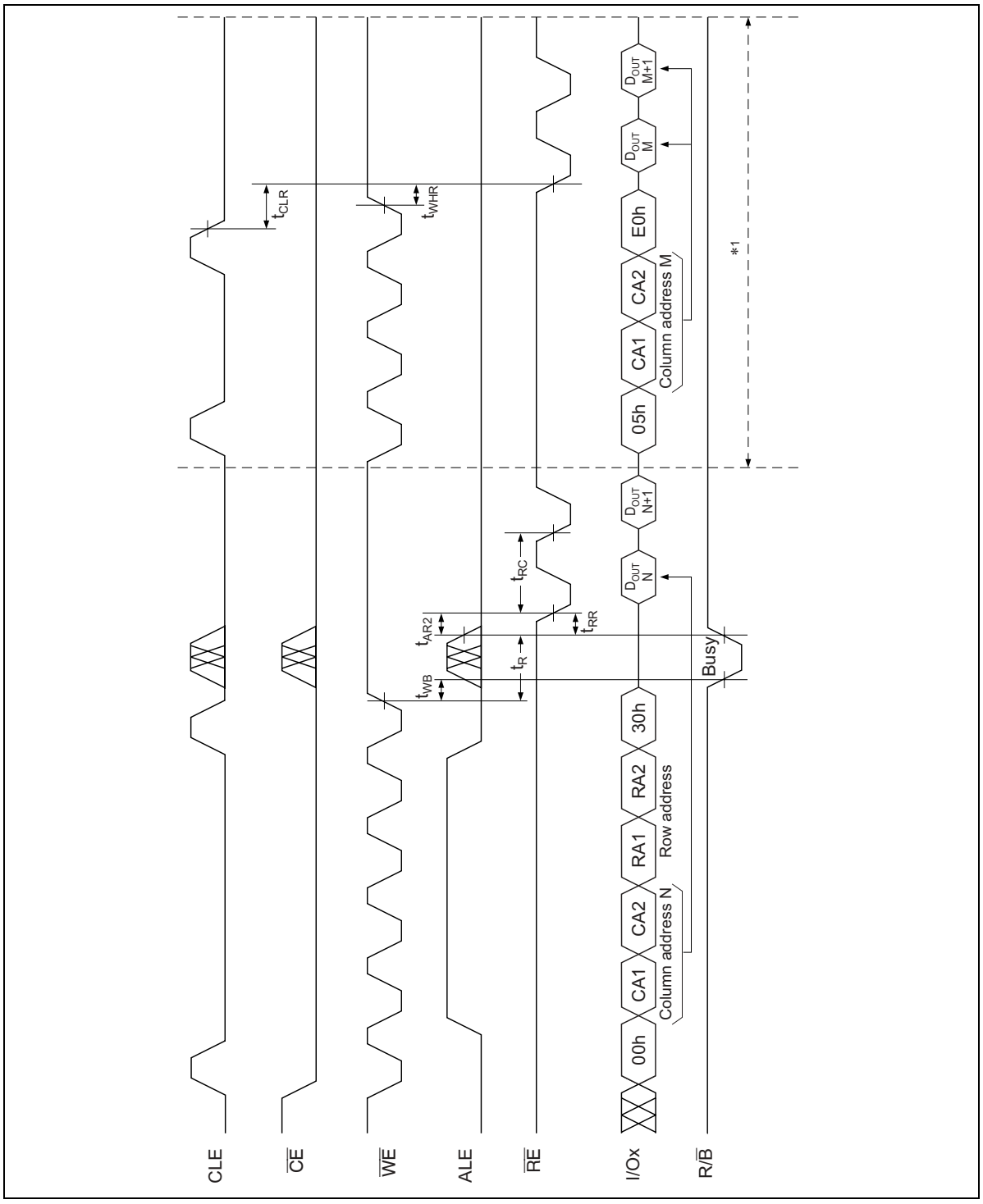
Read Operation



Read Operation (Intercepted by $\overline{CE}$)

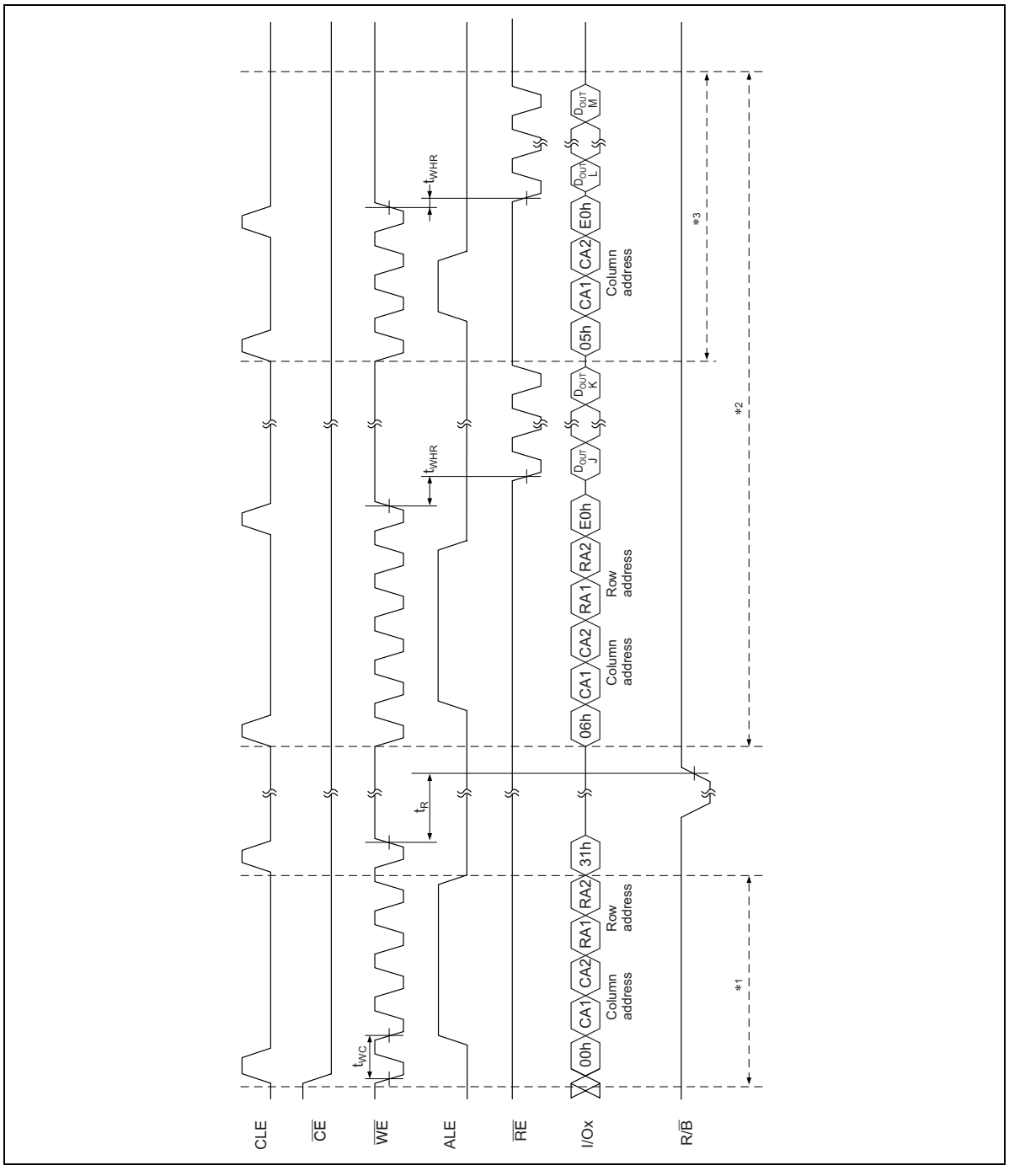


Random Data Output in a Page



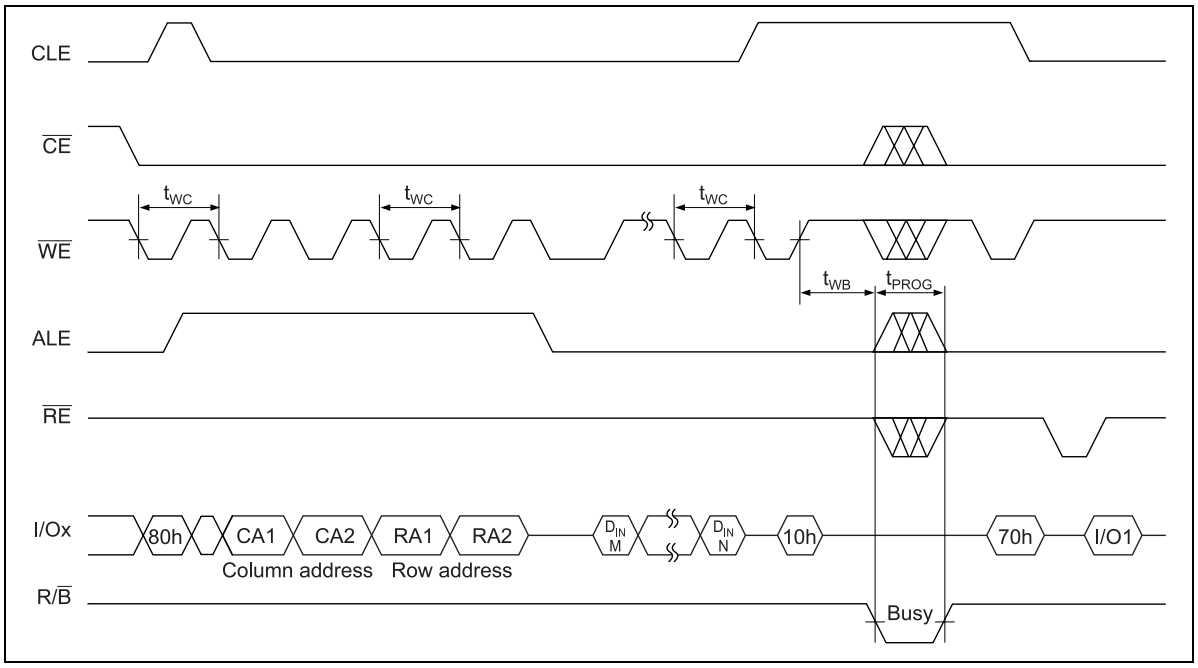
Note: 1. The head column address can be specified over and over.

Multi Bank Read

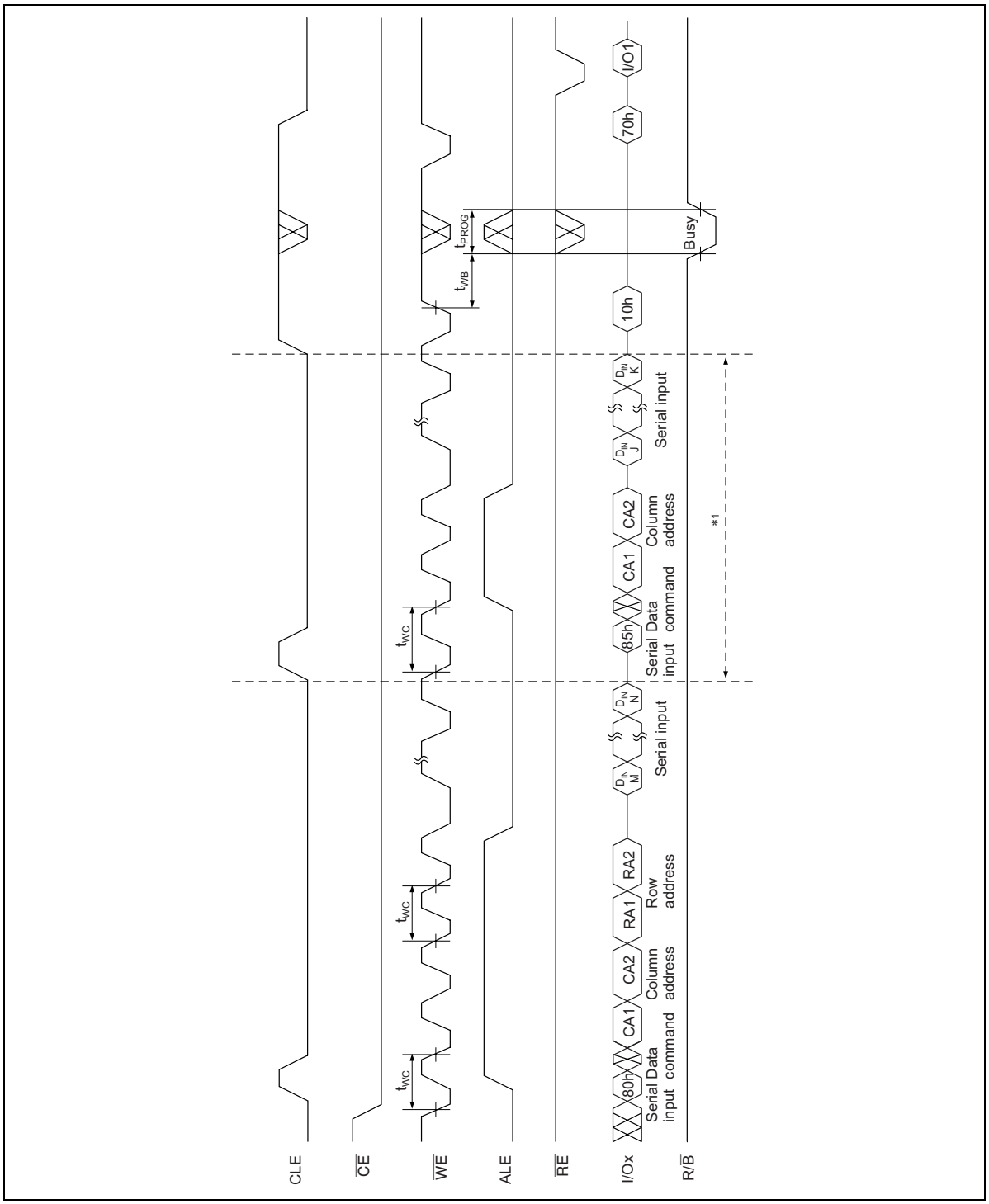


Notes: 1. A maximum 4 bank from Bank0 to Bank3 can be repeated.
2. Read out specified bank.
3. It is repeated over and over within the same page setup.

Page program Operation

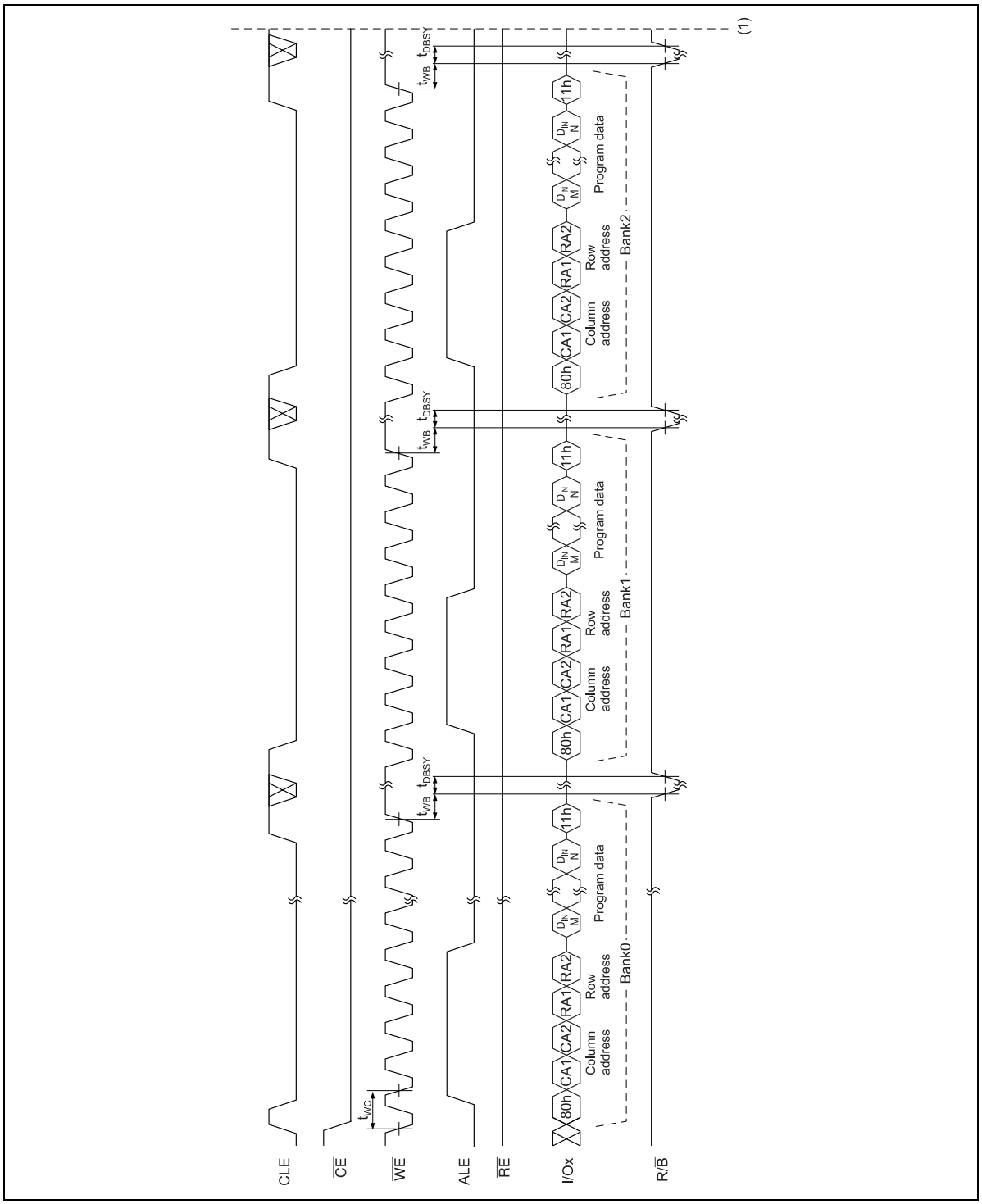


Page Program Operation with Random Data Input



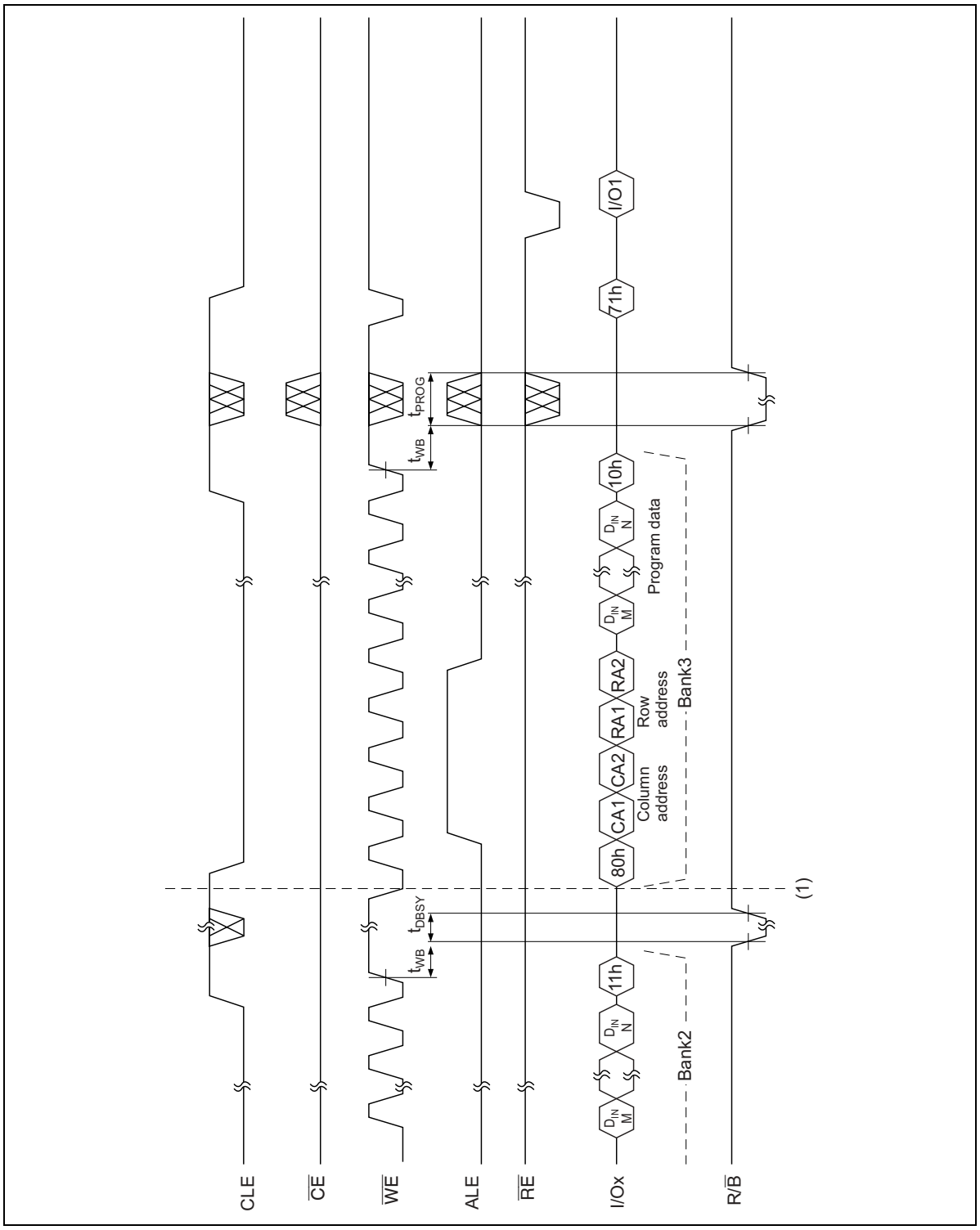
Note: 1. It is repeated over and over within the same page setup.

Multi Bank Program (1/2)

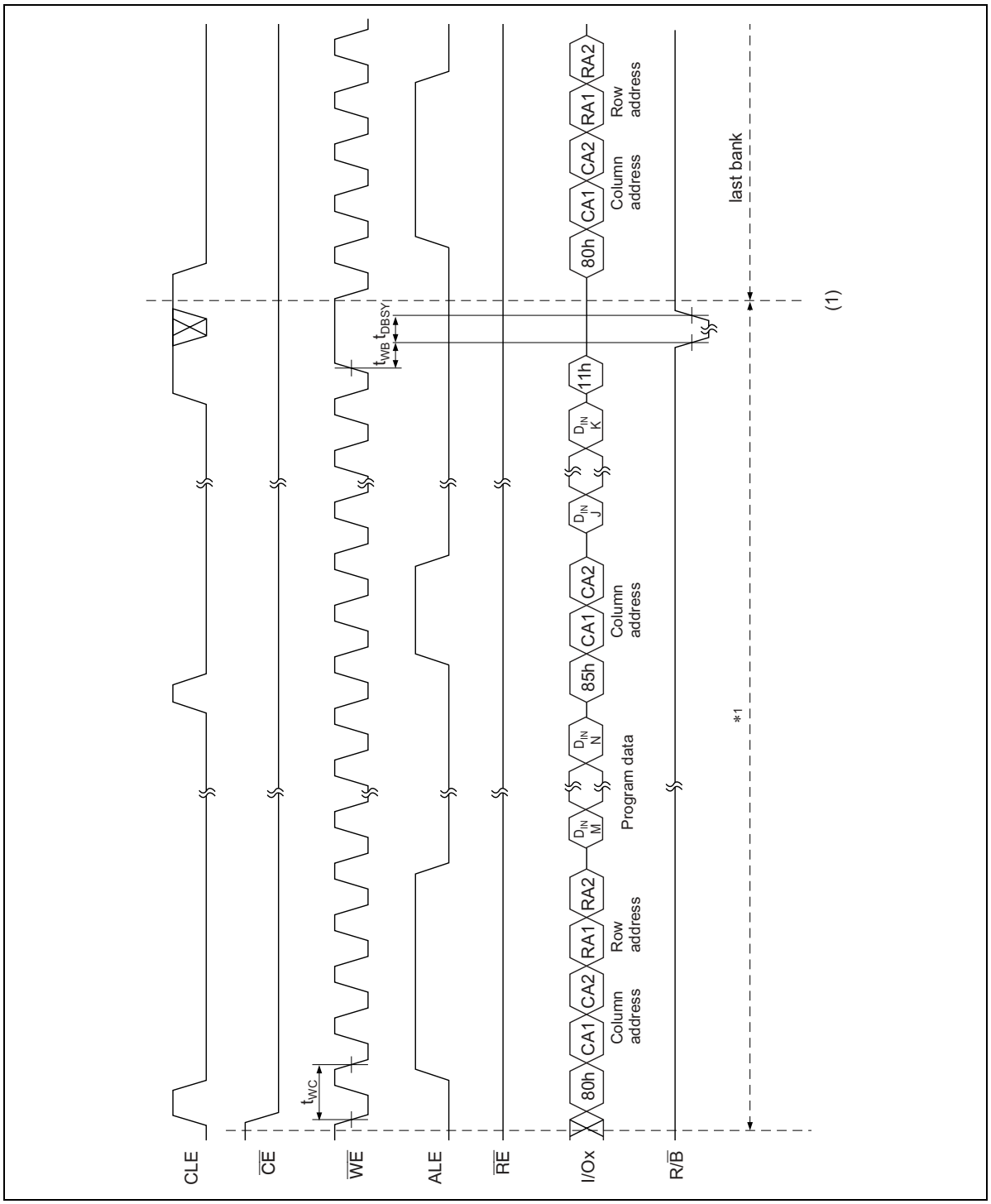


Note: 1. A maximum 4 bank from Bank0 to Bank3 can be repeated.

Multi Bank Program (2/2)

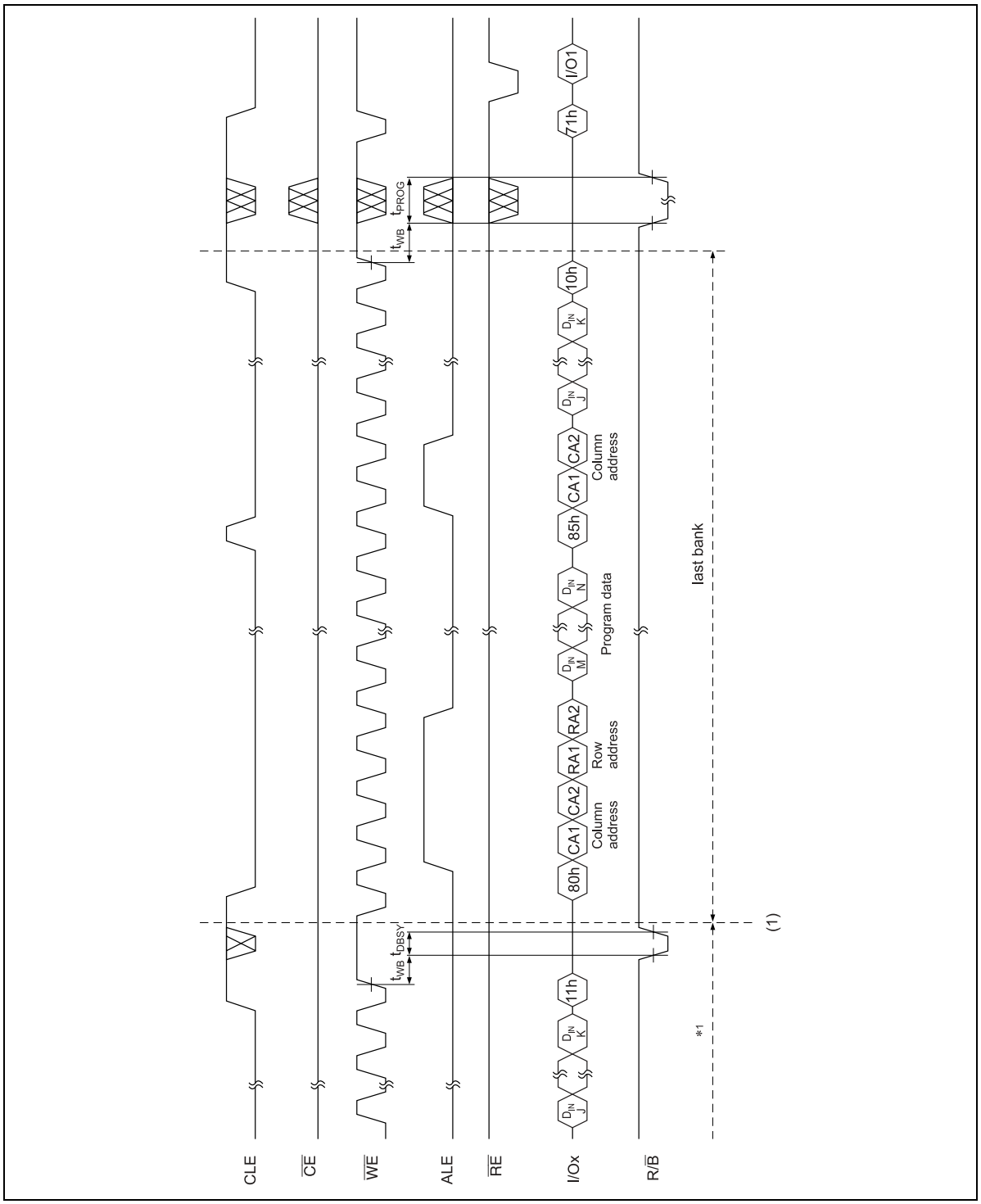


Multi Bank Program Operation with Random Data Input (1/2)



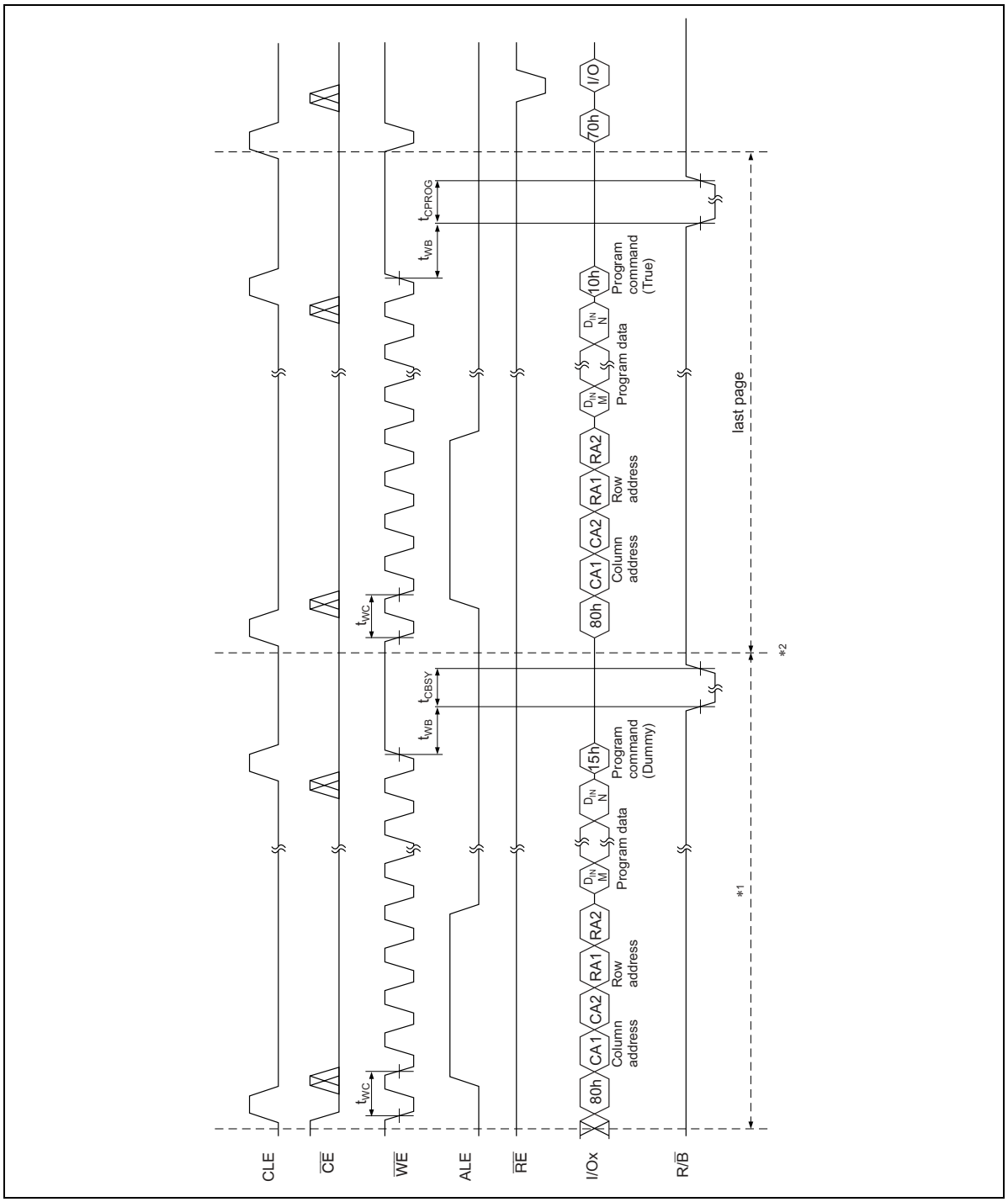
Note: 1. Maximum three times repeatable.

Multi Bank Program Operation with Random Data Input (2/2)



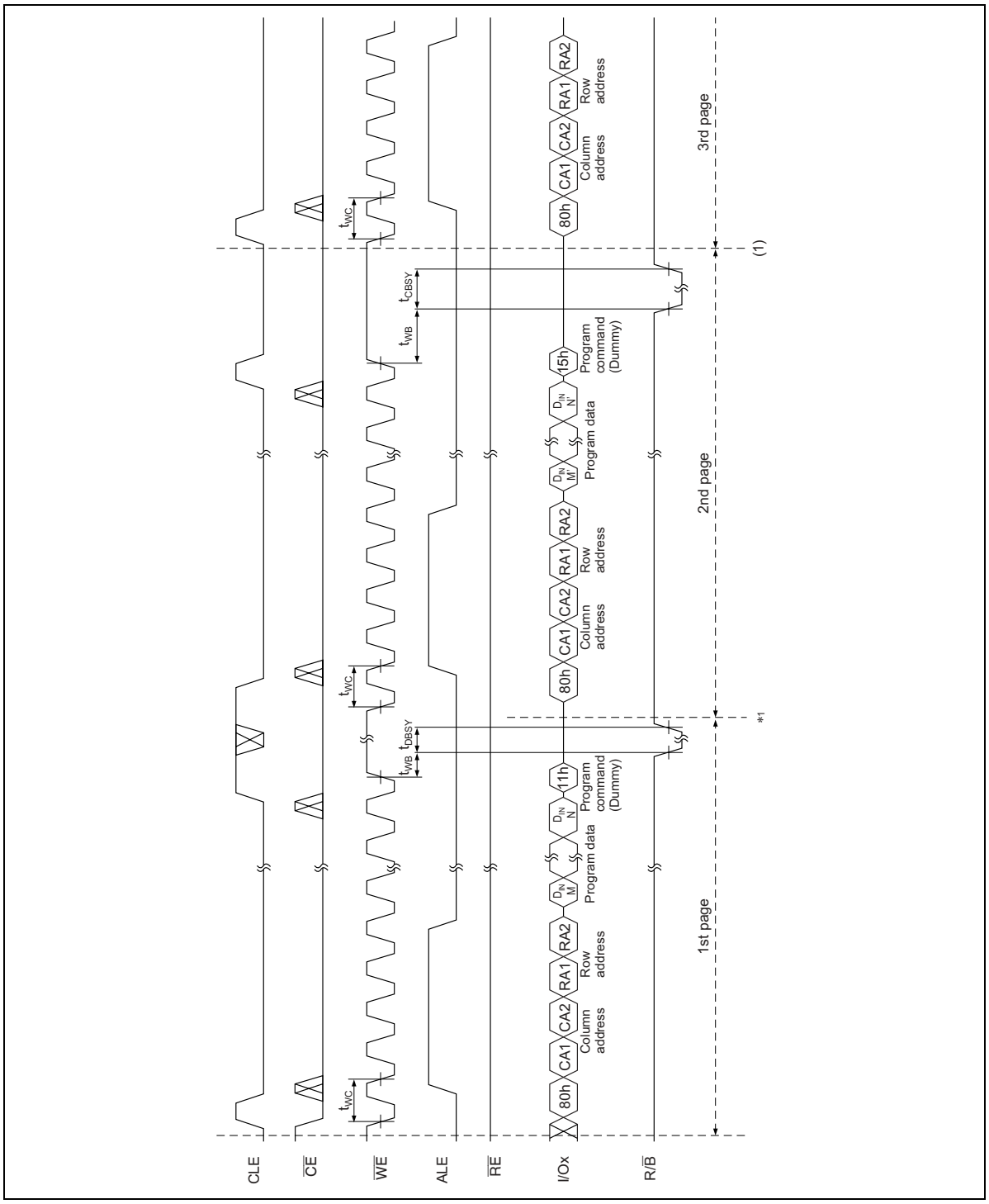
Note: 1. Maximum three times repeatable.

Cache Program



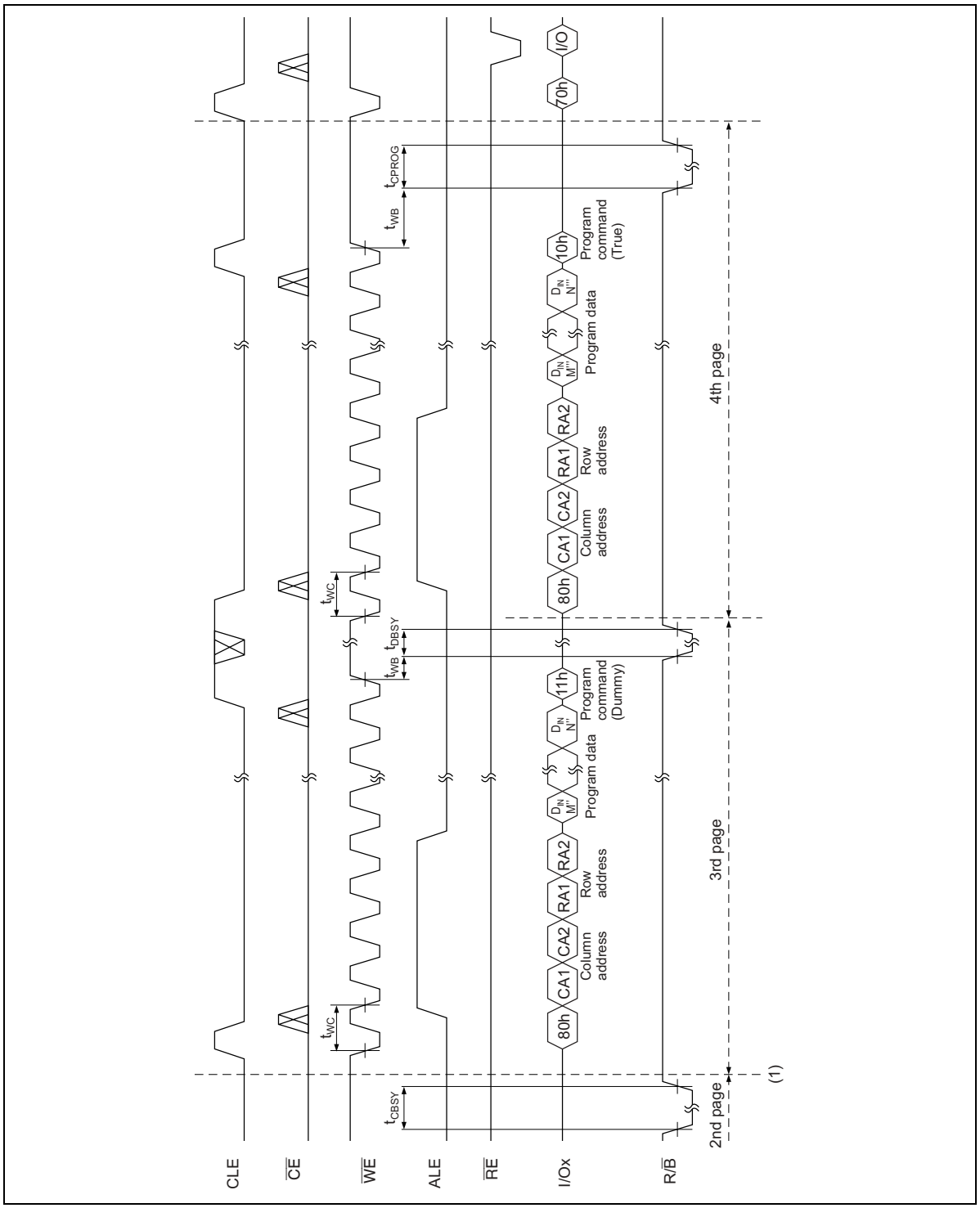
Notes: 1. There is no limitation in the number of Page address which can specify consecutively.
2. Don't specify a Page address inside the same bank consecutively.

2 Page Cache Program (1/2)

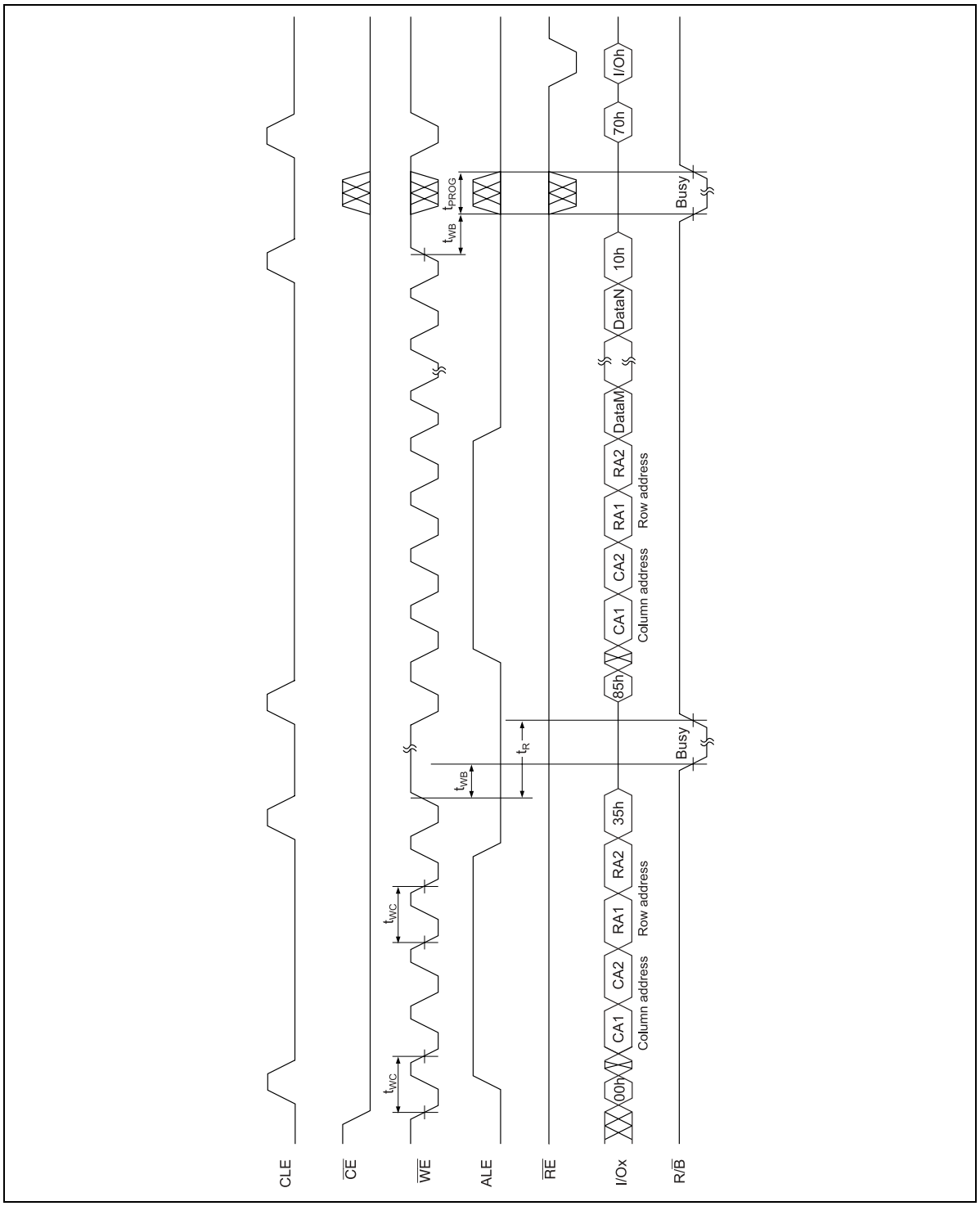


Note: 1. Don't specify a Page address inside the same bank consecutively.

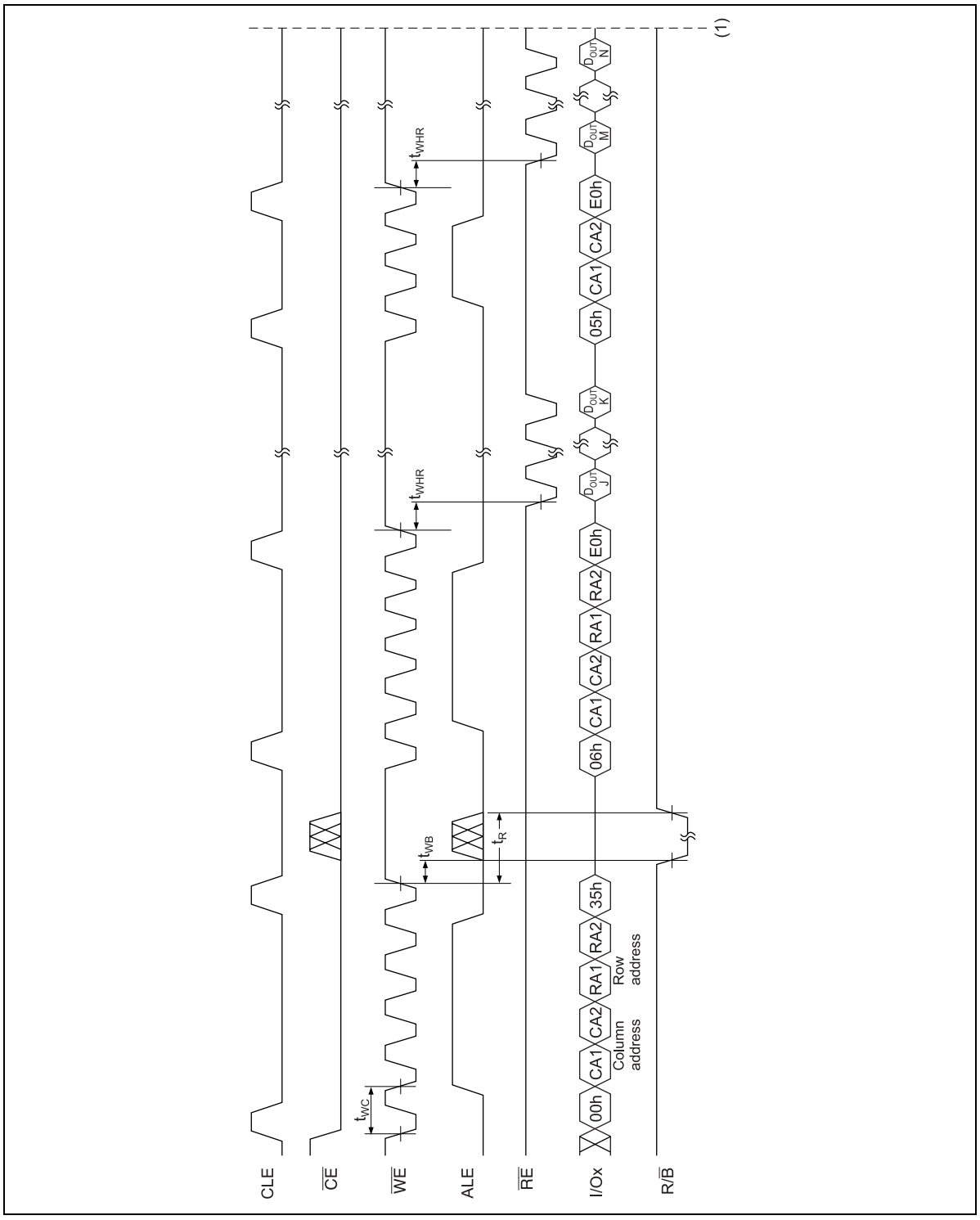
2 Page Cache Program (2/2)



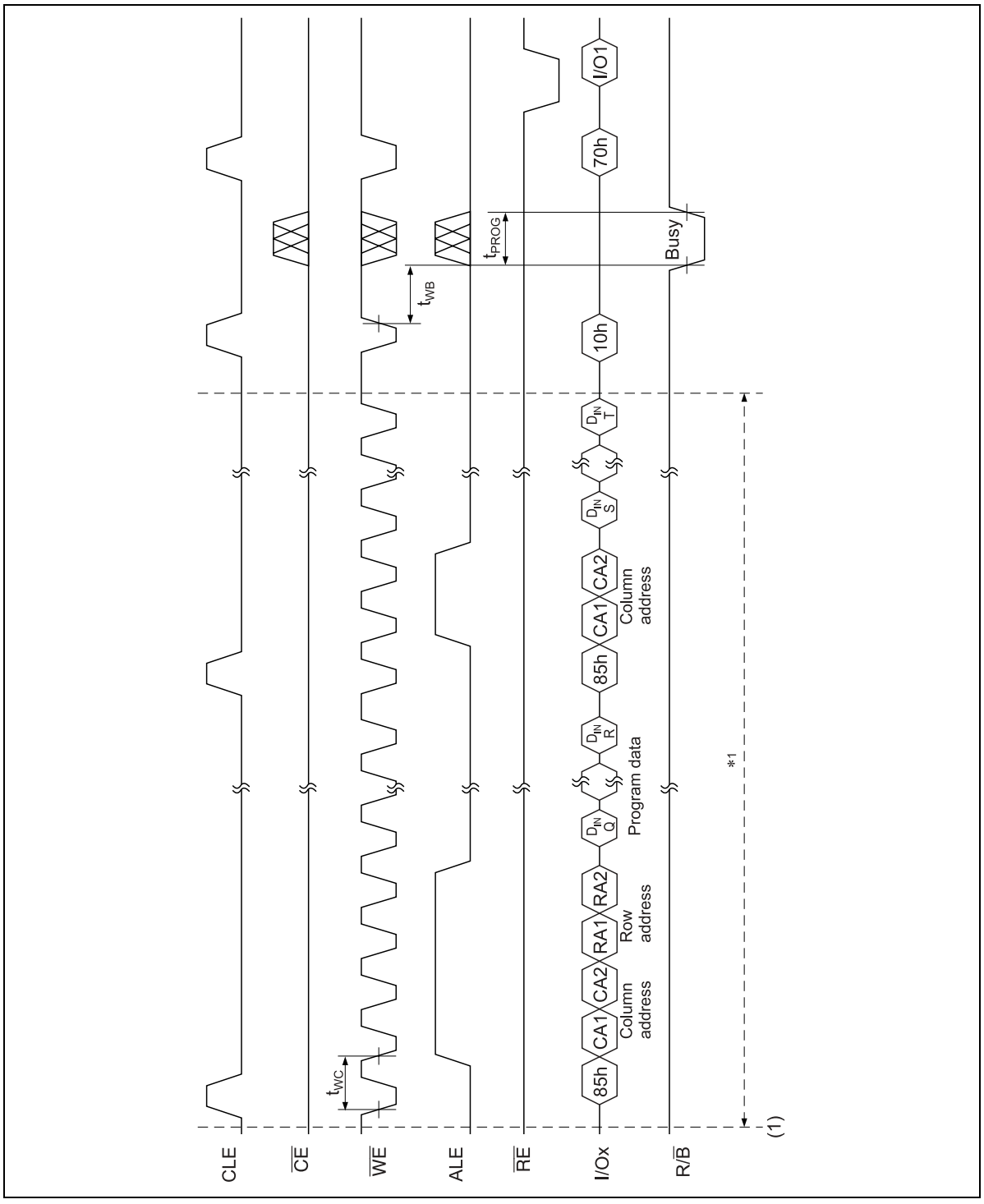
Copy Back Program Operation



Copy Back Program with Data Output (1/2)

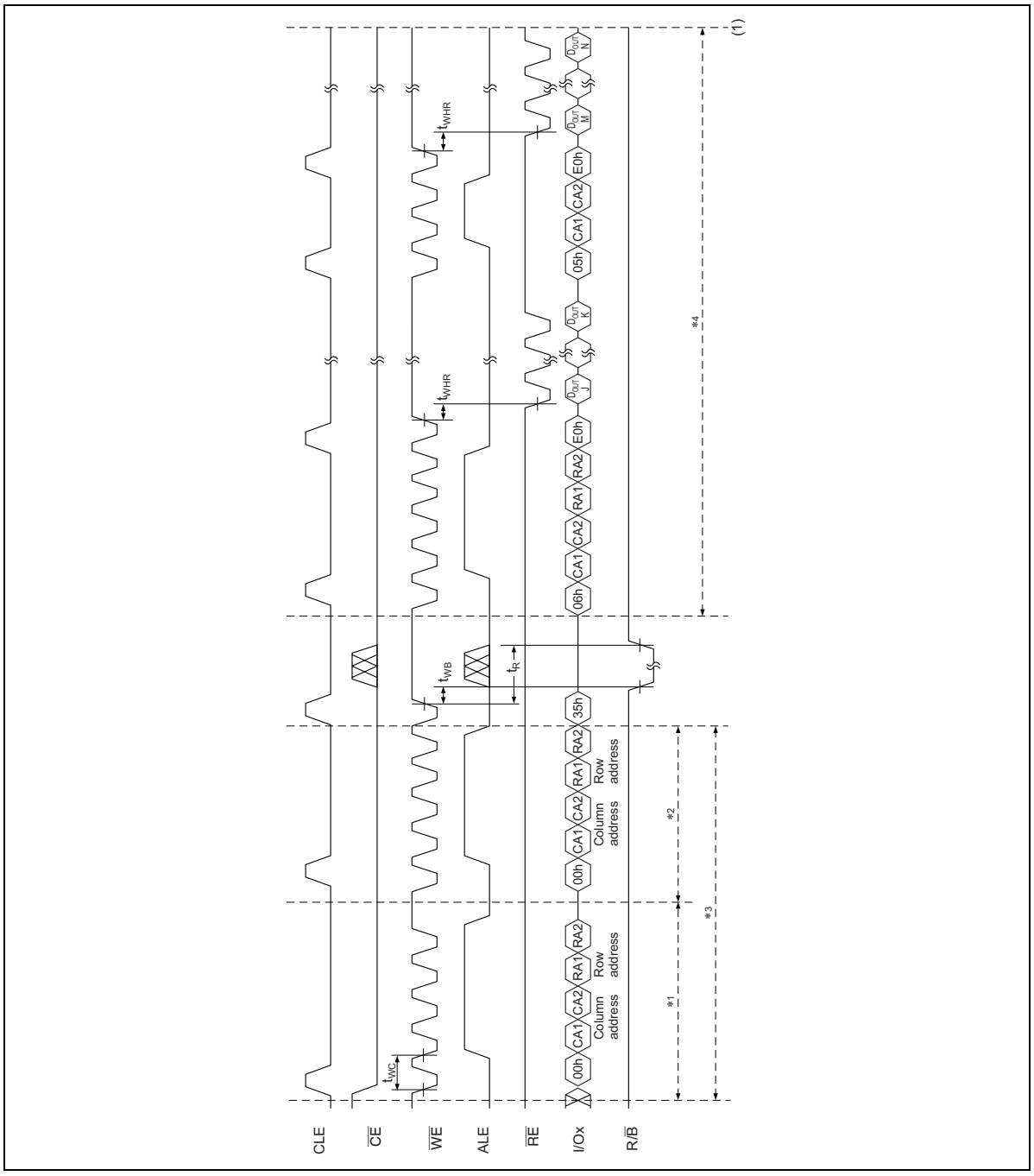


Copy Back Program with Data Output (2/2)



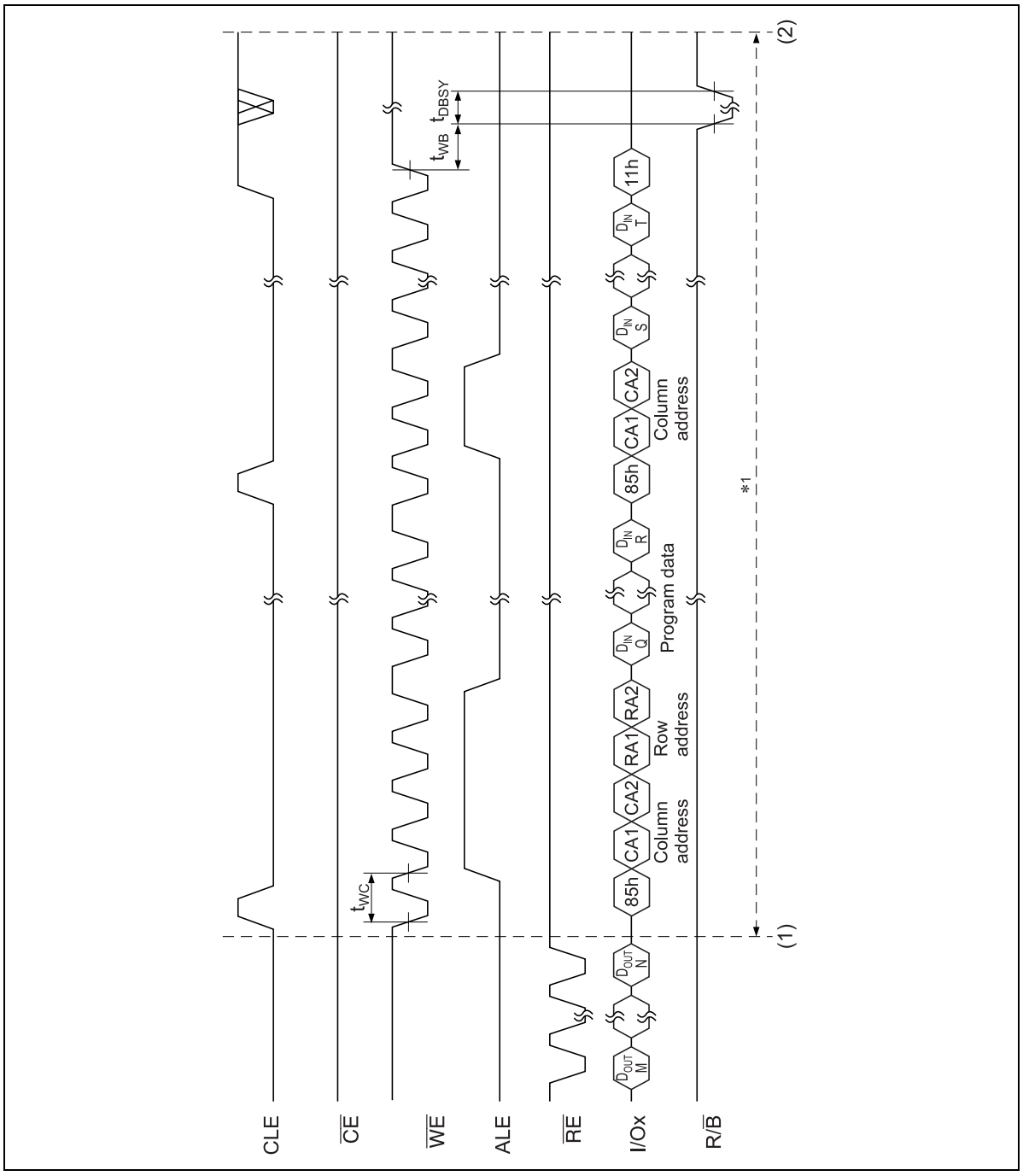
Note: 1. Updating copy data

Multi Bank Copy Back Program (1/3)



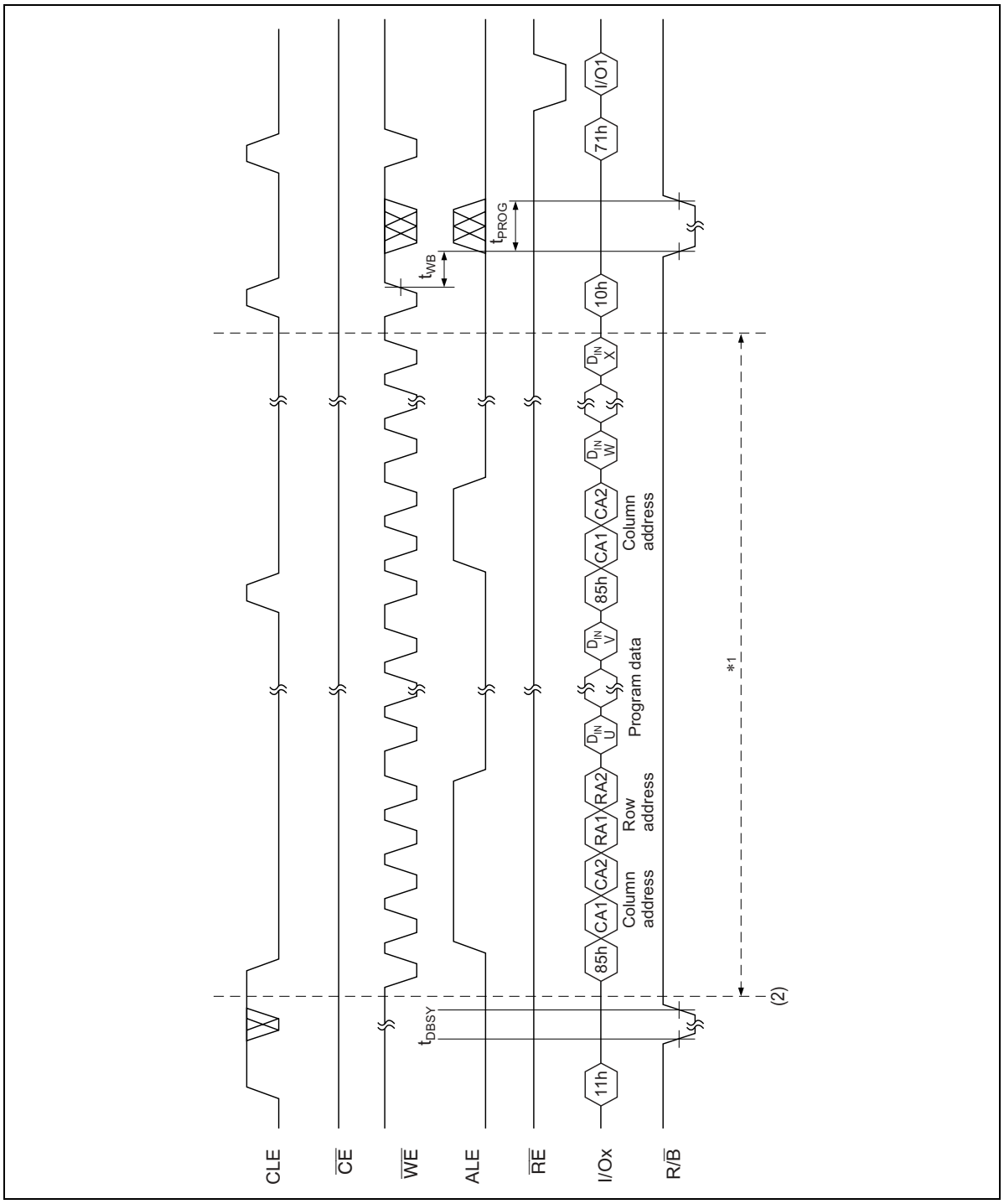
Notes: 1. Specifying the address of a source of copy.
2. Specifying the address of a source of copy.
3. A maximum 4 bank can be specified.
4. Read out the data of a source of copy.

Multi Bank Copy Back Program (2/3)



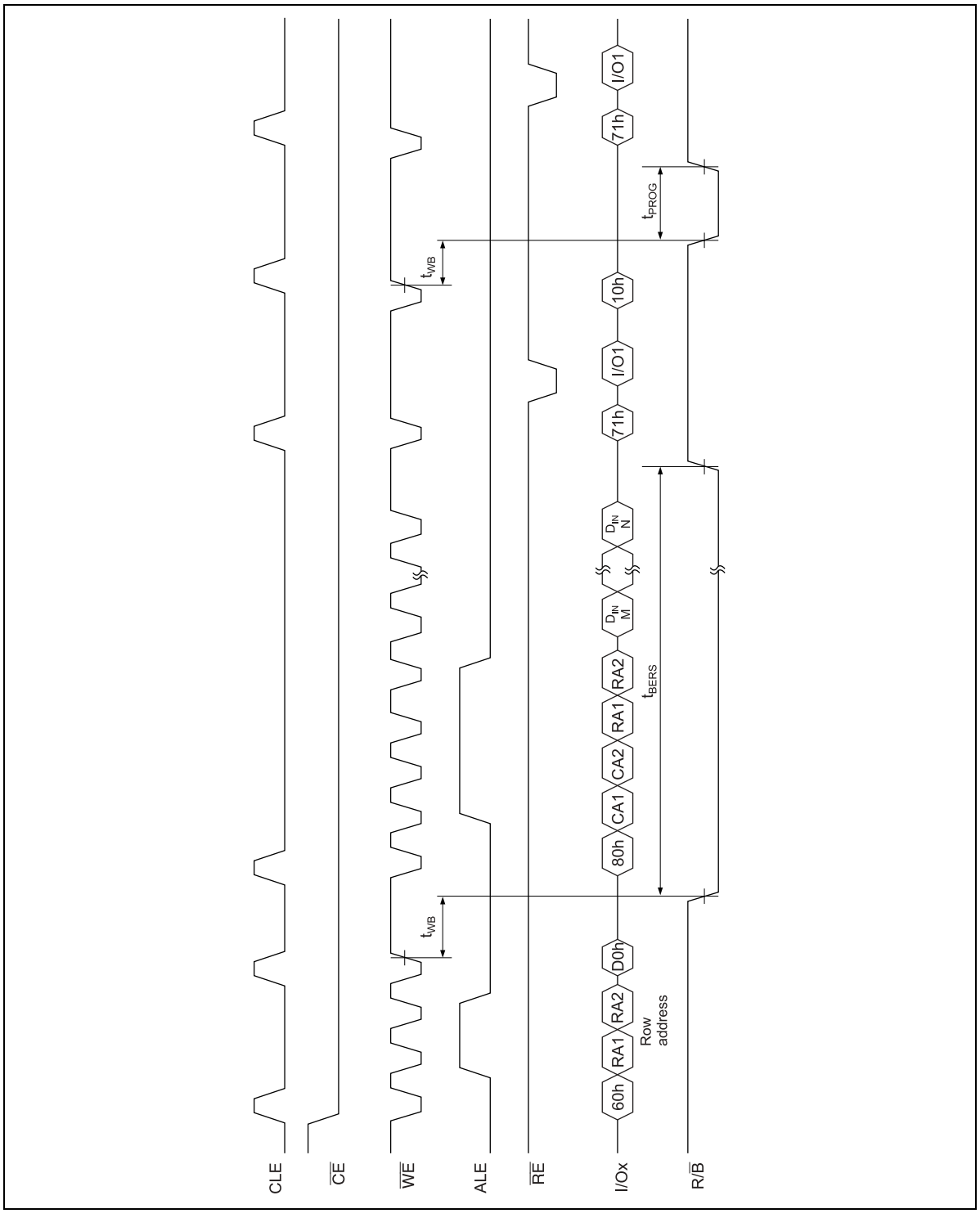
Note: 1. Updating a source data which did Copy Back Read.
Specifying Page address for post-copy.

Multi Bank Copy Back Program (3/3)

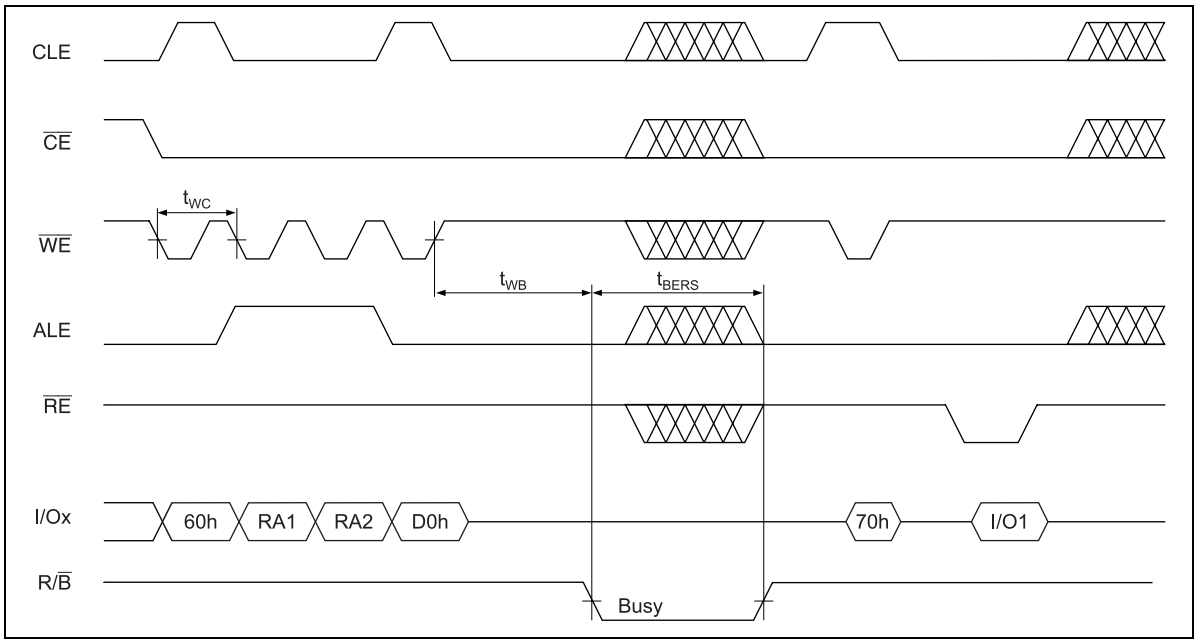


Note: 1. Updating a source data which did Copy Back Read.
Specifying Page address for post-copy.

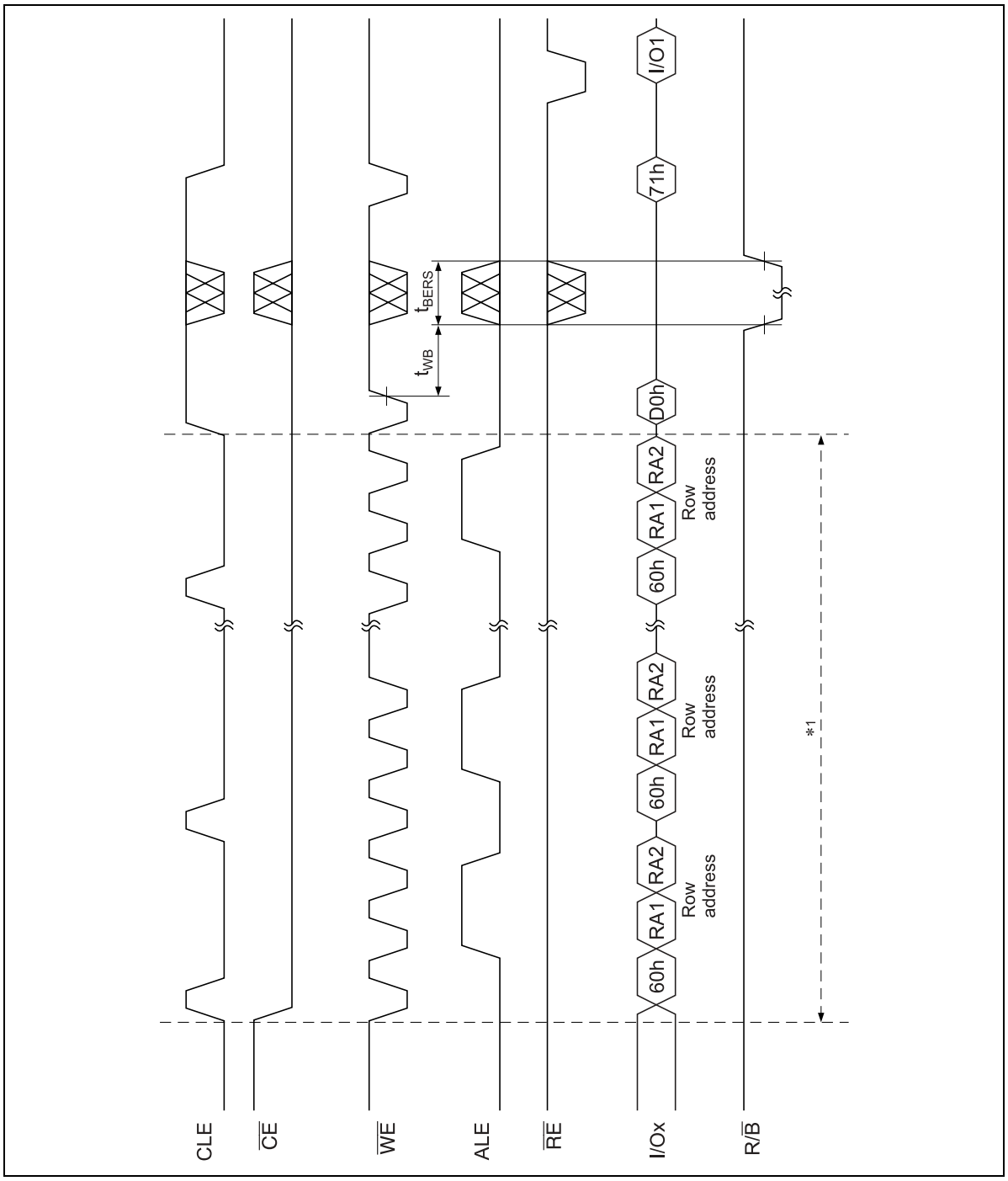
Program Data Input in Erase busy



Block Erase Operation

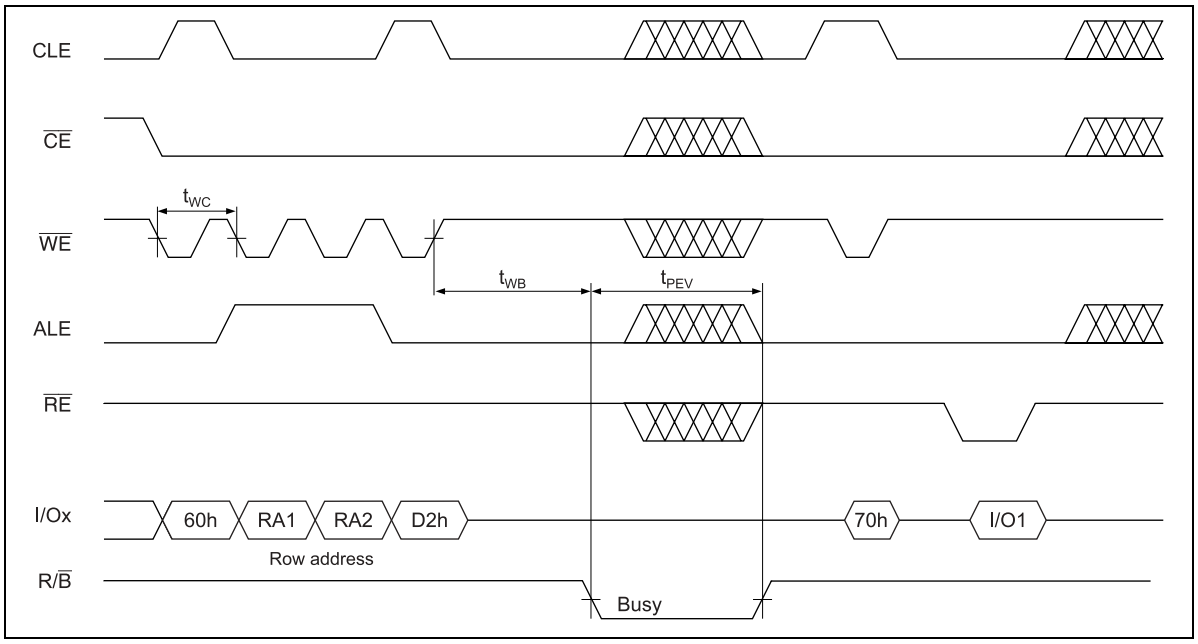


Multi Bank Block Erase

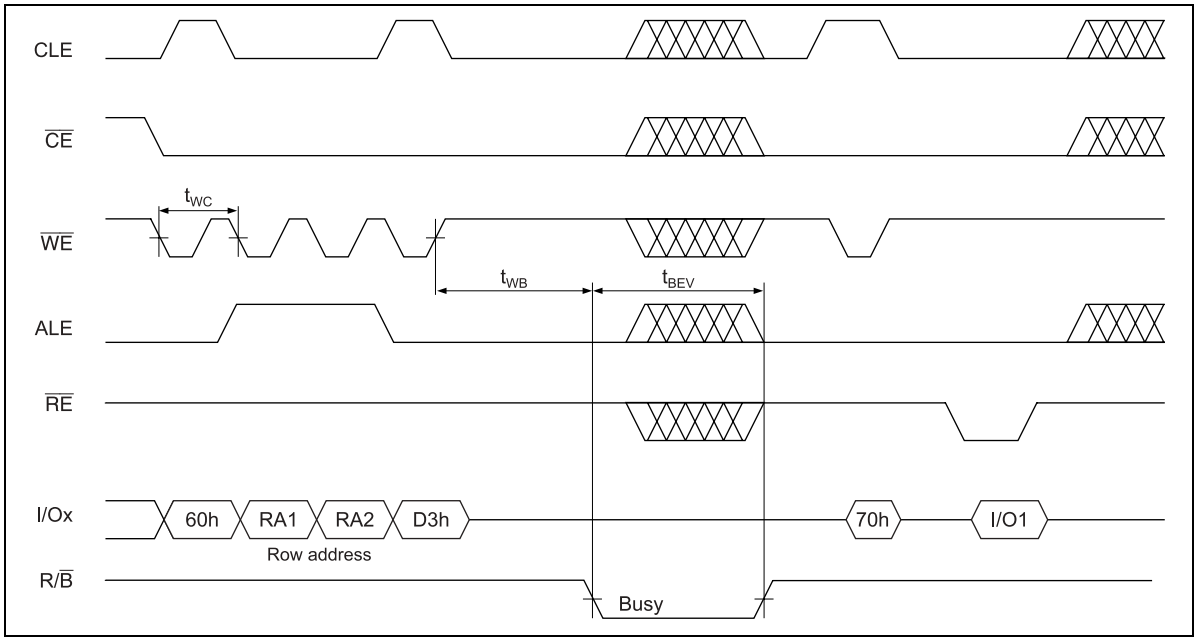


Note: 1. Possible to specify maximum 4 Bank from Bank 0 to Bank3.

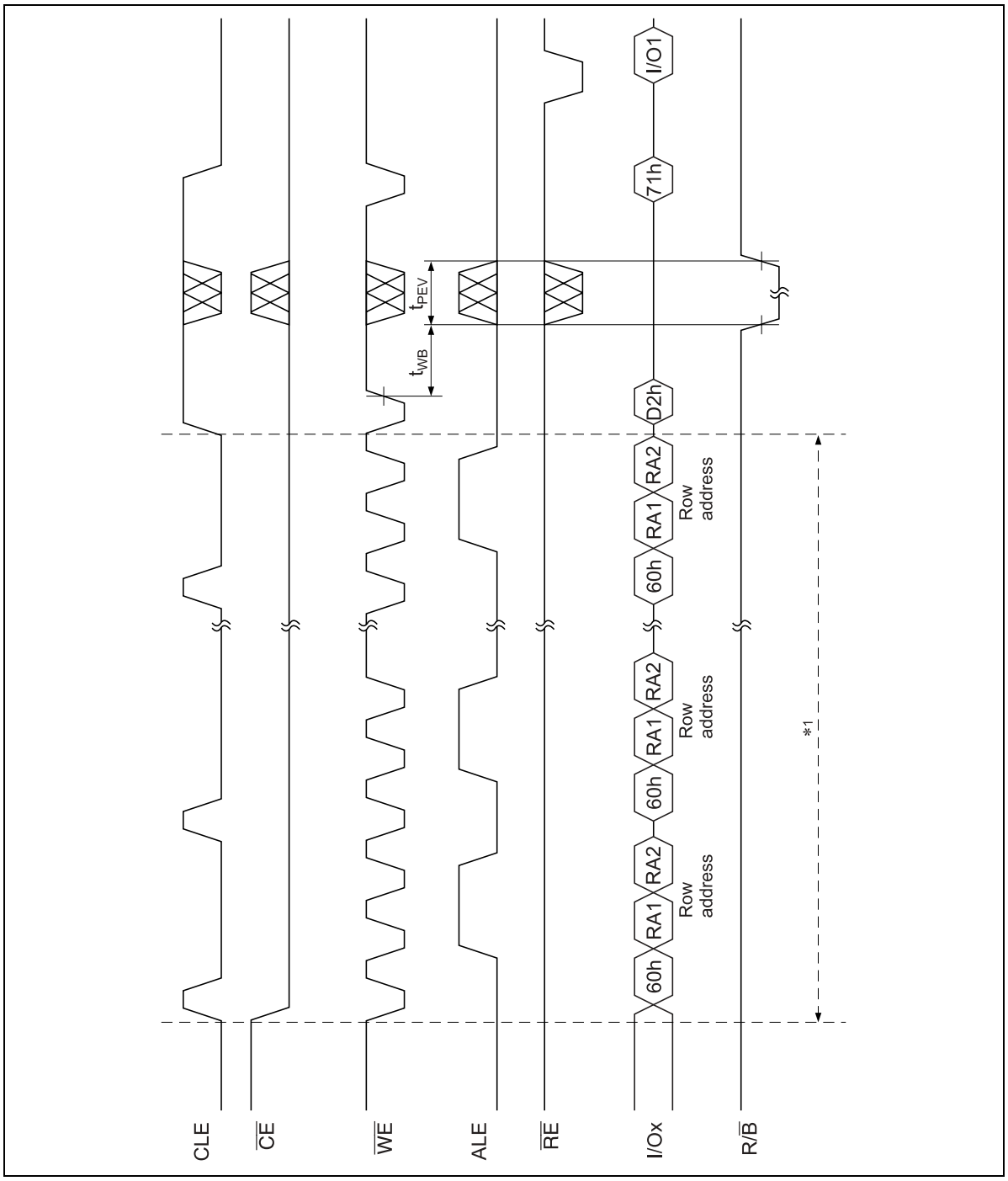
Page mode Erase Verify



Block mode Erase Verify

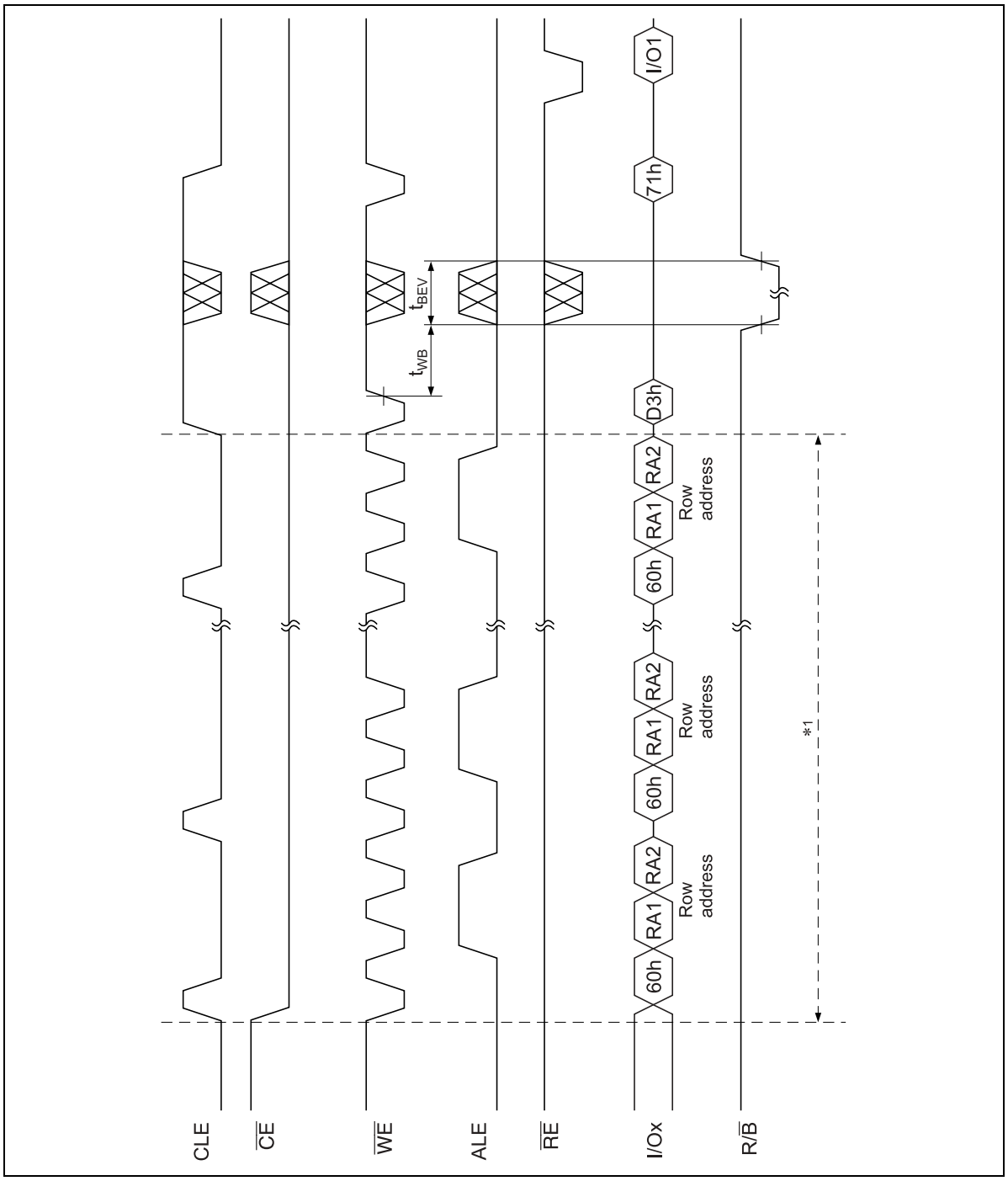


Multi Bank Page mode Erase verify



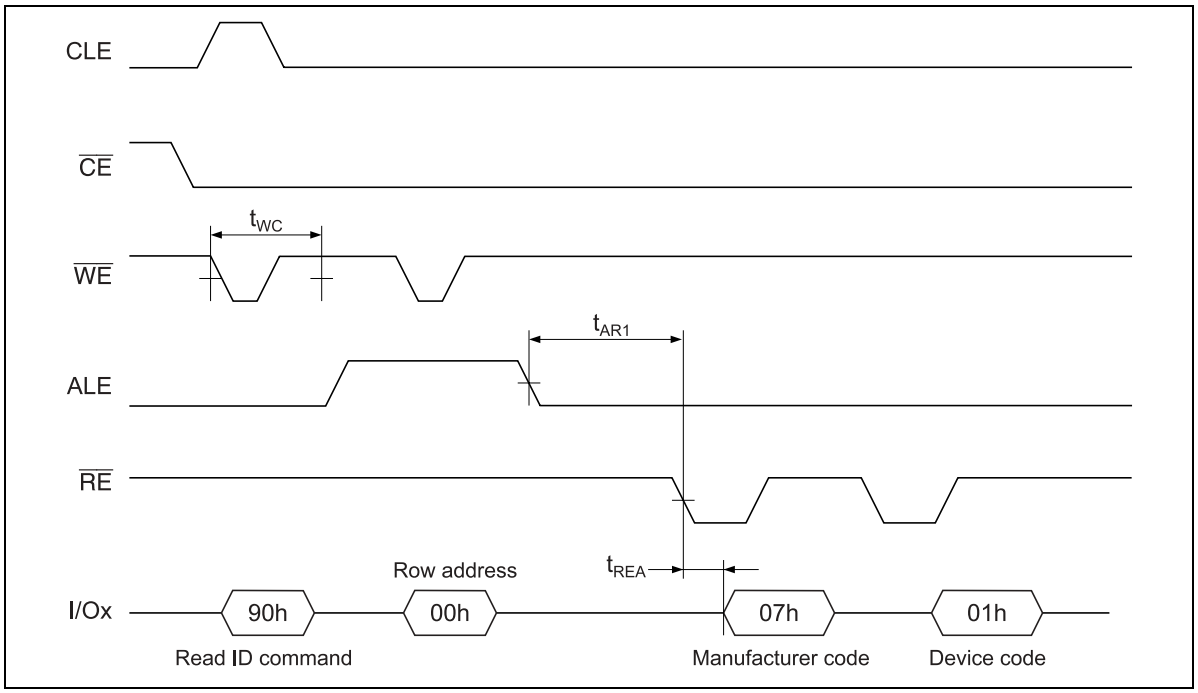
Note: 1. Possible to specify maximum 4 Bank from Bank 0 to Bank3.

Multi Bank Block mode Erase verify

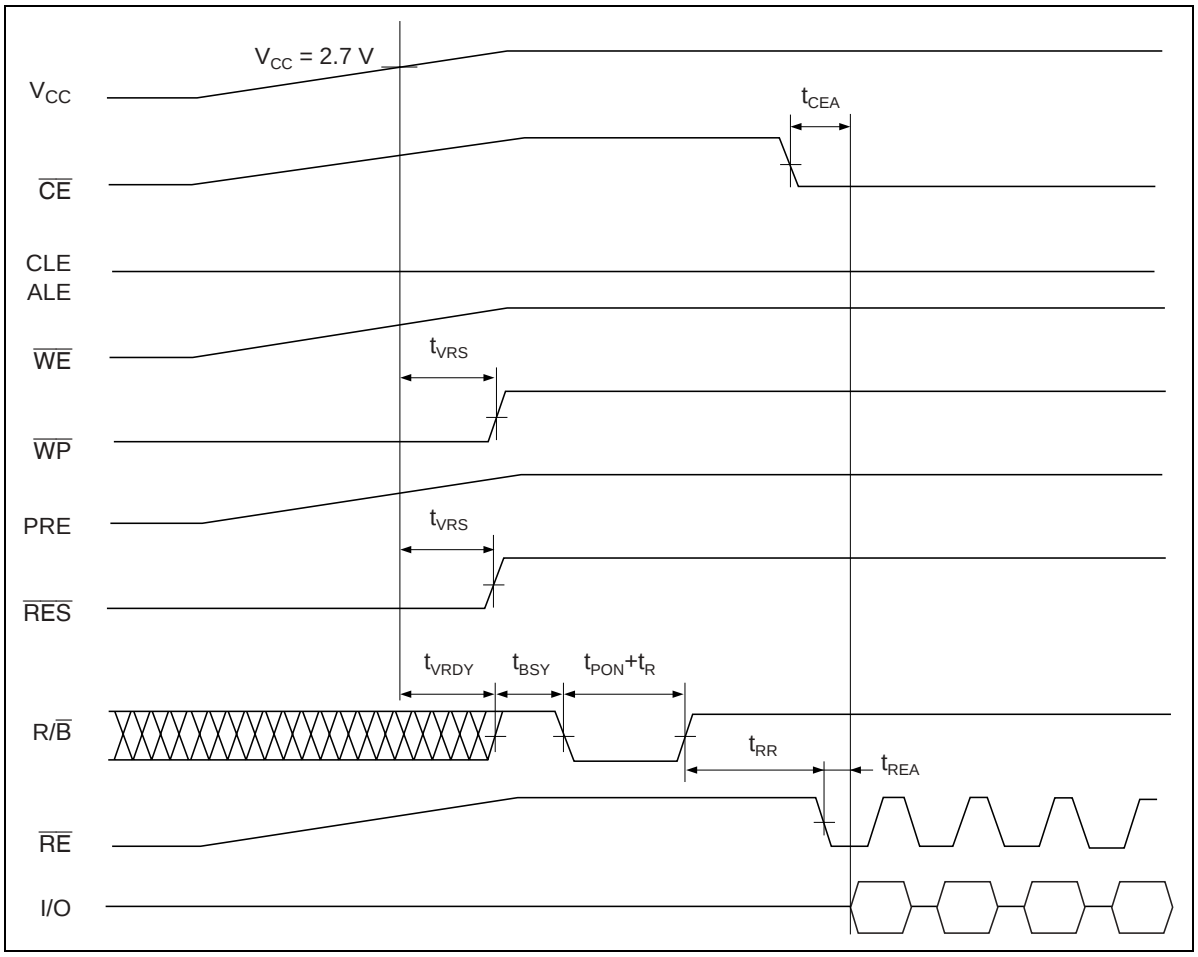


Note: 1. Possible to specify maximum 4 Bank from Bank 0 to Bank3.

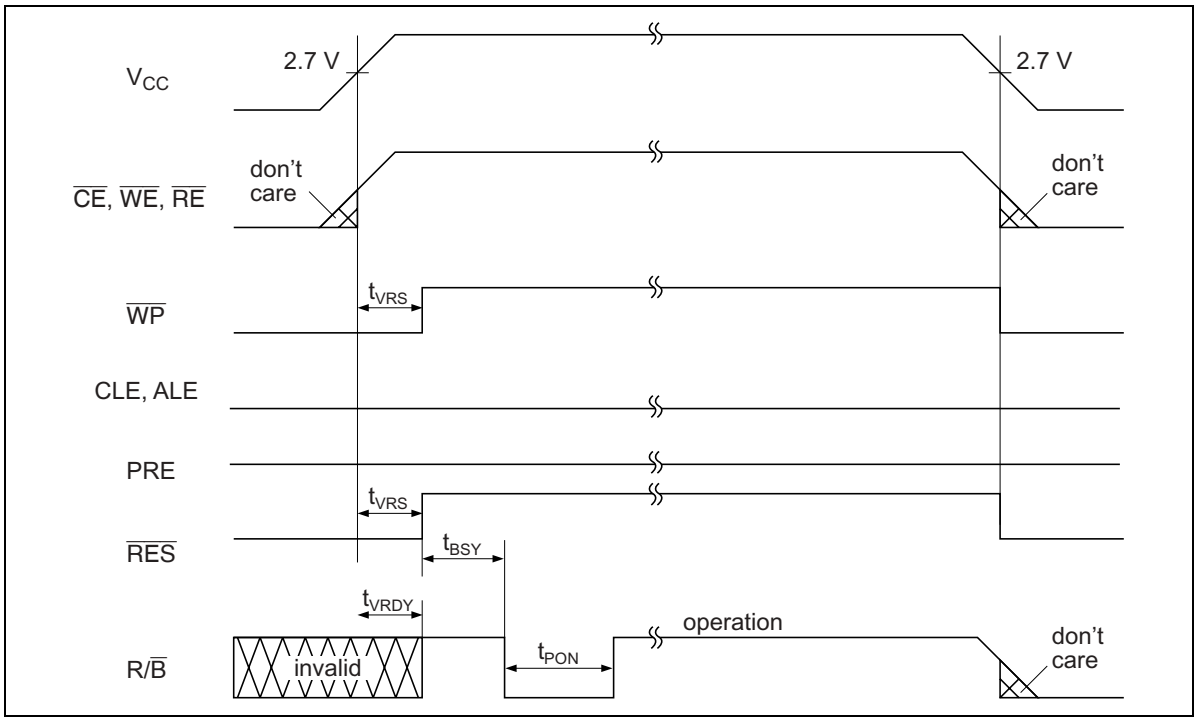
Read ID Operation



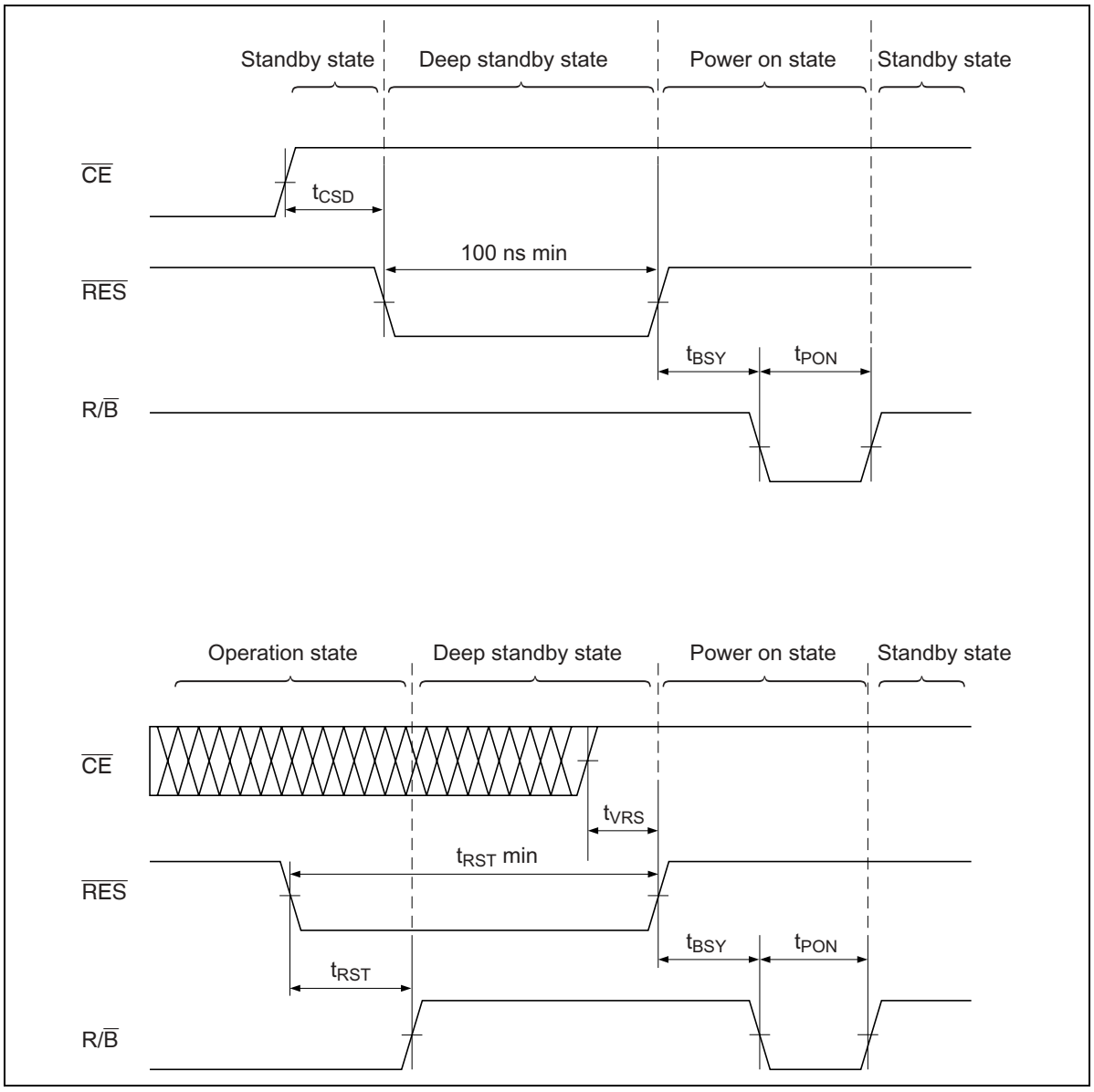
Power on Auto Read



Power on and off sequence



Deep Standby Mode



Notes on usage

1. Prohibition of undefined command input

The commands listed in the command definition can only be used in this device. It is prohibited to issue a command that is not defined in the list. If an undefined command is issued, the data held in the device may be lost.
Only the commands defined can be issued, in only defined timings. Otherwise, illegal operations may occur.

2. Limitation of command input in the busy state

In the busy state, following two commands are acceptable. Do not issue any other command except below two commands.

- Status read 70h, 71h, 72h, 73h, 74h, 75h, 76h
- Read command FFh

3. Commands limitation after commands (80h, 85h) are input at the first cycle of a program

After commands (80h, 85h) are input at the first cycle of a program, only the second cycle of the program commands (10h, 11h, 15h) and reset command (FFh) can be used. After a command 80h or 85h is input, the commands are prohibit.

4. R/$\overline{B}$ (Ready/$\overline{busy}$) pin handing

R/$\overline{B}$ pins are open-drain output pins, and they should be pulled up to V_{CC} with a resistances (more than 2kΩ).

5. Notes on $\overline{RE}$ signal

If the $\overline{RE}$ clock is sent before the address is input, the internal read operation may start unintentionally.
Be sure to send the $\overline{RE}$ clock after the address is input.
If the $\overline{RE}$ clock is input after the data of the last address is read during the read operation, invalid data is output.

6. Notes on Address taking

This product takes the address data by four cycles, and when five cycles or more are input, the address data since the fifth cycle becomes invalid.

7. Deep standby mode

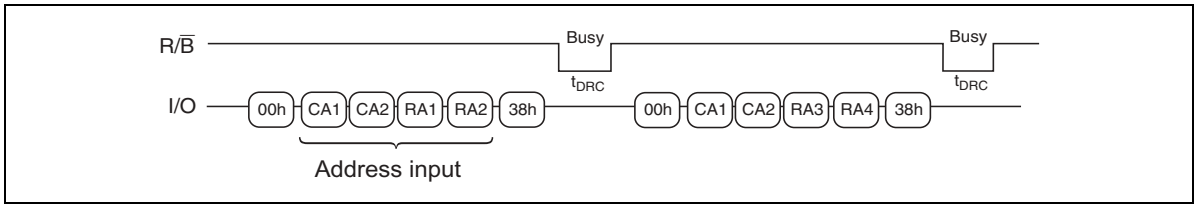
During command waiting or standby state, when $\overline{RES}$ pin goes to low, the device transfers to deep standby state.
When $\overline{RES}$ goes to high, the device returns form the deep standby state.

During command execution, going $\overline{RES}$ low stops command operation. If $\overline{RES}$ goes to low during erase/program/read operation, the command operation is forced to terminate and the applied page data is not guaranteed.

8. Notes on the power supply down

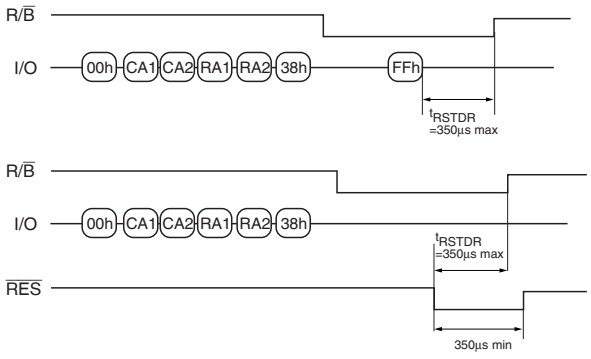
Please do not turn off a power supply in erase busy operation.
It is required to take the following measures on system side for expected power down.

When the power down is recognized to have occurred during erase busy operation, device recovery mode after the power on. The data in other blocks are protected, though the data in the applied block is invalid, by doing this.



Notes: 1. Please input any address for CA1 and CA2. Input an arbitrary address to CA1 and CA2.
2. The address input is necessary for RA1 and RA2 and RA4. Input 00h respectively. For RA3, input 04h.
3. Busy time (t_{DRC}) is as follows. When the data protect operation is unnecessary, end at the typ time in normal operation. When the data protect operation is executed, the time of 100ms or less is needed.
4. This protect operation is pause to input FF command or $\overline{RES}$ = L. In case of this pause, the protect operation is not guaranteed.

	typ	max
t_{DRC}	890µs	100ms



9. Unusable Block

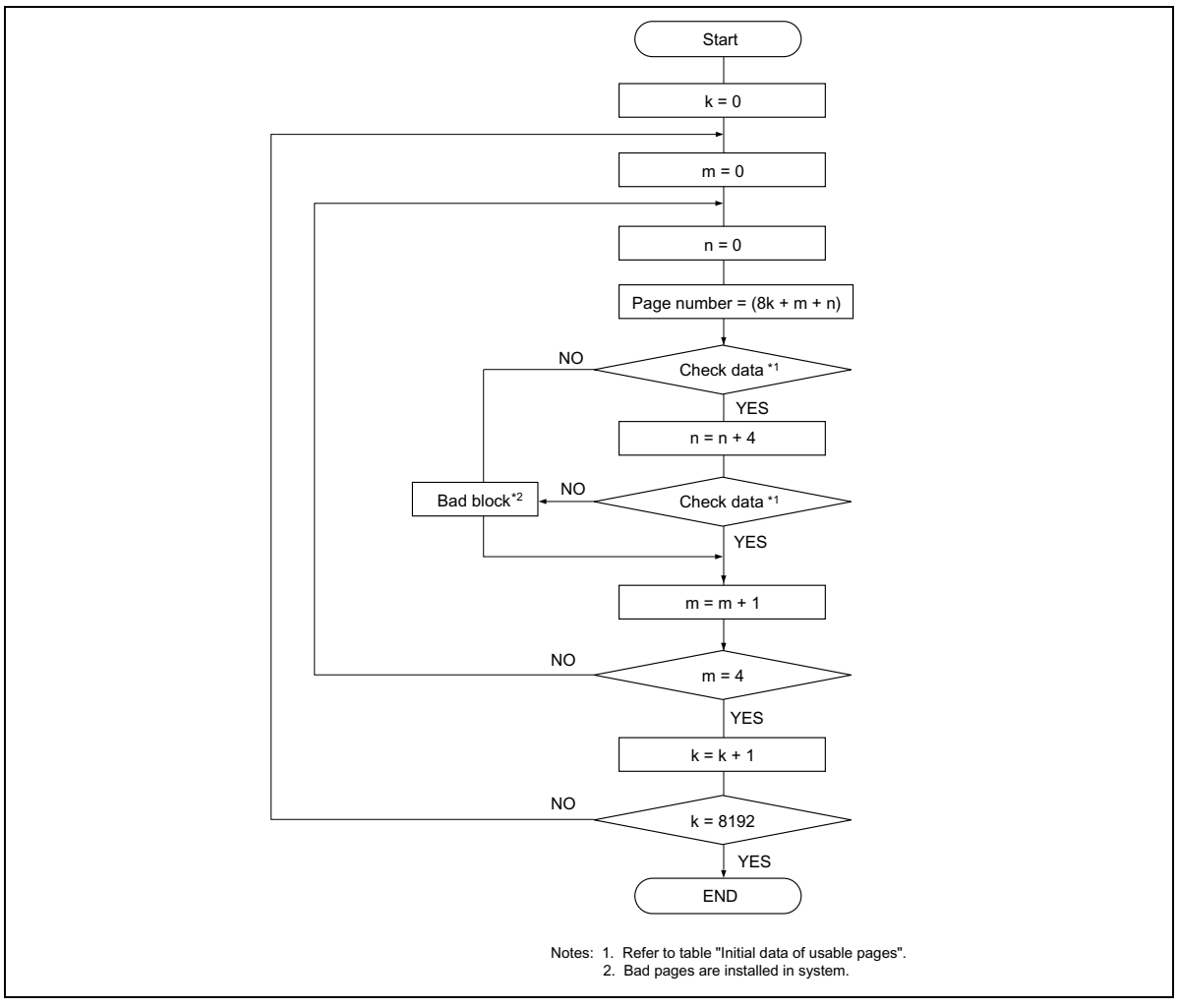
Initially, the HN29V2G74 includes unusable blocks. The usable blocks must be distinguished from the usable blocks bye the system as follows.

1. Confirm the blocks which cannot be used after mounting on the system. The following data is written on each page of the blocks which can be used. One block is composed of two pages, and following data is written in both pages commonly (Refer to "The Unusable Blocks Indication Flow").

Initial Data of Usable Pages

Column address	0h to 81Fh	820h	821h	822h	823h	824h	825h	826h to 83Fh
Data	FFh	1Ch	71h	C7h	1Ch	71h	C7h	FFh

2. Do not Program and Erase to the partial invalid blocks by the system.



The Unusable Blocks Indication Flow (per 1 chip)

10. Measures for don't care in timing waveforms for Program Data Input in Erase Busy

The timing waveforms in any mode is specified "Don't care", during $\overline{CE}$ = H other control signals become "Don't care". When $\overline{CE}$ = H, specify ALE and CLE = H, $\overline{WE}$ and $\overline{RE}$ = H.

11. Status read during read mode (data output)

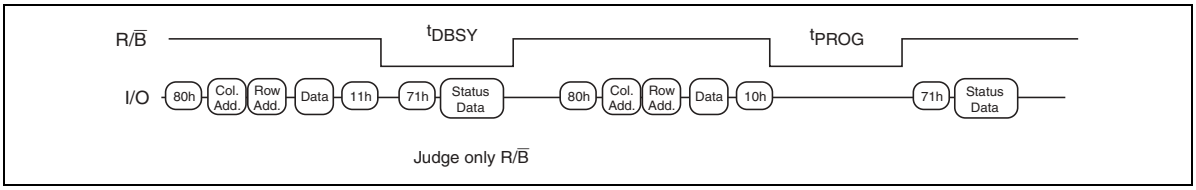
Input the status mode reset command (7Fh), when the device returns to the read mode, after the status read is executed the status read command (70h), during the busy status in the read mode.

12. Status read during read mode (data output)

The memory data cannot be output only by the $\overline{RE}$ clock, after the transition from the status read mode to the read mode by the 7Fh, when the device is set to the status read mode during the data output, in the read mode.
In this case, 06h command, column address, page address and E0h command must be input to the read operation.

13. Status read in Multibank program mode

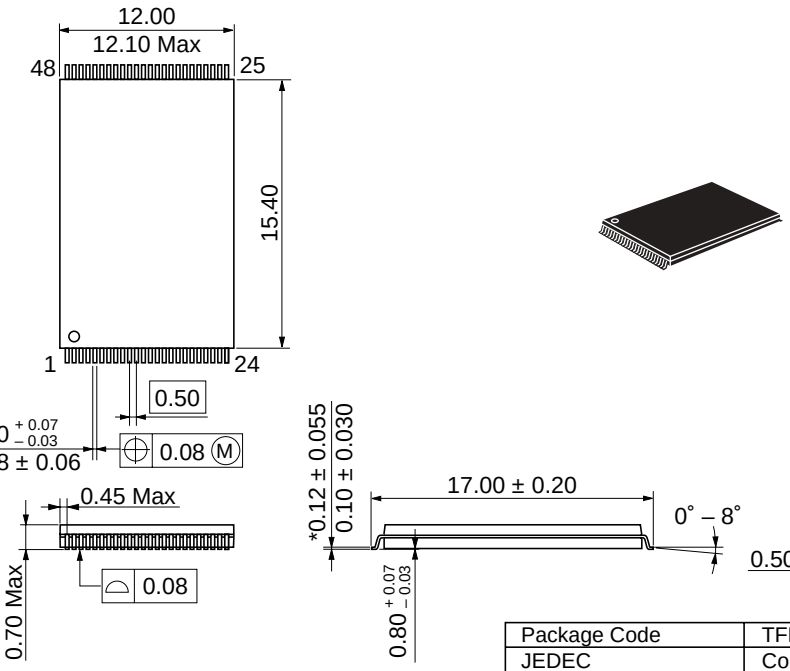
When execute status read during a dummy busy period after input command 11h in multibank program, judge only Ready/$\overline{Busy}$.



Package Dimensions

HN29V2G74WT-30 (TFP-48DBV)

Unit: mm



*Dimension including the plating thickness
Base material dimension

Package Code	TFP-48DB,TFP-48DBV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.26 g

Rev.	Date	Contents of Modification	
		Page	**Description**
0.01	Feb. 20, 2004	—	Initial issue
1.00	Jun. 18, 2004	—	Deletion of Preliminary
		—	V_{CC}: 3.0 V/3.6 V to 2.7 V/3.6 V
		1, 53	t_R Max (1st access time): 100µs to120µs
		9	Program/Erase Characteristics t_{PROG} Max: 1ms to 2.4 ms t_{CPROG} Max: 2ms to 4.8 ms t_{CBSY} Max: 1000µs to 2400 µs t_{BERS} Max: 2.4ms to 20 ms
		88	Notes on usage: Change of 8. Notes: 2., 4. Change of description "The address input is necessary for RA1 and RA2. Input 00h respectively." to "The address input is necessary for RA1 and RA2 and RA4. Input 00h respectively." "For RA3 and RA4, input 04h respectively." to "For RA3, input 04h." "Before confirmation of this command, the protect operation is not guaranteed." to "In case of this pause, the protect operation is not guaranteed."
2.00	Jul. 21, 2004	53	AC Characteristics t_{VRS} Min: 20µs to 100µs t_{VRDY} Max: 20µs to 100µs

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
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Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Colophon .1.0