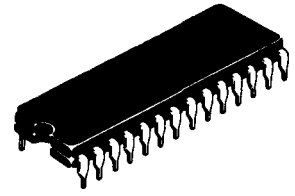
HN613128P, HN613128FP

16384-word×8-bit Mask Programmable Read Only Memory

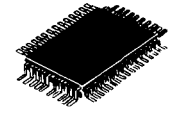
The HN613128P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The active level of the CS, OE_0, OE_1 input and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.

HN613128P



(DP-28)

HN613128FP

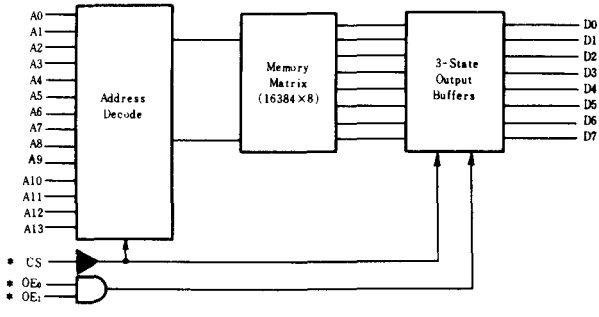


(FP-54)

■FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5-Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Select, Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation;
  Standby: 5μW (typ.)
  Operation: 50mW (typ.)
- Pin Compatible with EPROM

■BLOCK DIAGRAM



* Active level defined by the user.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
Input Voltage*	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range (under bias)	T_{bias}	−20 to +85	°C

* With respect to V_{SS}.

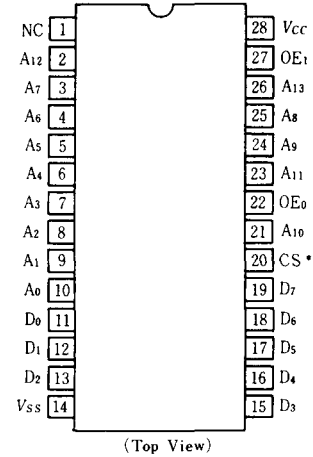
■RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	−20	—	75	°C

* With respect to V_{SS}.

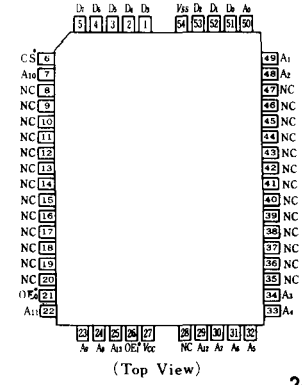
■PIN ARRANGEMENT

●HN613128P



(Top View)

●HN613128FP



(Top View)

■ ELECTRICAL CHARACTERISTICS (V_{CC}=5.0V±10%, V_{SS}=0V, Ta=−20 to +75°C)

Item	Symbol	Test Condition	min	typ**	max	Unit
Input High-level Voltage	V_{IH}		2.2	—	V_{CC}	V
Input Low-level Voltage	V_{IL}		−0.3	—	0.8	V
Output High-level Voltage	V_{OH}	I_{OH}=−205μA	2.4	—	—	V
Output Low-level Voltage	V_{OL}	I_{OL}=3.2mA	—	—	0.4	V
Input Leakage Current	I_{LI}	V_{in}=0 to 5.5V	—	—	2.5	μA
Output High-level Leakage Current	I_{LOH}	V_{out}=2.4V, CS=0.8V, $\overline{CS}$=2.2V	—	—	10	μA
Output Low-level Leakage Current	I_{LOL}	V_{out}=0.4V, CS=0.8V, $\overline{CS}$=2.2V	—	—	10	μA
Supply Current (Active/Standby)	I_{CC}*/ I_{SB}	V_{CC}=5.5V, I_{DOUT}=0mA, t_{RC}=min, duty=100%/$\overline{CS}$≥V_{CC}−0.2V, CS≤0.2V	—	10/1	25/30	mA/μA
Input Capacitance	C_{in}	V_{in}=0V, f=1.0MHz, Ta=25°C	—	—	10	pF
Output Capacitance	C_{out}	V_{in}=0V, f=1.0MHz, Ta=25°C	—	—	15	pF

* Steady state current ** V_{CC}=5V, T_a=25°C

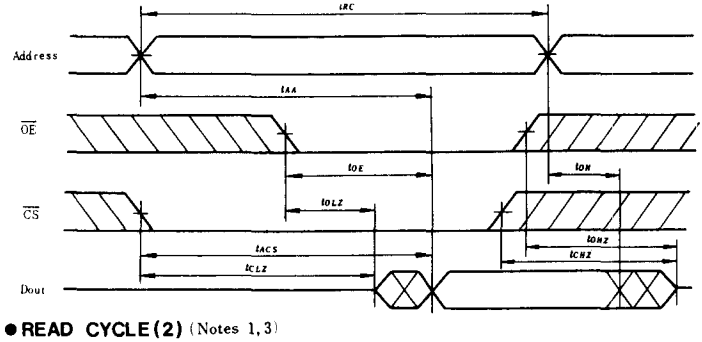
■ RECOMMENDED AC OPERATING CONDITIONS (READ SEQUENCE)

(V_{CC}=5.0V±10%, V_{SS}=0V, Ta=−20 to +75°C, All timing with t_r=t_f=20ns)

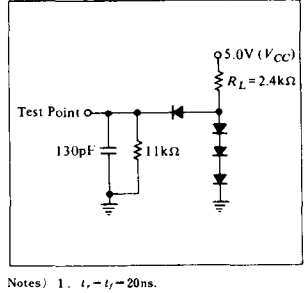
Item	Symbol	HN613128P		Unit
		min	max	
Read Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{AA}	—	250	ns
Chip Select Access Time	t_{ACS}	—	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	ns
Output Enable to Output Valid	t_{OE}	—	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	ns
Chip deselection to Output in High Z	t_{CHZ}	0	100	ns
Chip Disable to Output in High Z	t_{OHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	—	ns

■ TIMING WAVEFORM

● READ CYCLE (1)

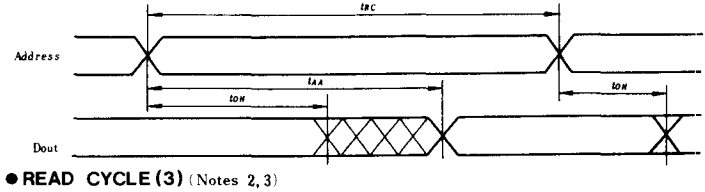


● AC TEST LOAD

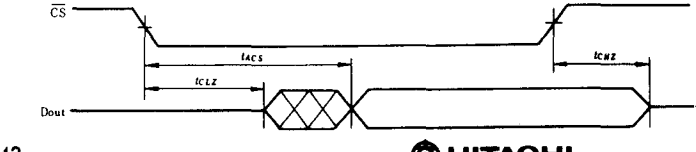


Notes) 1. t_r=t_f=20ns.
2. C_L includes jig capacitance.
3. All diodes are 1S2074Ⓗ.

● READ CYCLE (2) (Notes 1, 3)



● READ CYCLE (3) (Notes 2, 3)



NOTES:
1. Device is continuously selected.
2. Address Valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{OE}$ = *VIL*.
4. Input pulse level: 0.8 to 2.4V
5. Input and output reference level: 1.5V

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