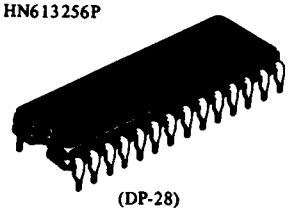
32768-word x 8-bit CMOS Mask Programmable Read Only Memory

The HN613256P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized system.

To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.

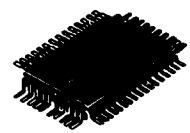
The active level of the CS and OE input, and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.

HN613256P



(DP-28)

HN613256FP

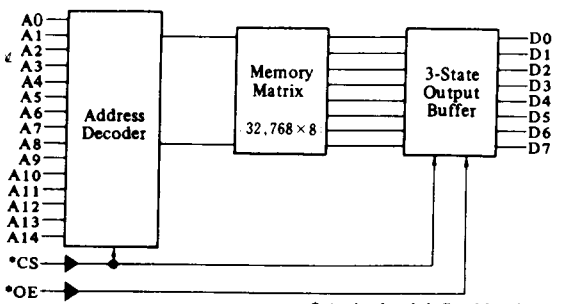


(FP-54)

■ FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time: 250ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ.), Operation 50mW (typ.)
- Pin Compatible with EPROM

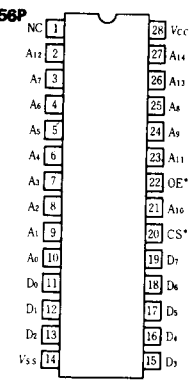
■ BLOCK DIAGRAM



* Active level defined by the user.

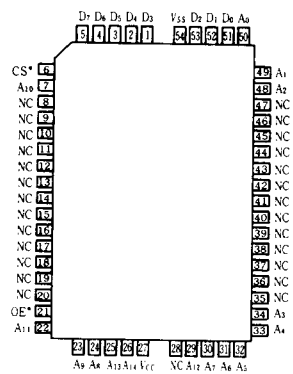
■ PIN ARRANGEMENT

● HN613256P



(Top View)

● HN613256FP



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	−0.3 to +7.0	V
All Input and Output Voltage*	V_T	−0.3 to +7.0	V
Operating Temperature Range	T_{opr}	−20 to +75	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range (Under Bias)	T_{bias}	−20 to +85	°C

*With respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	−0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	−20	—	75	°C

* With respect to V_{SS}.

HITACHI
Hitachi America Ltd. • 2210 O'Toole Avenue • San Jose, CA 95131 • (408) 435-8300

■ ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V±10%, V_{SS} = 0V, T_a = −20 ~ +75 °C)

Item		Symbol	Test Condition		min	typ**	max	Unit
Input Voltage		V_{IH}			2.2	–	V_{CC}	V
		V_{IL}			−0.3	–	0.8	V
Output Voltage		V_{OH}	I_{OH} = −205 µA		2.4	–	–	V
		V_{OL}	I_{OL} = 3.2 mA		–	–	0.4	V
Input Leakage Current		I_{LI}	V_{in} = 0 ~ 5.5V		–	–	2.5	µA
Output Leakage Current		I_{LOH}	CS = 0.8V, $\overline{CS}$ = 2.2V	V_{out} = 2.4V	–	–	10	µA
		I_{LOL}		V_{out} = 0.4V	–	–	10	µA
Supply Current	Active	I_{CC}*	V_{CC} = 5.5V, I_{out} = 0mA, t_{RC} = min, duty = 100%		–	15	30	mA
	Standby	I_{SB}	V_{CC} = 5.5V, $\overline{CS} \geq V_{CC}$ − 0.2V, CS ≦ 0.2V		–	1	30	µA
Input Capacitance		C_{in}***	V_{in} = 0V, f = 1 MHz, T_a = 25 °C		–	–	10	pF
Output Capacitance		C_{out}***			–	–	15	pF

* Steady state current *** This parameter is sampled and not 100% tested.
** V_{CC}=5V, T_a=25°C

■ AC CHARACTERISTICS (READ CYCLE)

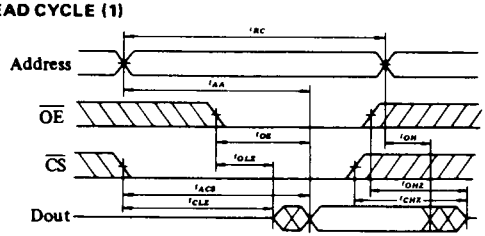
(V_{CC}=5V±10%, V_{SS}=0V, Ta=−20~+75°C, t_r=t_f=20ns)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	250	–	ns
Address Access Time	t_{AA}	–	250	ns
Chip Select Access Time	t_{ACS}	–	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	ns
Output Enable to Output Valid	t_{OE}	–	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	100	ns
Output Disable to Output in High Z	t_{OHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	–	ns

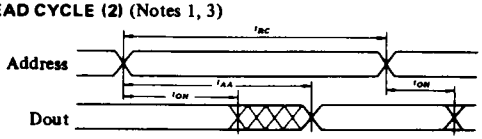
* t_{HZ} and t_{HZ} defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.

■ TIMING WAVEFORM

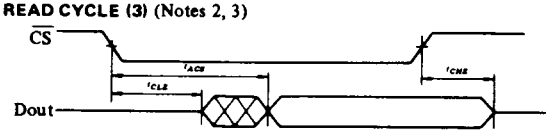
• READ CYCLE (1)



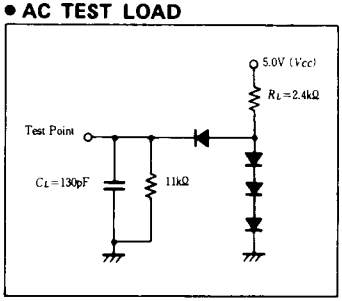
• READ CYCLE (2) (Notes 1, 3)



• READ CYCLE (3) (Notes 2, 3)



• AC TEST LOAD



Notes : 1. t_r = t_f = 20ns
2. C_L includes jig capacitance
3. All diodes are 1S2074Ⓗ

NOTES:
1. Device is continuously selected.
2. Address Valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{OE}$ = V_{IL}.
4. Input pulse level: 0.8 to 2.4V
5. Input and output reference level: 1.5V