

Shantou Huashan Electronic Devices Co.,Ltd.

NPN DARLINGTON TRANSISTOR

HP142T

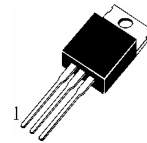
APPLICATIONS

High DC Current Gain

ABSOLUTE MAXIMUM RATINGS ($T_a=25^{\circ}\text{C}$)

T_{stg} —Storage Temperature	—55~150 $^{\circ}\text{C}$
T_j —Junction Temperature	150 $^{\circ}\text{C}$
P_C —Collector Dissipation ($T_c=25^{\circ}\text{C}$)	80W
V_{CBO} —Collector-Base Voltage	100V
V_{CEO} —Collector-Emitter Voltage	100V
V_{EBO} —Emitter-Base Voltage	5V
I_C —Collector Current (DC)	10A
I_B —Base Current	0.5A

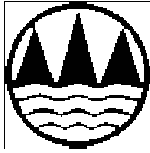
TO-220



1 — Base, B
2 — Collector, C
3 — Emitter, E

ELECTRICAL CHARACTERISTICS ($T_a=25^{\circ}\text{C}$)

Symbol	Characteristics	Min	Typ	Max	Unit	Test Conditions
$BV_{\text{CEO(SUS)}}$	Collector-Emitter Sustaining Voltage	100			V	$I_C=30\text{mA}$, $I_B=0$
I_{CEO}	Collector Cutoff Current			2	mA	$V_{\text{CE}}=50\text{V}$, $I_B=0$
I_{CBO}	Collector Cutoff Current			1	mA	$V_{\text{CB}}=100\text{V}$, $I_E=0$
I_{EBO}	Emitter-Base Cutoff Current			2	mA	$V_{\text{EB}}=5\text{V}$, $I_C=0$
$H_{\text{FE}}(1)$	DC Current Gain	1000				$V_{\text{CE}}=4\text{V}$, $I_C=5\text{A}$
$H_{\text{FE}}(2)$		500				$V_{\text{CE}}=4\text{V}$, $I_C=10\text{A}$
$V_{\text{CE(sat1)}}$	Collector- Emitter Saturation Voltage			2	V	$I_C=5\text{A}$, $I_B=10\text{mA}$
$V_{\text{CE(sat2)}}$				3	V	$I_C=10\text{A}$, $I_B=40\text{mA}$
$V_{\text{BE(sat)}}$	Base- Emitter Saturation Voltage			3.5	V	$I_C=10\text{A}$, $I_B=40\text{mA}$
$V_{\text{BE(on)}}$	Base- Emitter On Voltage			3	V	$V_{\text{CE}}=4\text{V}$, $I_C=10\text{A}$,
t_D	Deiay time		0.15		μS	$V_{\text{CC}}=30\text{V}$, $I_C=5\text{A}$ $I_{B1}=20\text{mA}$ $I_{B2}=-20\text{mA}$
t_R	Rise Time		0.55		μS	
t_S	Storage Time		2.5		μS	
t_F	Fall Time		2.5		μS	



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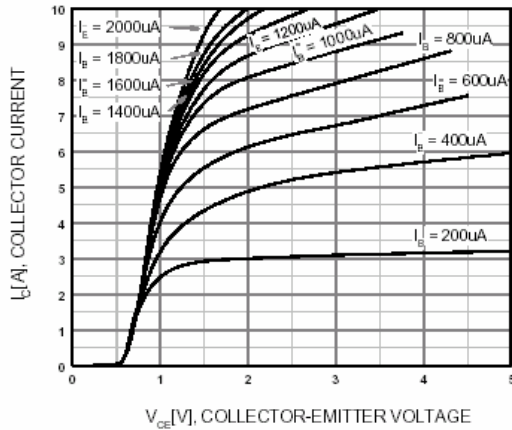


Figure 1. Static Characteristic

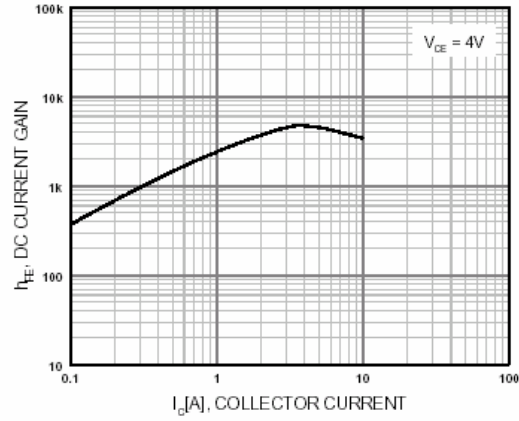


Figure 2. DC current Gain

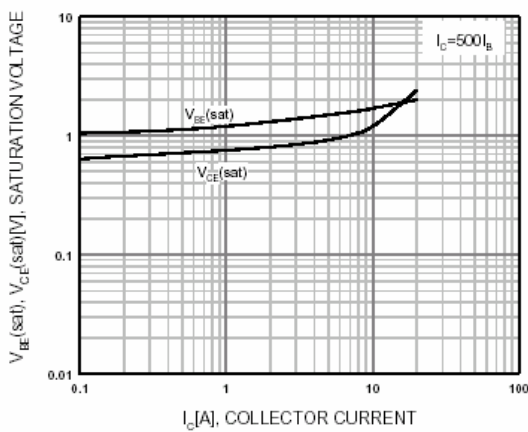


Figure 3. Collector-Emitter Saturation Voltage
Base-Emitter Saturation Voltage

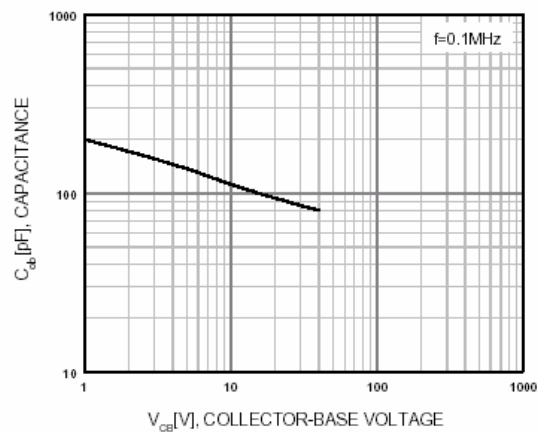


Figure 4. Collector Output Capacitance

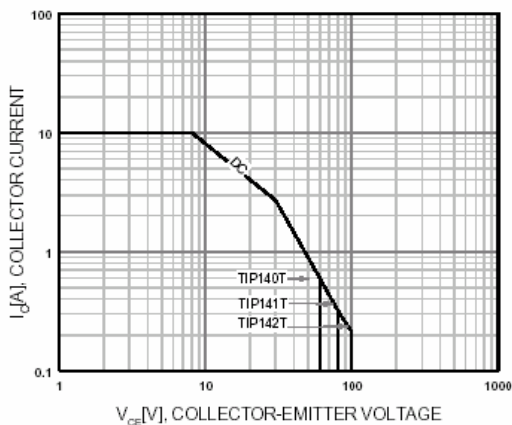


Figure 5. Safe Operating Area

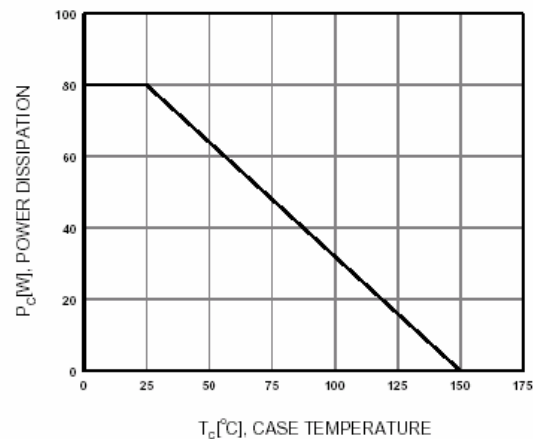


Figure 6. Power Derating