Silicon Bipolar Monolithic QPSK Modulator

Technical Data

HPMX-2001

Features

- **I/Q Bandwidth: DC - 700 MHz**
- **LO Frequency Range: DC-2000 MHz**
- **Standby Mode - P_d 10 mW**
- **Low Cost Plastic Surface Mount Package**

Applications

- **Digital Cellular Radio (eg., GSM, ADC)**
- **RF Data Links**
- **Vector Generators**
- **AM Modulator**
- **Single Sideband Mixer**

Description

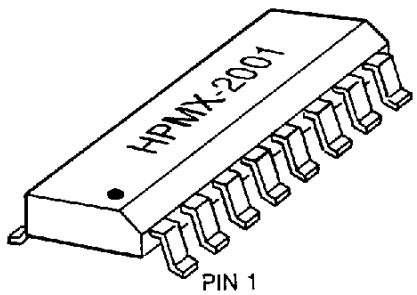
The HPMX-2001 is a silicon monolithic quadrature phase shift keyed modulator in a plastic surface mount SO-16 package. It is designed for wide or narrow band applications and has a typical LO operating frequency range of DC-2000 MHz and typical I/Q bandwidth of DC-700 MHz.

The modulator may be operated in any combination of single or differential input/output configurations. The LO inputs are self biasing and have 50 Ohm termination impedances. The I & Q inputs are open base and require 2.5 V DC bias. This allows direct coupling to the I & Q inputs. The RF output is designed to drive a 50 Ohm load and has a saturated output power level of -5.5 dBm.

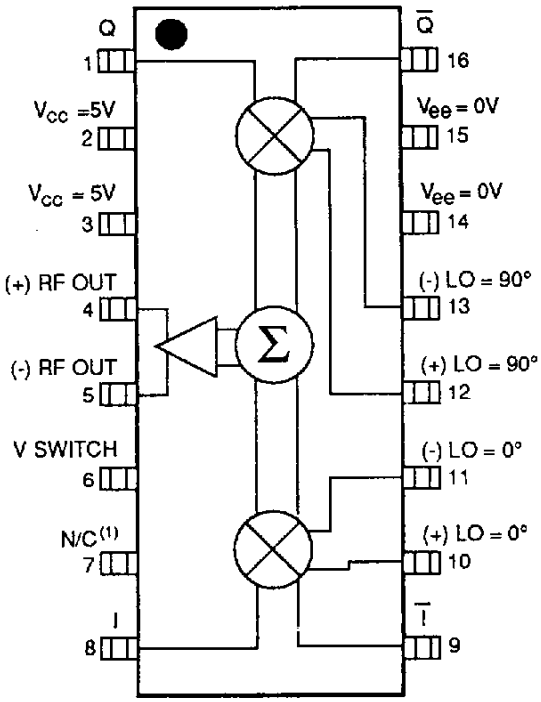
The internal signal paths of the modulator are fully differential to help reduce susceptibility to common mode noise. The small amplitude and phase imbalance of the device, 0.5 dB and 1 degree respectively, makes the modulator suitable for many communication applications. The HPMX-2001 also features a standby mode in which the device consumes only 10 mW of power.

The HPMX-2001 is manufactured using Hewlett-Packard's 13 GHz F_t, 25 GHz F_{max} silicon bipolar integrated circuit process.

Plastic SO-16 Package



Functional Block Diagram and Pin Configuration



NOTE 1: DO NOT GROUND PIN 7.

HPMX-2001 Absolute Maximum Ratings, T_A = 25°C*

Symbol	Parameter	Units	Maximum
V_{cc}	Supply Voltage	Volts	6
V_{in} I/Q	I/Q Input Voltage	Volts P-P	4
P_{in} LO	LO Input Power	dBm	10
V_{sw}	Standby Switch Voltage	Volts	6
T_{op}	Ambient Operating Temperature	°C	-55 to +85
T_{stg}	Storage Temperature	°C	-55 to +150

*Operation in excess of any one of these conditions may result in permanent damage to this device.

Care should be taken to prevent Electro Static Discharge (ESD) that could permanently damage the device. Class I device.

Notes: 1. A θ_{ja} of 200°C/W should be used for derating and junction temperature calculations: $T_j = (P_d \times \theta_{ja}) + T_a$

2. Maximum soldering temperature is 260°C for 5 seconds.

Electrical Parameters, T_A = 25°C, V_{cc} = 5V, Single Ended Operation

Symbol	Parameter/Test Condition: Z_o = 50 Ohms	Units	Typ.
I_{cc}	Supply Current	mA	20
P_{sw}	Standby Power, V_{sw} = +2.5 Volts	mW	10
–	LO Operating Frequency Range	MHz	DC to 2,000
–	I/Q Modulating Frequency Range	MHz	DC to 700
–	I/Q Input Impedance	Ohms pF	25K 1.0

RF Electrical Parameters, T_A = 25°C, V_{cc} = 5V, Single Ended Operation

Symbol	Parameters/Test Conditions: LO = -13 dBm, F = 100 MHz, I/Q = 70 KHz 1 Volt P-P, Z_o = 50 Ohms		Units	Typ.
P_{1dB}	Power Out at 1 dB Compression		dBm	-9.5
P_{sat}	Saturated Output Power		dBm	-5.5
Noise	Output Noise Floor		dBm/Hz	-135
–	LO Input SWR		SWR	2.3:1
–	RF Output SWR		SWR	1.6:1
A_i	I/Q Amplitude Imbalance		dB	±0.5
P_i	I/Q Phase Imbalance		Deg.	±1.0
–	Modulation products power level in dB relative to the desired sideband at the output	Residual LO Undesired Sideband	dBc dBc	-37(3) -33(4)

Notes: 3. Improved LO rejection may be obtained by adjusting I/Q bias voltages.

4. Undesired sideband and harmonic suppression may be improved by adjusting I/Q amplitude and phase and/or using differential operation.

RF Electrical Parameters, T_A = 25°C, V_{cc} = 5V, Single Ended Operation

Symbol	Parameters/Test Conditions: LO = -13 dBm, F = 900 MHz, I/Q = 70 KHz 1 Volt P-P, Z_o = 50 Ohms	Units	Typ.
P_{1dB}	Power Out at 1 dB Compression	dBm	-9.5
P_{sat}	Saturated Output Power	dBm	-6.0
Noise	Output Noise Floor	dBm/Hz	-135
–	LO Input SWR	SWR	2.3:1
–	RF Output SWR	SWR	1.6:1
A_i	I/Q Amplitude Imbalance	dB	±1.0
P_i	I/Q Phase Imbalance	Deg.	±1.0
–	Modulation products power level in dB relative to the desired sideband at the output — Residual LO Undesired Sideband	dBc dBc	-35[3] -30[4]

Notes: 3. Improved LO rejection may be obtained by adjusting I/Q bias voltages.

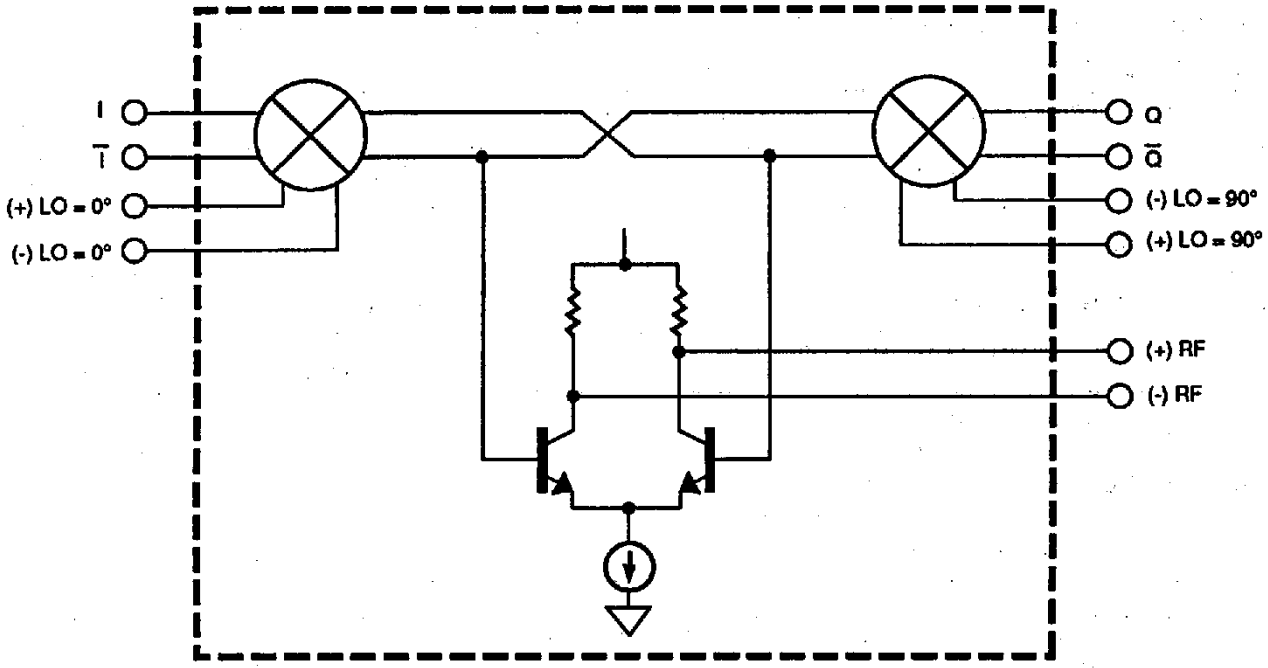
4. Undesired sideband and harmonic suppression may be improved by adjusting I/Q amplitude and phase and/or using differential operation.

Theory of Operation

Figure 1 shows the simplified schematic for the HPMX-2001. There are four differential input pairs (I, Q, LO = 0°, LO = 90°) and one differential output pair (RF). Any of the inputs or outputs can be used single-endedly with the proper terminations. The bias circuit for the LO inputs provides 50 Ohm matching of typically 2.3:1 in either differential or single-ended mode. The I and Q inputs are differentially mixed with the LO = 0° and LO = 90° signals respectively. The two mixer cells are double balanced to improve port isolation and reduce spurious signals at the RF output.

The outputs of the mixers are cross coupled into the summing amplifier circuit. This helps to reduce any internally generated offsets which tend to cause greater feedthrough of unwanted signals to the RF outputs.

The mixer and summing subcells utilize current sources that are controlled by the standby circuit. When the standby mode is activated, the control line turns off the current sources for all subcells. The resulting power dissipation is due only to the standby circuit.



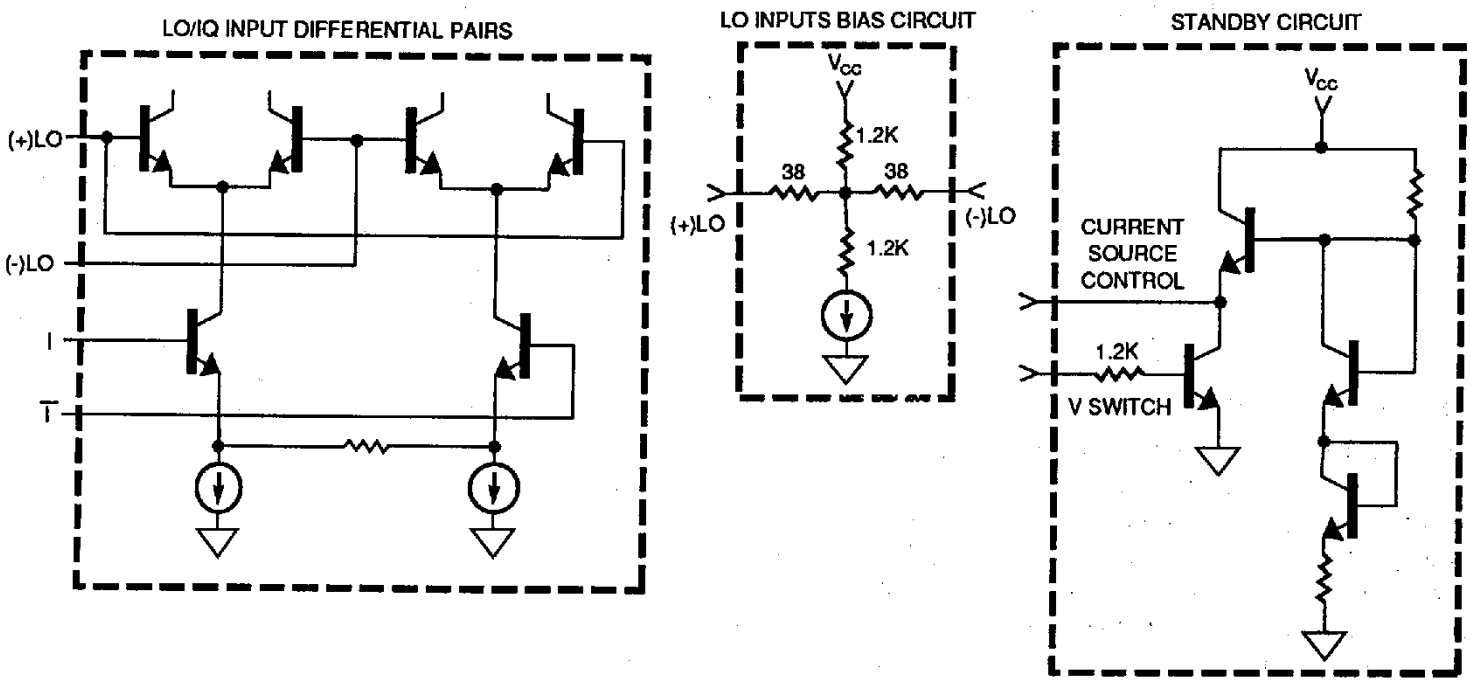
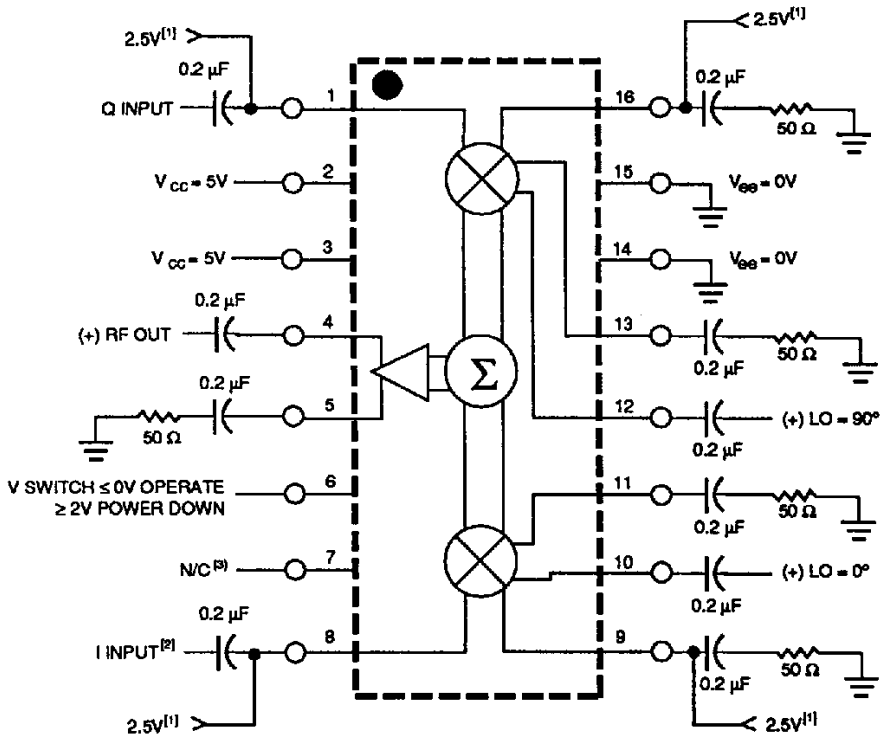


Figure 1. HPMX-2001 Simplified Schematic



NOTES:
1. IMPROVED LO REJECTION MAY BE OBTAINED BY ADJUSTING THE I/Q BIAS VOLTAGES.
2. UNDESIRED SIDEBAND AND HARMONIC SUPPRESSION MAY BE IMPROVED BY ADJUSTING I/Q AMPLITUDE AND PHASE AND/OR USING DIFFERENTIAL OPERATION.
3. DO NOT GROUND PIN 7.

Figure 2. HPMX-2001 Test Circuit, Single Ended Operation[2]

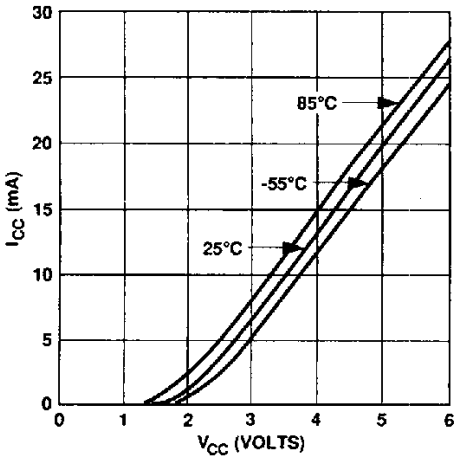


Figure 3. Typical I_{CC} vs. V_{CC} vs. Temperature

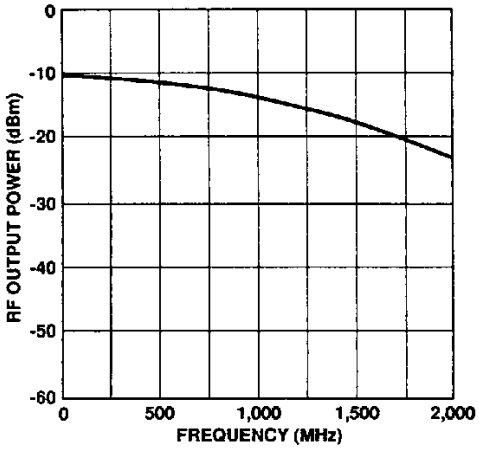


Figure 4. Typical RF-LO Frequency Response, LO = -13 dBm, I and Q = 70 KHz, 688 mV P-P

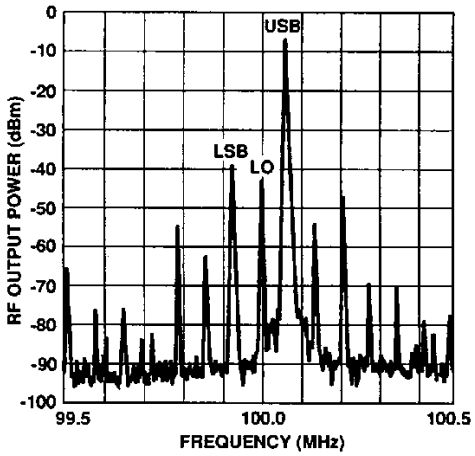


Figure 5. Typical Output Frequency spectrum, LO = 100 MHz -13 dBm, I/Q = 70 KHz 1 Volt P-P

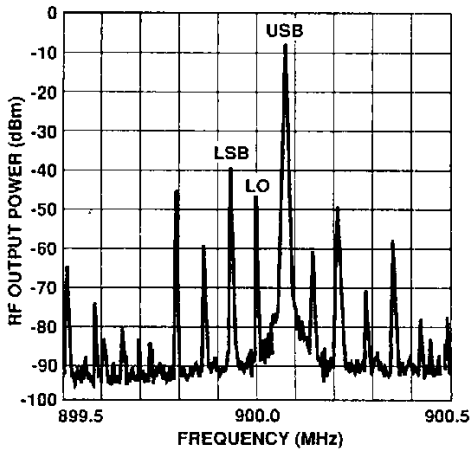


Figure 6. Typical Output Frequency spectrum, LO = 900 MHz -13 dBm, I/Q = 70 KHz 1 Volt P-P

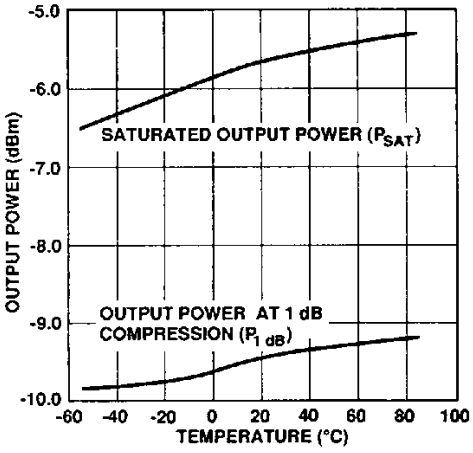


Figure 7. Output Power vs. Temperature, V_{CC} = 5 Volts, F = 100 MHz.

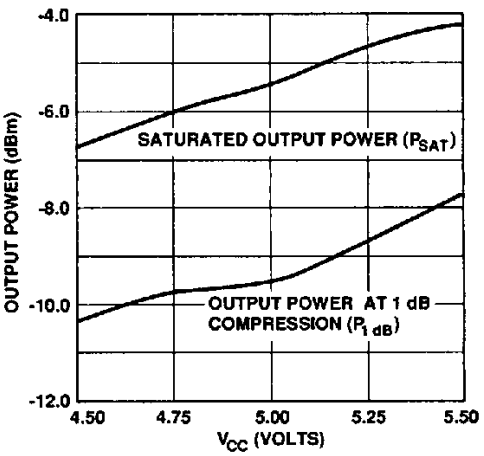
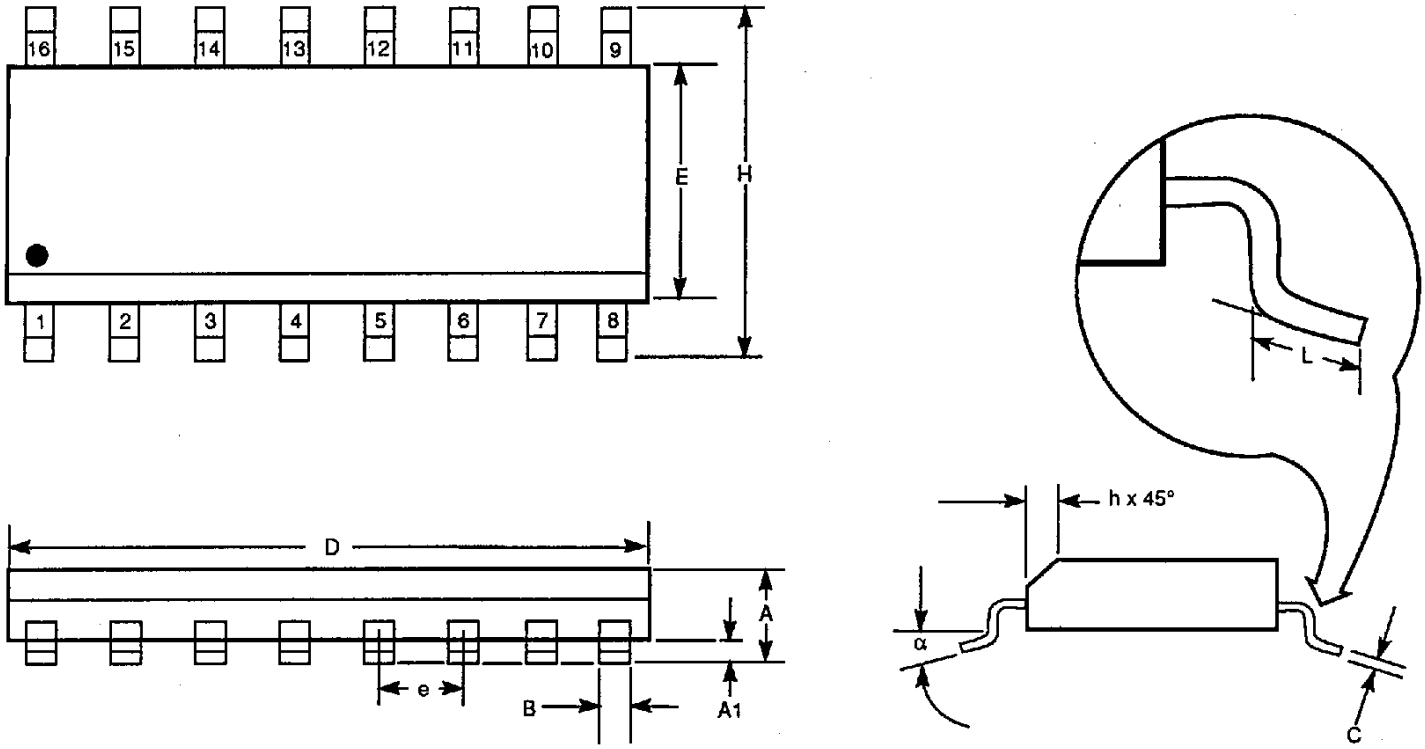


Figure 8. Output Power vs. V_{CC}, T_A = 25°C, F = 100 MHz.

Package Dimensions

Plastic SO-16 Package



Symbol	Dimensions	
	Min.	Max.
A	1.35 (0.053)	1.75 (0.068)
A1	0.10 (0.004)	0.25 (0.0098)
B	0.35 (0.0138)	0.49 (0.0192)
C	0.19 (0.007)	0.25 (0.0098)
D	9.80 (0.386)	10.00 (0.394)
E	3.80 (0.150)	4.00 (0.157)
e	1.27 BSC (0.050)	
H	5.80 (0.228)	6.20 (0.244)
h	0.25 (0.010)	0.50 (0.020)
L	0.40 (0.016)	1.27 (0.050)
α	0°	8°

Meets JEDEC outline dimensions.
Dimensions are in millimeters (inches)