1.5–2.5 GHz Upconverter/ Downconverter

Technical Data

HPMX-5001

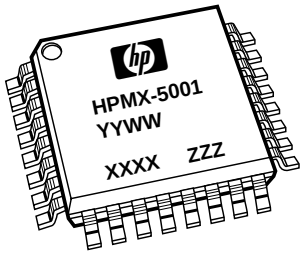
Features

- **2.7 V Single Supply Voltage**
- **Low Power Consumption (60 mA in Transmit Mode, 39 mA in Receive Mode Typical)**
- **2 dBm Typical Transmit Power at 1900 MHz**
- **Half-Frequency VCO with Frequency Doubler**
- **32/33 Dual-Modulus Prescaler**
- **Flexible Chip Biasing, Including Standby Mode**
- **TQFP-32 Surface Mount Package**
- **Operation to 2.5 GHz**
- **Use with Companion HPMX-5002 IF chip**

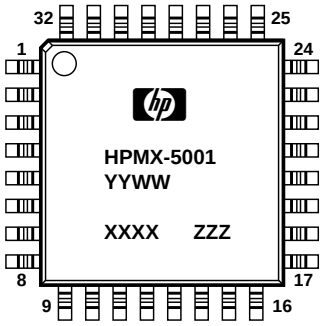
Applications

- **DECT, UPCS and ISM Band Handsets and Basestations**

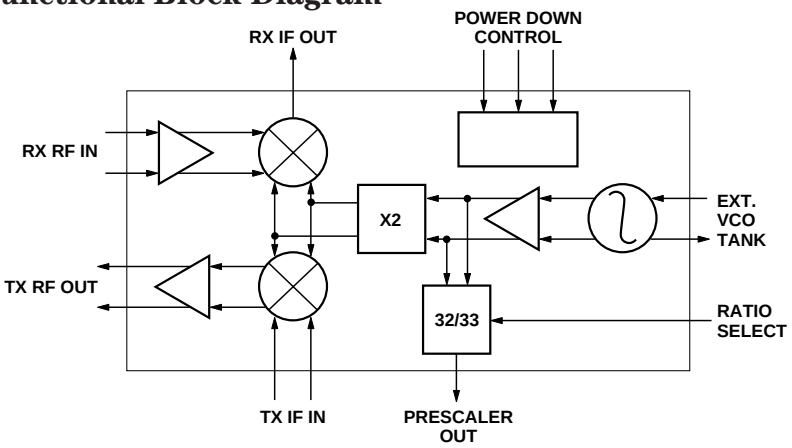
Plastic TQFP-32 Package



Pin Configuration



Functional Block Diagram



General Description

The HPMX-5001 Upconverter/ Downconverter provides RF system designers with all of the necessary features to perform an RF-to-IF downconversion for a receive path, as well as an IF-to-RF upconversion for transmit mode.

Designed to meet the unique needs of portable applications, the HPMX-5001 combines the qualities of flexible chip biasing, low power consumption, and true 2.7 V minimum supply voltage operation to provide superior performance and battery life. By incorporating the active elements of the VCO on-chip, as well as a 32/33 dual-modulus prescaler, overall system component count and costs are decreased. The 32-TQFP package insures that this high level of integration occupies a small amount of printed circuit board space.

The HPMX-5001 can be used in either dual-conversion systems (with the HPMX-5002 IF Demodulator/Modulator) or single-conversion systems. The HPMX-5001 is manufactured using Hewlett-Packard's HP-25 Silicon Bipolar Process with 25 GHz f_T and 30 GHz f_{Max}.

HPMX-5001 Absolute Maximum Ratings[1]

Parameter	Min.	Max.
V_{CC} Supply Voltage	-0.2 V	8 V
Voltage at Any Pin[4]	-0.2 V	V_{CC} + 0.2 V
Power Dissipation[2,3]		600 mW
RF Input Power		15 dBm
Junction Temperature		+150°C
Storage Temperature	-55°C	+125°C

Thermal Resistance[2]:
θ_{jc} = 100°C/W

Notes:
1. Operation of this device in excess of any of these parameters may cause permanent damage.
2. T_{CASE} = 25°C.
3. Derate at 10 mW/°C for T_{CASE} > 90°C.
4. Except CMOS logic inputs–see Summary Characterization Information table.

HPMX-5001 Guaranteed Electrical Specifications

Unless otherwise noted, all parameters are guaranteed under the following conditions: V_{CC} = 3.0 V. Test results are based upon use of networks shown in test board schematic diagram (see Figure 28). Typical values are for V_{CC} = 3.0 V, T_A = 25°C.

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
G_C	Receive Conversion Gain[1]	dB	12	14	
P_{out}	Transmitter Power Output Input[2] 2:1 output VSWR	dBm	0	2	
I_{CC}	Device Supply Current Transmit Mode	mA		64	80
	Receive Mode	mA		43	54
	Synth Mode	mA		15	19
	Standby Mode (with DIVMC Set High)	µA		1	50
V_{DIV}	DIV Single-Ended Swing[3]	V_{PP}	0.7	1	

Notes:
1. 50 Ω RF source, 100 MHz < I_F < 300 MHz, 1.89 GHz RF. There is a 750 Ω resistor on chip between RXIF and RXIFB (pins 3 and 4). A matching network from 750 Ω to 50 Ω is used for this measurement. Insertion loss of the matching network is included in the net conversion gain figure. See Figure 28.
2. Signal injected into P3 in Figure 28 is -12.5 dBm.
3. DIV output AC coupled into a 2 kΩ || 10 pF load. See test board schematic diagram, Figure 28.

HPMX-5001 Summary Characterization Information

Typical values measured on test board shown in Figure 28 at V_{CC} = 3.0 V, T_A = 25°C, RXIF = 110.592 MHz, TXRF = 1.89 GHz, unless otherwise noted.

Symbol	Parameters and Test Conditions	Units	Typical	
V_{IH}	CMOS Input High Voltage (Can Be Pulled up as High as V_{CC} + 7 V)[1]	V	≥ V_{CC} - 0.8	
V_{IL}	CMOS Input Low Voltage	V	≤ V_{CC} - 1.9	
I_{IH}	CMOS Input High Current	µA	<10	
I_{IL}	CMOS Input Low Current	µA	>-300	
t_s	DIVMC Setup Time[2,8]	ns	4	
t_h	DIVMC Hold Time[2,8]	ns	0	
t_{pd}	DIV Propagation Delay[2,8]	ns	<7	
	Mode Switching Time[3]	µs	<1	
Receive Mode			1.89 GHz	2.45 GHz
Gc	Receive Conversion Gain[9]	dB	14	13.5
NF	Noise Figure[4]	dB	10	10
I_{IP3}	Input Third Order Intercept Point	dBm	-8	-9
I_{P1dB}	Input 1 dB Gain Compression Point	dBm	-18	-18
	LO Leakage (2 x f_{VCO}) at IF Port	dBm	-57	—
$VSWR_{in}$	Input VSWR[5]		1.3:1	1.3:1
Transmit Mode[6]				
PIM_3	Power Output Level for >35 dB IM_3 Suppression[10]	dBm	—	-5
O_{P1dB}	Output 1 dB Gain Compression Point	dBm	0	0
$VSWR_{out}$	Output VSWR		1.8:1	1.8:1
	LO Suppression (2 x f_{VCO})	dBc	25	30
$F_{3dB}IF$	IF 3 dB Bandwidth	MHz	500	500
	Transmitter C/N @ 2 x f_{VCO} + 4 MHz[11]	dBc/Hz	+137	+134
Synth Mode				
	1LO Frequency Range[7]	MHz	750-1200	

Notes:

1. All CMOS logic inputs are internally pulled up to logic high level.
2. See Figure 2 for detailed timing diagram.
3. Between any two different biasing modes. This switching time does not include PLL lock-up time.
4. Single sideband noise figure.
5. In modes other than receive, the VSWR may be as high as 10:1.
6. Single-ended 50 Ω RF load, 300 Ω series IF terminations (600 Ω differential), 100 MHz < IF < 300 MHz, 1.89 GHz RF.
7. The LO is followed by a frequency doubler which raises the LO range to 1500-2400 MHz.
8. DIV output AC coupled into a 2 kΩ || 10 pF load. See test diagram, Figure 28.
9. 50 Ω RF source, 110 MHz < IF < 300 MHz, 1.89 GHz or 2.45 GHz RF. There is a 750 Ω resistor on chip between RXIF and RXIFB (pins 3 and 4). A matching network from 750 Ω to 50 Ω is used for this measurement. Insertion loss of the matching network is included in the net conversion gain figure.
10. PIM_3 is the maximum SSB output power for at least 35 dB IM_3 spur suppression.
11. Measured at saturated output power for 1.89 GHz. Measured at -5 dBm SSB output power for 2.45 GHz.

Table 1 - HPMX-5001 Pin Description

No.	Mnemonic	I/O Type	Description
1	TXCTRL	CMOS I/P	Controls biasing of transmit mixer, amplifiers, and doubler
3	RXIFB	Analog O/P	Inverted single-ended downconverted receiver output, normally tied to V_{CC} (internal 750 Ω resistor connects to RXIF)
4	RXIF	Analog O/P	Single-ended downconverted receiver output, drives SAW filter (internal 750 Ω resistor connects to RXIFB)
5	TXIF	Analog I/P	Transmit non-inverting IF input
6	TXIFB	Analog I/P	Transmit inverting IF input
7	LNAREF	Analog DC I/P	Reference input for receive input amplifier
8	RXRF	Analog I/P	Receive RF input
10	TXRXVCC	DC Supply	Supply voltage for transmit path, receive front-end and mixer
11,15	TXRXGND	Ground	Ground for transmit path, receive front-end and mixer
12	TXRFB	Analog O/P	Inverting output of transmit path (see test diagram for matching network)
14	TXRF	Analog O/P	Non-inverting output of transmit path (see test diagram for matching network)
16	DBLVCC	DC Supply	Supply voltage for LO frequency doubler
17	DBLGND	Ground	Ground for LO frequency doubler
20	VCOTNKS	Analog I/P	Sense line from external tank circuit to on-chip VCO amplifier
21	VCOTNKF	Analog O/P	Force line from on-chip VCO amplifier to external tank circuit
22	VCOVCC	DC Supply	Supply voltage for on-chip VCO amplifier
23	VCOGND	Ground	Ground for on-chip VCO amplifier
26	DIVVCC	DC Supply	Supply voltage for 32/33 dual-modulus prescaler
27	DIVGND	Ground	Ground for 32/33 dual-modulus prescaler
28	DIV	Analog O/P	Output from 32/33 dual-modulus prescaler
30	DIVMC	CMOS I/P	Modulus control signal for 32/33 dual-modulus prescaler
31	LOCTRL	CMOS I/P	Controls biasing for VCO and 32/33 dual modulus prescaler
32	RXCTRL	CMOS I/P	Controls biasing for receive mixer, amplifiers, and doubler
2,9,13, 18,19,24, 25,29	VSUB	Ground	Substrate bias voltage

Table 2 - HPMX-5001 Mode Control

(CMOS Logic Levels - all pins internally pulled up to high level)

Mode	TXCTRL	RXCTRL	LOCTRL
Transmit	0	1	0
Receive	1	0	0
Synth	1	1	0
Standby	1	1	1

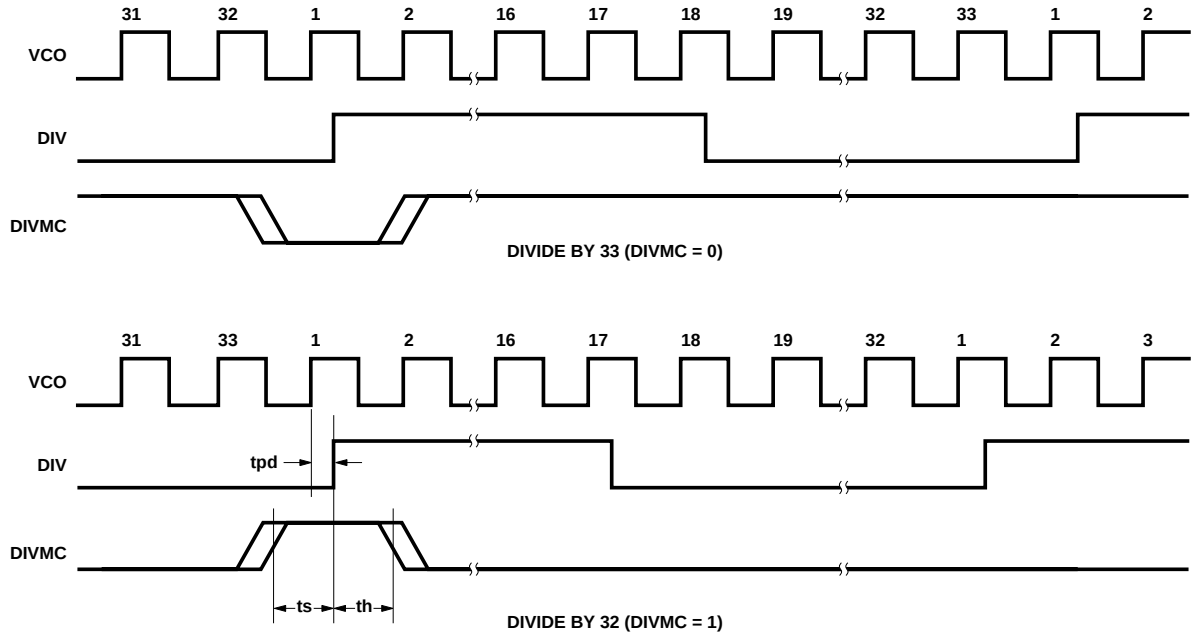


Figure 2. HPMX-5001 Prescaler Timing Diagram.

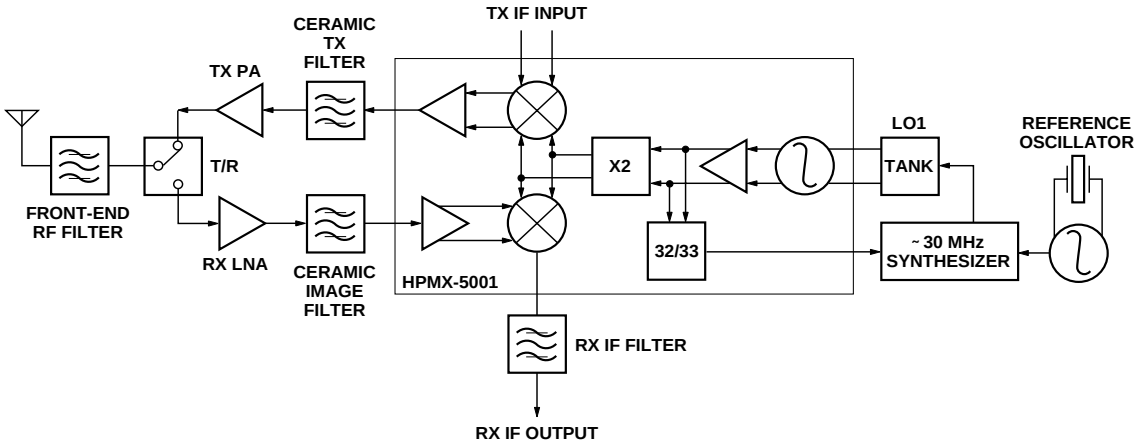


Figure 3. HPMX-5001 Block Diagram/Typical Application.

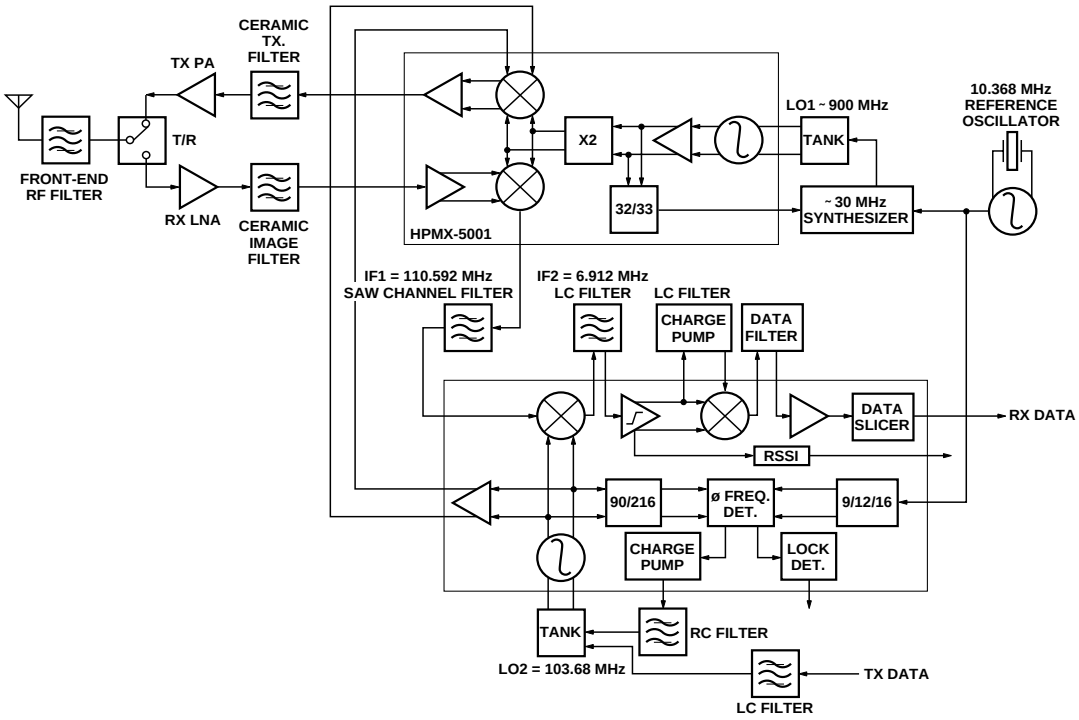


Figure 4. Typical HPMX-5001 Application with HPMX-5002 IF Chip. All Other Connections Go to Burst Mode Controller, Power Source, or Ground.

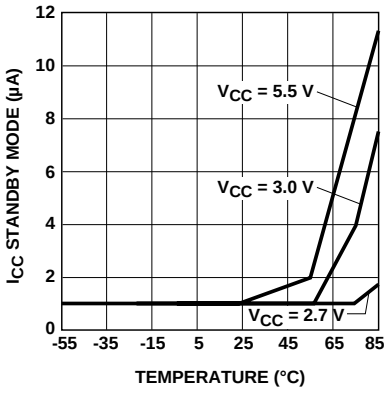


Figure 5. I_{CC} in Standby Mode vs. Temperature and V_{CC}.

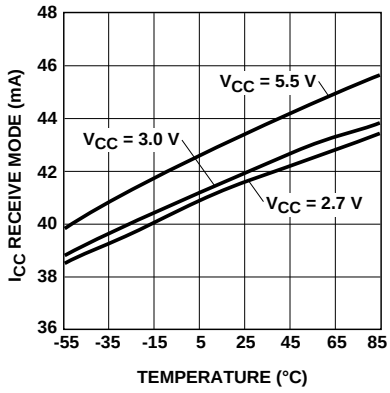


Figure 6. I_{CC} in Receive Mode vs. Temperature and V_{CC}.

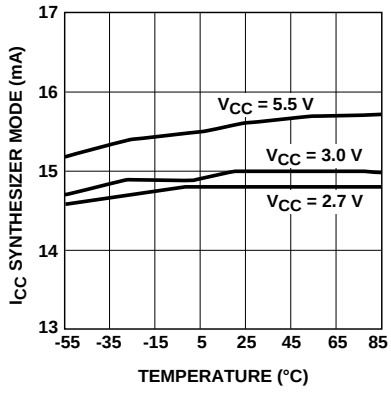


Figure 7. I_{CC} in Synthesizer Mode vs. Temperature and V_{CC}.

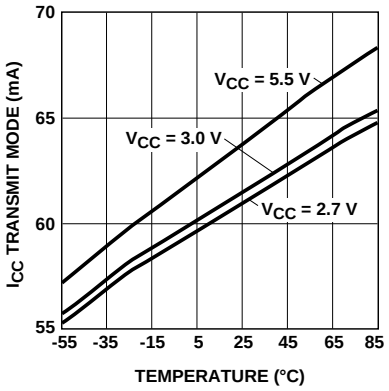


Figure 8. I_{CC} in Transmit Mode vs. Temperature and V_{CC}.

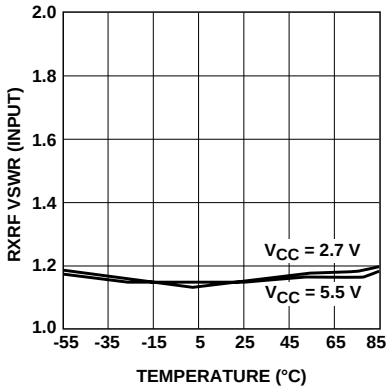


Figure 9. Receive Downconverter Input VSWR vs. Temperature and V_{CC}.

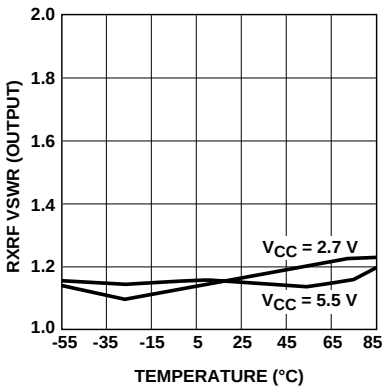


Figure 10. Receive Downconverter Output VSWR vs. Temperature and V_{CC}.

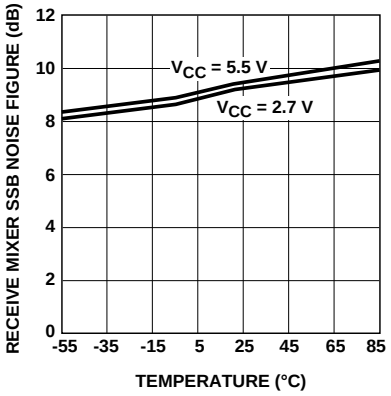


Figure 11. Receive Downconverter SSB Noise Figure vs. Temperature and V_{CC}.

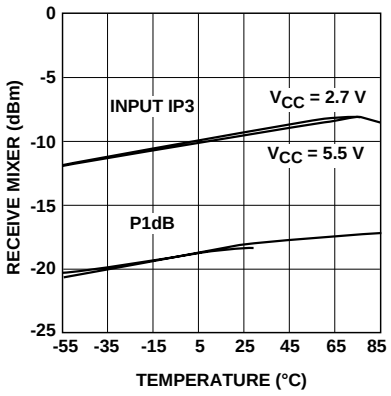


Figure 12. Receive Downconverter Input Third Order Intercept Point and Output 1 dB Compression Point vs. Temperature and V_{CC}.

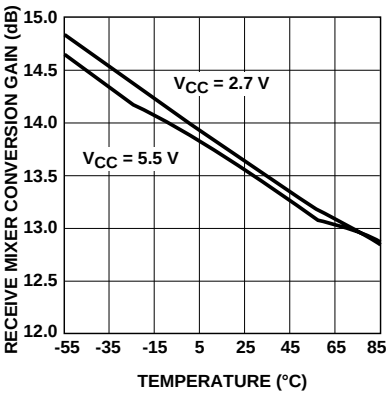


Figure 13. Receive Downconverter Conversion Gain vs. Temperature and V_{CC}.

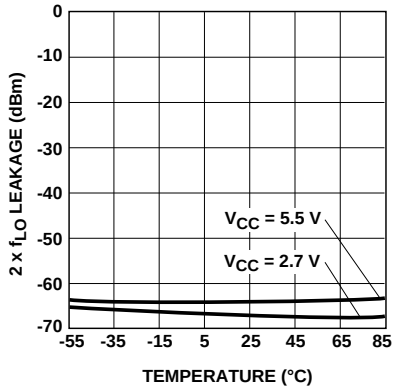


Figure 14. 2 x f_{LO} Leakage at Receive Downconverter Output vs. Temperature and V_{CC}.

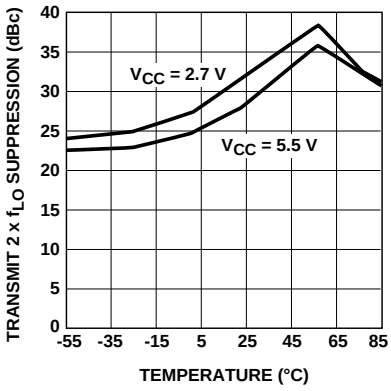


Figure 15. 2 x f_{LO} Suppression at Transmit Upconverter Output vs. Temperature and V_{CC}.

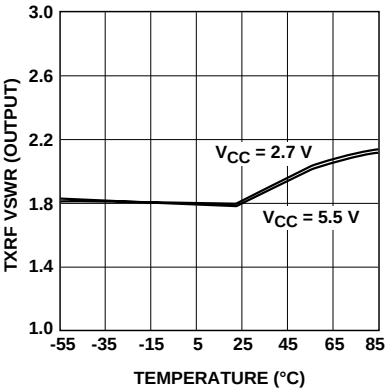


Figure 16. Transmit Upconverter Output VSWR vs. Temperature and V_{CC}.

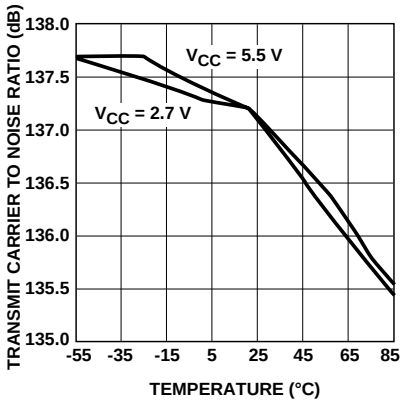


Figure 17. Carrier to Noise Ratio at Transmit Upconverter Output vs. Temperature and V_{CC}.

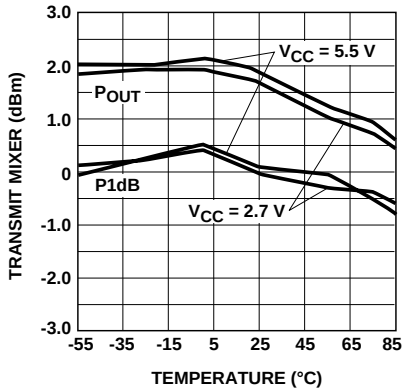


Figure 18. Transmit Upconverter Power Output and Output 1 dB Compression Point vs. Temperature and V_{CC}.

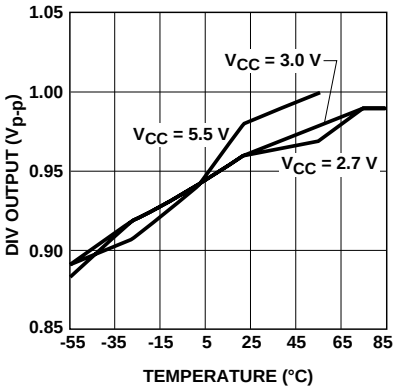


Figure 19. Prescaler Output Voltage vs. Temperature and V_{CC}.

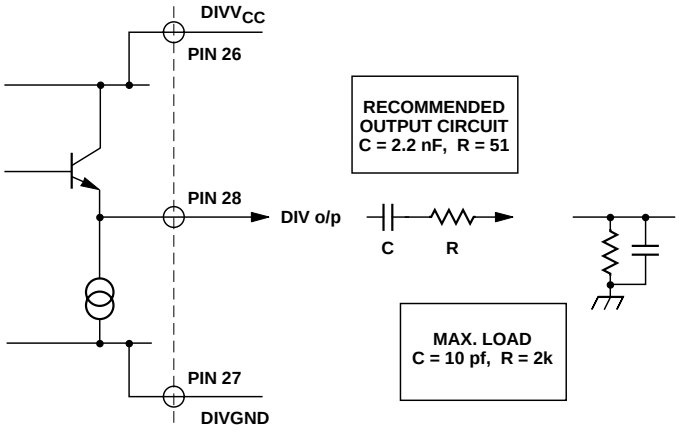


Figure 20. Equivalent Circuit and Recommended Output and Load Circuits for the HPMX-5001 Prescaler Output.

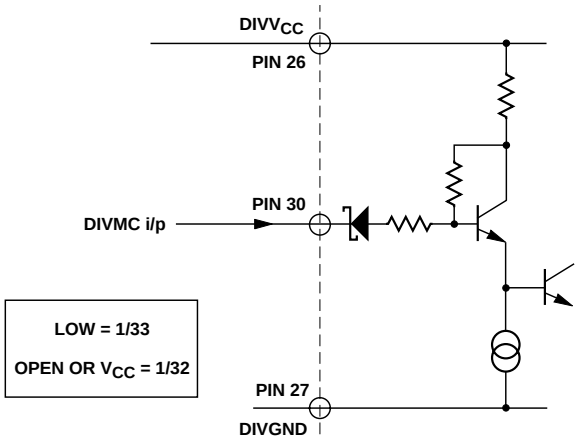


Figure 21. Equivalent Circuit for the Divider Modulus Control.

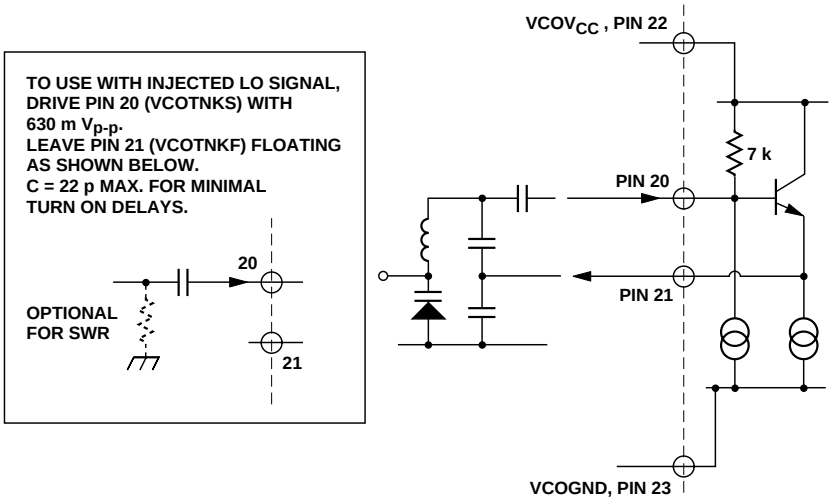


Figure 22. Equivalent Circuit for VCO Tank Connection and Recommended Tank Circuit.

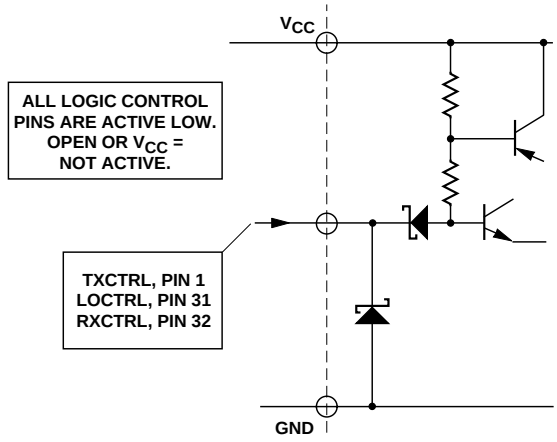


Figure 23. Equivalent Circuit for Logic Control Pin 1, 31, and 32.

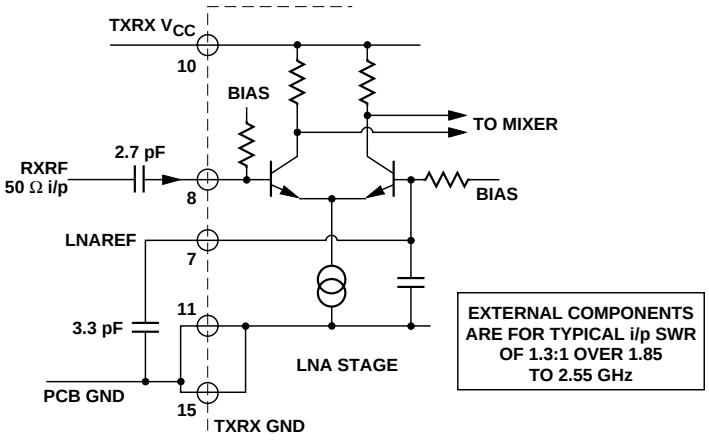


Figure 24. Equivalent Circuit for RXRF Input.

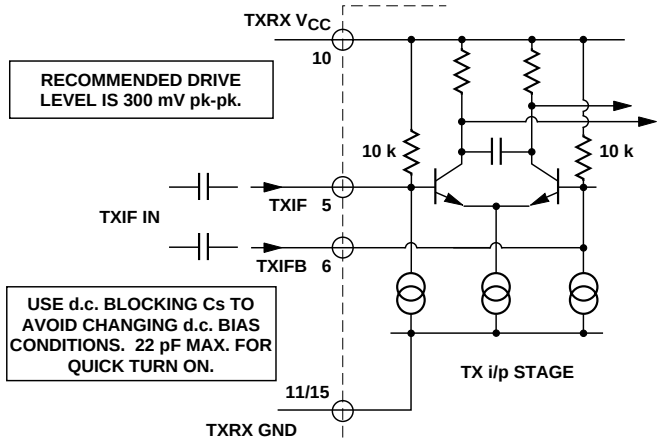


Figure 25. Equivalent Circuit for TXIF Input.

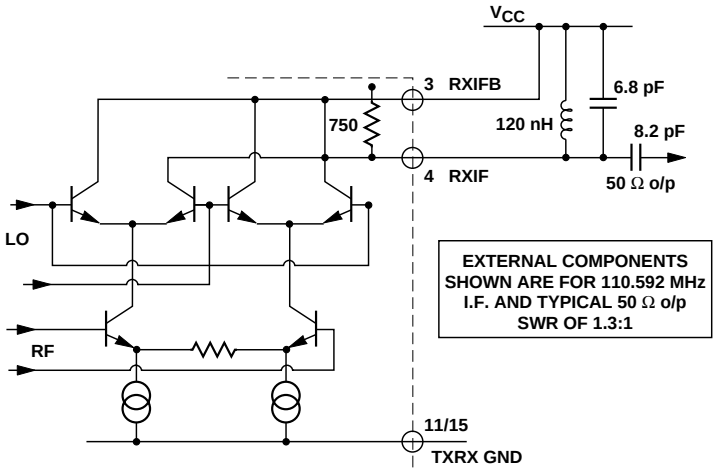


Figure 26. Equivalent Circuit for the RXIF Output and Recommended Matching Circuit for 110.592 MHz IF.

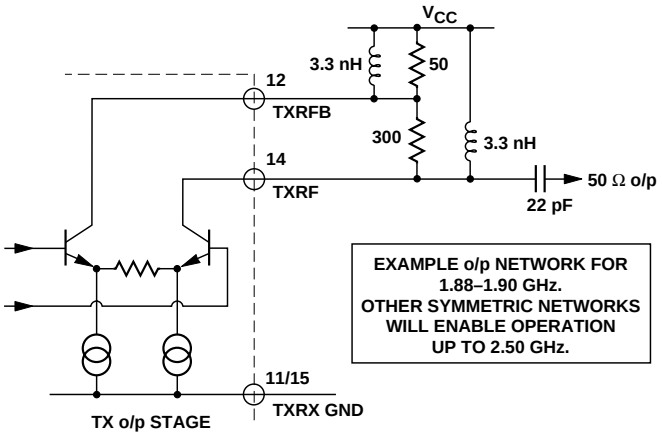


Figure 27. Equivalent Circuit for TXRF Output and Matching Network for DECT Phone Operation.

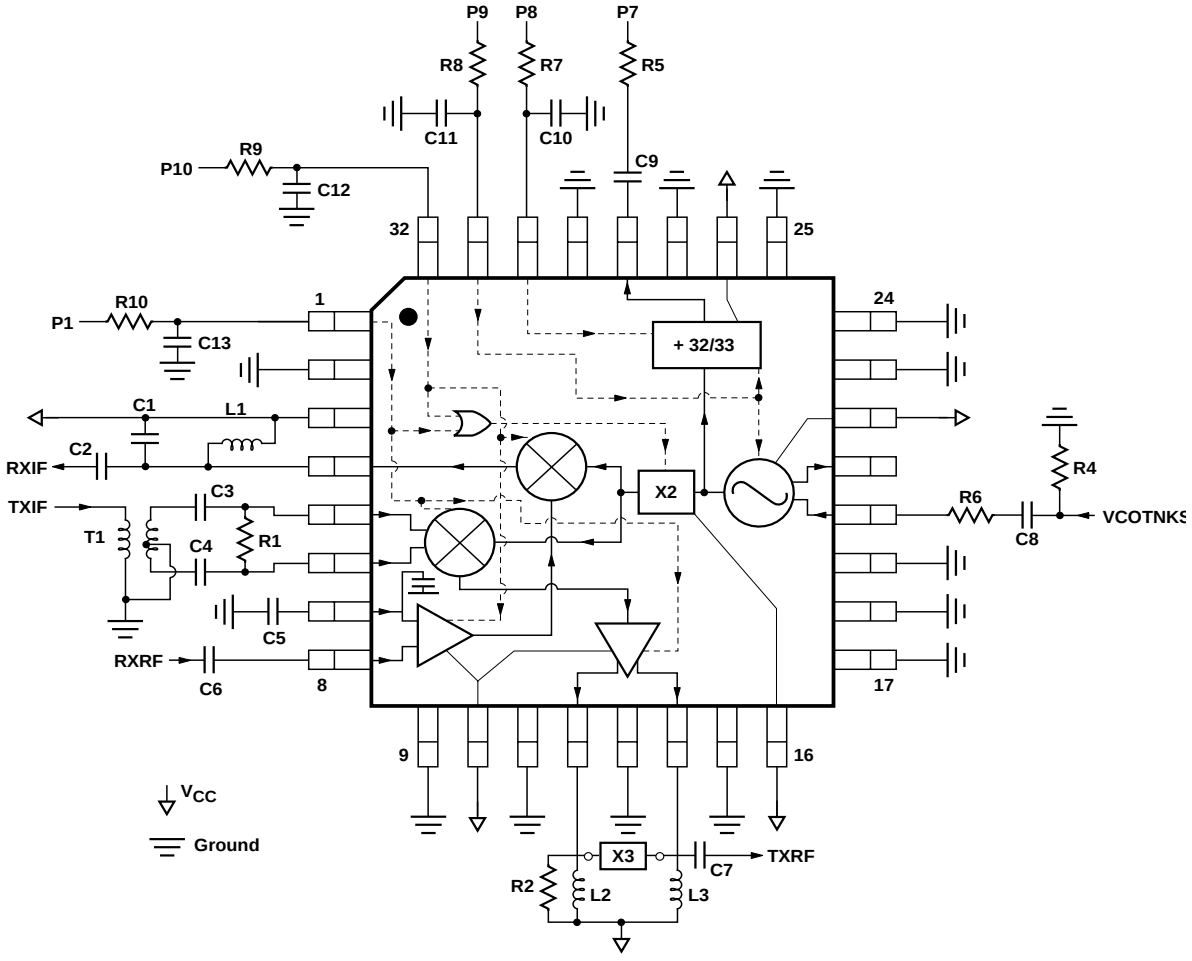


Figure 28. Test Board Schematic Diagram. All I/O Labels Correspond to Those on the Test board. See Table 3 for Component Values.

Table 3. Test Board Components Shown in Figure 28.
Note: Required V_{CC} decoupling capacitors are not shown on the schematic. Detailed schematic and board layout are available in Application Note 1081.

Component Label	Value (Size)
R1	270 (0805)
R2, R4, R5	51.1 (0805)
X3	R = 300 (0805) for 1.89 GHz, L = 3.3 nH for 2.45 GHz
R6	20 (0805)
R7, R8, R9, R10	1100 (0805)
C1	see Table 4
C2	see Table 4
C3, C4, C10, C11, C12, C13	1 nF (0805 or 0504)
C5	3.3 pF (0504 or 0603)
C6	2.7 pF (0805)
C7	22 pF (0805) for 1.89 GHz, 3.3 pF for 2.45 GHz
C8	12 pF (0805 or 0504)
C9	2.2 nF (0805)
L1	see Table 4
L2, L3	3.3 nH (0805)
T1	1:4 Balun T4-1-X65

Table 4. Component changes for dfferent IF frequencies.

IF Frequency	C1, pF	C2, pF	L1, nH	VSWR
110 MHz	6.8	8.2	120	1.3:1
200 MHz	1.0	3.9	100	1.3:1
250 MHz	1.2	3.9	56	1.3:1
300 MHz	1.2	3.9	39	1.3:1
350 MHz	2.7	2.7	27	1.3:1

Functional Description

A typical DECT application of the HPMX-5001 in a dual-conversion superheterodyne radio transceiver is shown in Figure 3. The HPMX-5001 is designed to provide four different modes of operation:

- Transmit, where the VCO, doubler, upconverting mixer, associated buffers, and prescaler are enabled
- Receive, where the VCO, doubler, downconverting mixer, associated buffers, and prescaler are enabled
- Synthesizer, where only the VCO and prescaler are active
- Standby, where all circuits are disabled

These four modes are controlled via a three wire interface, TXCTRL, RXCTRL, and LOCTRL. Figure 1 shows the programming logic states for all four modes. The detailed description of the three active modes is given below.

Transmit Mode

For transmit upconversion, a differential narrow-band modulated signal is AC-coupled into the TXIF and TXIFB inputs. The differential signal may be generated by the HPMX-5002 IF Demodulator/Modulator. Once on-chip, the signal is buffered and applied to a double-balanced Gilbert cell mixer. The upconverted RF signal is then amplified to generate a -0.6 dBm single-ended, single-sideband power signal at the 1 dB compression point. The RF outputs, TXRF and TXRFB, are open-collector outputs (see test diagram Figure 28 for recommended matching network). The TXRF output is AC-coupled into a 50 Ω transmit filter. This signal is then filtered and amplified off-chip by an external power amplifier before it is switched into the antenna. The HPMX-5001 may also be used in DECT systems which utilize direct modulation of the 1LO for data transmission. In this case, either the TXIF or TXIFB input, but not both, must be tied to V_{CC} to cause the upconverting mixer to act as a buffer stage.

Receive Mode

In receive mode, a preamplified RF signal is passed through an image filter and applied as a single-ended signal to the 50 Ω RXRF input. Use of a 2.7 pF blocking capacitor is recommended. RXRF is the non-inverting input of the RF input amplifier. The inverting input of this amplifier, LNAREF, is self-biased and requires only an external capacitor (recommended value of 3.3 pF) to ground. The receive downconversion mixer also employs a double-balanced Gilbert cell configuration. The production version of the HPMX-5001 will have two equivalent open collector outputs. The HPMX-5001 can operate at IF frequencies up to 300 MHz (see Figure 28 for recommended matching network).

Synthesizer Mode

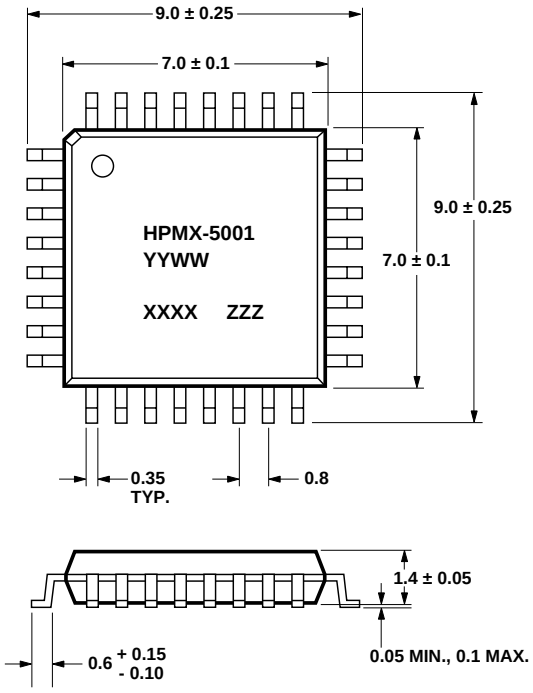
The on-chip 32/33 dual-modulus prescaler, in conjunction with the VCO, external tank circuit, and CMOS synthesizer, form a phase-locked loop (PLL). The prescaler divider output and modulus control input are designed to be compatible with positive-edge triggered CMOS synthesizers from a variety of vendors. The timing requirements for the prescaler are shown in Figure 2. It is important to note that the prescaler divides the VCO signal, and not the frequency doubler output. Local oscillator (LO) signal generation on the HPMX-5001 is accomplished through the combination of a VCO and frequency doubler. The VCO is a simple Clapp oscillator for the best possible noise performance. The VCO force and sense pins (VCOTNKF, VCOTNKS) are self-biased, so that the connections to the tank (minimum Q of 20) are through AC-coupling capacitors. VCOTNKS can also be used with an injected LO. VCOTNKF would then be left floating. The doubler circuit multiplies the VCO frequency by two. This enables the VCO to have lower sensitivity to both package parasitics and LO re-radiation. Separate bias pins and buffering are utilized to minimize pulling of the VCO when the chip is switched from synthesizer to transmit or receive mode.

Part Number Ordering Information

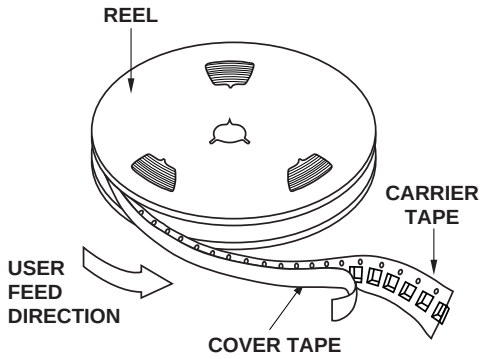
Part Number	No. of Devices	Container
HPMX-5001-STR	10	Strip
HPMX-5001-TR1	1000	Tape and Reel
HPMX-5001-TY1	250	Tray

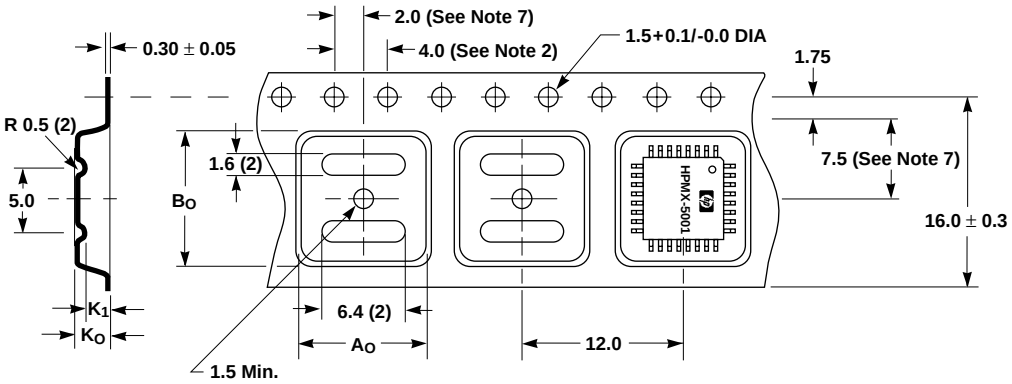
Package Dimensions 32 Pin Thin Quad Flat Package

All dimensions shown in mm.



Tape Dimensions and Product Orientation for Outline TQFP-32





Cover tape width = 13.3 ± 0.1 mm
Cover tape thickness = 0.051 mm (0.002 inch)

A_O = 9.3 mm
B_O = 9.3 mm
K_O = 2.2 mm
K_1 = 1.6 mm

NOTES:
1. Dimensions are in millimeters
2. 10 sprocket hole pitch cumulative tolerance ±0.2
3. Chamber not to exceed 1 mm in 100 mm
4. Material: black conductive Advantek™ polystyrene
5. A_O and B_O measured on a plane 0.3 mm above the bottom of the pocket.
6. K_O measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.