IF Modulator/Demodulator IC

Technical Data

HPMX-5002

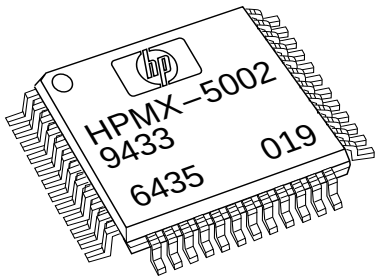
Features

- **Use with HPMX-5001 Up/Down Converter Chip for DECT Telephone Applications**
- **2.7–5.5 V Single Supply Voltage**
- **>75 dB RSSI Range**
- **Internal Data Slicer**
- **On-chip LO Generation, Including VCO, Prescalers and Phase/Frequency Detector**
- **Flexible Chip Biasing, Including Standby Mode**
- **Supports Reference Crystal Frequencies of 9, 12, and 16 Times the DECT Bit Rate (1.152 MHz)**
- **IF Input Frequency Range up to 250 MHz**
- **TQFP-48 Surface Mount Package**

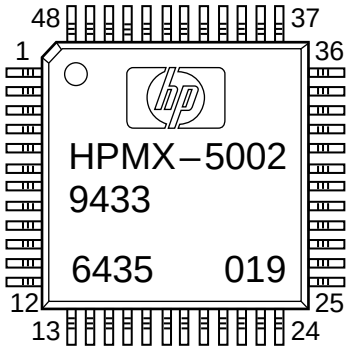
Applications

- **DECT, Unlicensed PCS and ISM Band Handsets, Basestations and Wireless LANs**

Plastic TQFP-48 Package



Pin Configuration



Description

The Hewlett-Packard HPMX-5002 IF Modulator/Demodulator provides all of the active components necessary for the demodulation of a downconverted DECT signal. Designed specifically for DECT, the HPMX-5002 contains a down-conversion mixer (to a 2nd IF), limiting amplifier chain, discriminator/data slicer, lock detector, and RSSI circuits. The LO2 generation is also included on-chip, via a VCO, dividers, and phase/frequency detector. The divide ratios are programmable to support reference frequencies of either 9, 12, or 16 times the DECT bit rate of 1.152 MHz allowing the use of common, low cost crystals.

The LO2 VCO can also be utilized in transmit mode by directly modulating the external VCO tank. An AGC loop in the buffered VCO output suppresses harmonics and reduces signal level variability.

The HPMX-5002 is designed to meet the size and power demands of portable applications. Battery cell count and cost are reduced due to the 2.7 V minimum supply voltage. The TQFP-48 package, combined with the high level of integration, means smaller footprints and fewer components. Flexible chip biasing takes full advantage of the power savings inherent in time-duplexed systems such as DECT.

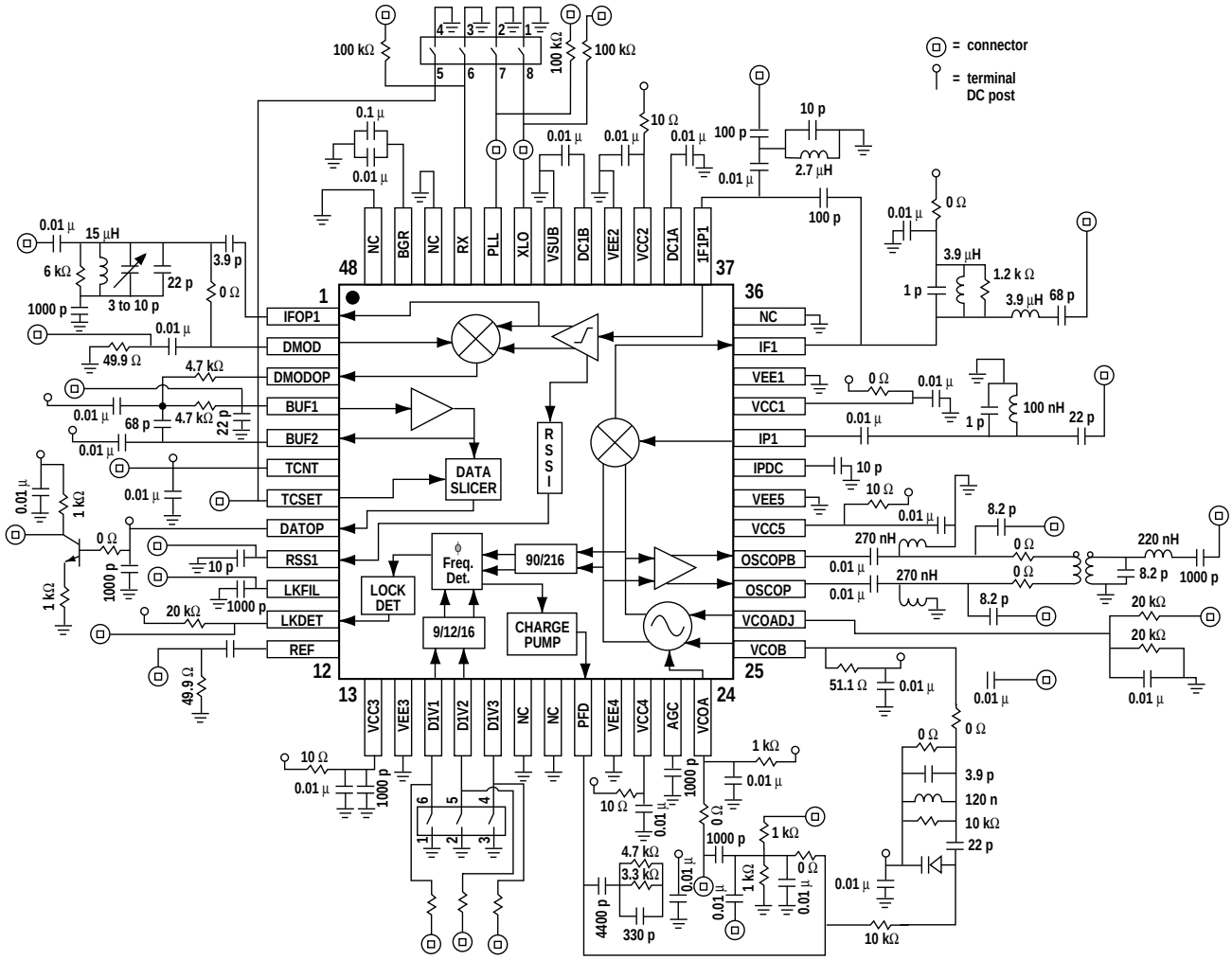
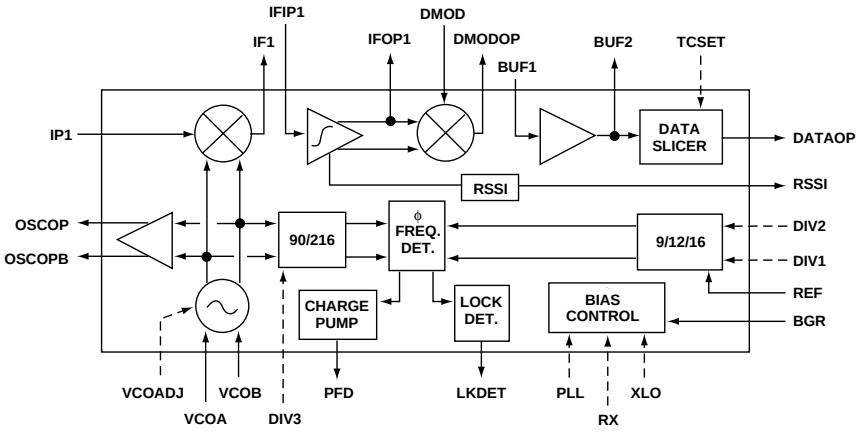


Figure 1. HPMX-5002 Test Board Schematic Diagram.

HPMX-5002 Functional Block Diagram



HPMX-5002 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Min.	Max.
	V_{CC} Supply Voltage	V	-0.2	7.5
	Voltage at any Pin[4]	V	-0.2	V_{CC} + 0.2
P_{diss}	Power Dissipation[2,3]	mW		200
	Junction Temperature	°C		+110
T_{STG}	Storage Temperature	°C	-55	+125

Thermal Resistance[2]:
θ_{jc} = 80°C/W

Notes:
1. Operation of this device in excess of any of these parameters may cause permanent damage.
2. T_{case} = 25°C
3. Derate at 10 mW/°C for T_{case} > 90°C
4. Except CMOS logic inputs, see Summary Characterization Information Table.

HPMX-5002 Guaranteed Electrical Specifications

Unless otherwise noted, all parameters are guaranteed under the following conditions: 2.7 V < V_{CC} < 5.5 V. Test results are based upon use of networks shown in test diagram (see Figure 1). f_{in} = 110.592 MHz. Typical values are for V_{CCX} = 3.0 V, T_A = 25°C.

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
I_{ccx}	Total V_{ccx} supply current (PLL locked)	RX mode	mA		21	27
	(PLL locked)	PLL mode	mA		16	20
		TX "flywheel" mode	mA		9	11.5
		Standby mode	µA			100
	Charge pump current	high current mode	µA	400	550	1000
	Charge pump current	low current mode	µA	30	50	100
GIF1	Mixer power gain from IP1 to IF1, external load impedance of 600 Ω	input matched to 50 Ω	dB	5	8	
VDATOP	Data slicer output level	Logic '0'	V			0.3
VDATOP	Data slicer output level	Logic '1'	V	V_{ccx}-0.3		

HPMX-5002 Summary Characterization Information

Typical values measured on test board shown in Figure 1 at V_{ccx} = 3.0 V, T_A = 25°C, V_{ref} = 300 mV_{pp} (or P_{in} =0 dBm), f_{in} = 110.592 MHz, f_{LO2} = 103.68 MHz, unless otherwise noted.

Symbol	Parameters and Test Conditions		Units	Typ.
V_{IH}	CMOS input high voltage (can be pulled up as high as V_{cc}+7V), Note 1		V	≥ V_{cc} - 0.8
V_{IL}	CMOS input low voltage	Note 1	V	≤ V_{cc} - 2.4
I_{IH}	CMOS input high current		µA	< 50
I_{IL}	CMOS input low current		µA	> - 50
	Mode switching time		µS	< 1
$P_{1\ dB}$	Mixer input 1 dB compression point	matched to 50 Ω source	dBm	-23
I_{IP3}	Mixer input IP3	matched to 50 Ω source	dBm	-17
NF_{IF1}	Mixer SSB noise figure (see test diagram Fig. 1)	input matched to 50 Ω source, 600 Ω load at output	dB	12
Z_{inIP1}	Mixer input impedance	50 MHz < f_{in} < 250 MHz	Ω	100
	RSSI dynamic range (for signal input at IFIP1; RSSI output measured with 6 bit ADC)	Note 2	dB	75
	RSSI voltage change	Note 2	mV/dB	17
	RSSI output voltage. V_{ccx} = 3 V, V_{RSSI} is monotonic	2 IF limiter input level: - 90 dBm -50 dBm -20 dBm	V	 0.88 1.48 2.04
$Z_{outRSSI}$	RSSI output impedance		kΩ	30
$IF2f_{3\ dB}$	IF2 limiter bandwidth		MHz	45
A_{VIF2}	IF2 limiter voltage gain	Prior to limiting, Note 3	dB	57
$Z_{inIFIP1}$	IF2 limiter input impedance at pin IFIP1	Note 3	Ω	600
V_{outLO2}	LO2 output buffer differential amplitude (between OSCOP and OSCOPB)	>1.5 kΩ differential load, f_{vco} = 103.68 MHz, V_{CC} = 3 V	mVp-p	335
	Bit slicer time constant ratio (Figure 7)	TCSET = 0 vs. TCSET = 1		80:1
	LO2 VCO output buffer noise floor (@ 4 MHz offset)	tank circuit Q = 35	dBc/Hz	-142
	PLL charge pump leakage current		pA	<100
ILKDET	Lock detector current sink	Logic '0' (unlocked)	mA	1.1

Notes:

1: All logic inputs must be set to either logic high or logic low.

2: RSSI signal is monotonic over stated dynamic range, but not necessarily linear. Voltage change is defined in the linear region of the transfer curve.

3: IF2 frequency in the range 1 MHz < f < 45 MHz, with 10 nF capacitors from DC1A and DC1B to ground.

HPMX-5002 Pin Description

No.	Mnemonic	I/O Type	Description
1	IFOP1	Analog O/P	Output of IF amplifier, feeds quadrature network for discriminator
2	DMOD	Analog I/P	Input to discriminator mixer, driven by output of quadrature network
3	DMODOP	Analog O/P	Output of discriminator mixer, drives external low-pass data filter
4	BUF1	Analog I/P	Noninverting input of buffer amplifier that drives the data slicer
5	BUF2	Analog O/P	Output of buffer amplifer that drives the data slicer
6	TCNT	Analog DC	External capacitor connection which sets time constant for data slicer
7	TCSET	CMOS I/P	Data slicer time constant select
8	DATOP	CMOS O/P	Output bit stream from data slicer
9	RSSI	Analog O/P	Receive Signal Strength Indicator output
10	LKFIL	Analog DC	External capacitor connection which sets time constant for lock detector
11	LKDET	CMOS O/P	Indicates that LO2 PLL is in lock status
12	REF	Analog I/P	Reference signal for LO2 PLL
13	VCC3	DC Supply	PLL supply voltage
14	VEE3	Ground	PLL ground
15	DIV1	CMOS I/P	Controls divide ratio for reference frequency input to the LO2 PLL
16	DIV2	CMOS I/P	Controls divide ratio for reference frequency input to the LO2 PLL
17	DIV3	CMOS I/P	Controls divide ratio for VCO frequency input to the LO2 PLL
20	PFD	Analog O/P	LO2 PLL phase/frequency detector charge pump output
21	VEE4	Ground	LO2 VCO ground
22	VCC4	DC Supply	LO2 VCO supply voltage
23	AGC	Analog DC	External capacitor connection to compensate LO2 VCO AGC loop
24	VCOA	Analog I/P	VCO tank force line
25	VCOB	Analog O/P	VCO tank sense line
26	VCOADJ	Analog I/P	Controls amplitude of buffered LO2 VCO output
27	OSCOP	Analog O/P	Buffered LO2 output (+)
28	OSCOPB	Analog O/P	Buffered LO2 output (-)
29	VCC5	DC Supply	1st IF supply voltage
30	VEE5	Ground	1st IF ground
31	IPDC	Analog DC	External capacitor connection for decoupling 1st IF bias point
32	IP1	Analog I/P	1st IF input signal
33	VCC1	DC Supply	IF limiting amplifier supply voltage
34	VEE1	Ground	IF limiting amplifier ground
35	IF1	Analog O/P	Downconverted signal from front-end mixer, drives external filter (hi-Z output, open collector)
37	IFIP1	Analog I/P	Input to IF limiting amplifier, driven by external filter (600 Ω impedance, internally set)
38	DC1A	Analog DC	External capacitor connection for decoupling IF limiting amplifier
39	VCC2	DC Supply	IF limiting amplifier supply voltage
40	VEE2	Ground	IF limiting amplifier ground

HPMX-5002 Pin Description, continued

No.	Mnemonic	I/O Type	Description
41	DC1B	Analog DC	External capacitor connection for decoupling IF limiting amplifier
42	VSUB	Ground	Substrate connection
43	XLO	CMOS I/P	Controls bias to VCO and PLL components in conjunction with PLL pin
44	PLL	CMOS I/P	Controls bias to VCO and PLL components in conjunction with XLO pin
45	RX	CMOS I/P	Controls bias to receive signal path, RSSI, data slicer
47	BGR	Analog DC	External capacitor connection for decoupling bandgap reference voltage
18,19, 36, 46, 48	N/C	Not connected	All unconnected pins should be connected to a low-noise ground

Table 1: HPMX-5002 Mode Control
(CMOS Logic Levels)

Logic State	Mode	PLL	XLO	RX	Sections ON (Note a)	Current @ 3.0 V	
0	—	0	0	0	RxP/VCO/—	14 mA	
1	TX	0	0	1	—/VCO/—	8.2 mA	
2	—	0	0	0	RxP/—/—	8.25 mA	
3	—	0	1	1	—/—/—	2.48 mA	Note b
4	RX	1	0	0	RxP/VCO/DIV	19.2 mA	
5	PLL	1	0	1	—/VCO/DIV	13.4 mA	
6	—	1	1	0	RxP/—/—	8.26 mA	
7	STBY	1	1	1	—/—/—	7.0 µA	

Table 2: HPMX-5002 PLL Divider Programming
(CMOS Logic Levels)

REF divide by:	DIV1	DIV2	DIV3
9	1	0	X
12	0	0	X
16	0	1	X
Not defined	1	1	X
LO2 divide by:			
90	X	X	0
216	X	X	1

Note a:
RxP = Receive Path (Mixer, Limiter, Discriminator, RSSI, Opamp, Data Slicer). VCO = VCO, AGC.
DIV = Dividers and Phase Frequency Detector. Text explanation is in Modes of Operation.

Note b:
Mode 3 is NOT a Standby Mode. Bandgap reference + 1st down convert mixer are still on (input amplifier of first down convert mixer is off).

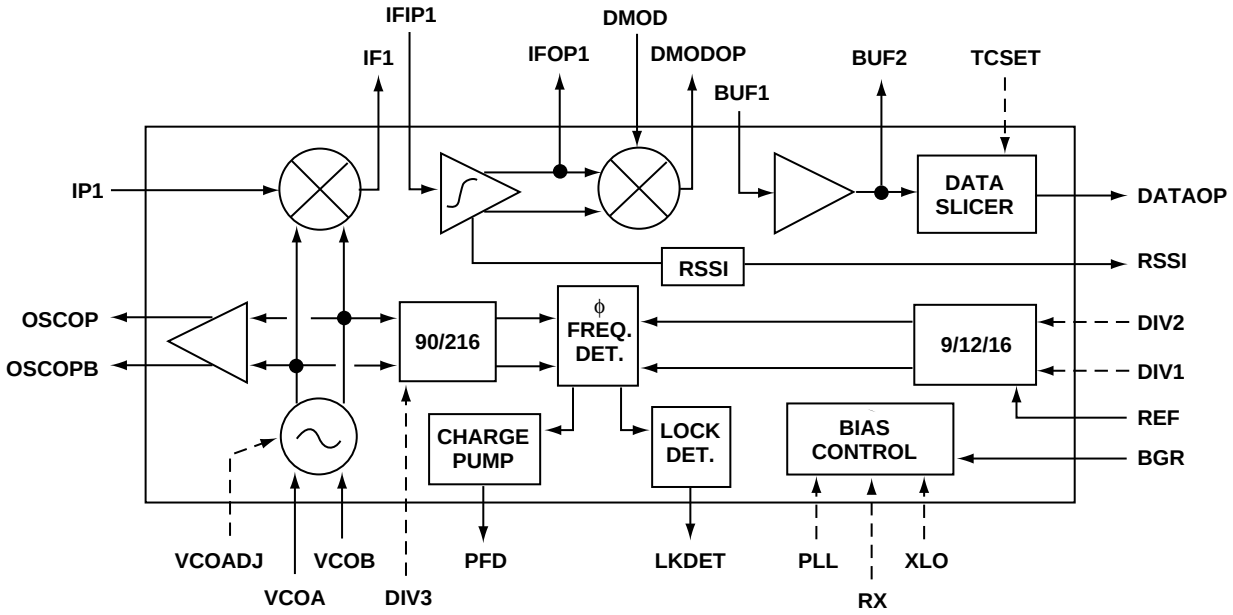


Figure 2. HPMX-5002 Detailed Block Diagram.

Functional Description

Please refer to Figure 2, Detailed Block Diagram, above. Figure 2 contains a graphical representation of all 32 active signal pins of the HPMX-5002. For clarity, the supply, ground, and substrate pins are deleted.

Modes of Operation

The HPMX-5002 supports four basic modes of operation. The logic states necessary to program each mode are listed in Table 1, Mode Programming. The modes are:

Receive mode (RX), which is used during the receive time slot in DECT systems. All blocks are powered on in this mode.

LO2 synthesis mode (PLL), which enables the IC to achieve phase lock without biasing the receive signal path, thus saving power. This is very useful for DECT blind-slot applications.

Transmit mode (TX), designed for use when the LO2 VCO is directly modulated by the DECT data stream for subsequent up-conversion to the channel frequency (with the HPMX-5001 DECT Upconverter/Down-converter). In this mode, only the VCO and LO2 output buffer are biased and operational. In order to use the LO2 VCO as a modulation source, it is necessary to first program the HPMX-5002 in PLL mode. Once the loop has achieved lock, the PLL is then disabled by setting the PLL pin to a logic 0. This puts the VCO into "**flywheel**" operation, preventing the PLL from interfering with the modulation of the VCO. Leakage in the tank circuit shown in Figure 3 allows the VCO to drift at a rate of 2.5 kHz per mS, well within the DECT specs of 13 kHz per mS.

Standby mode, where all blocks are powered down. This mode allows the system designer to effectively turn the IC off without having to use battery control, and also allows the IC to change quickly to an active mode.

A short text description of Table 1 is summarized below:

PLL low:	Forces DIV off
PLL high:	DIV is on only if XLO is 0
XLO low:	Forces VCO on
XLO high:	Forces VCO off, DIV off
RX low:	Forces RX on
RX high:	Forces RX off

Detailed Circuit Description

PLL Section

The PLL section of the HPMX-5002 contains three major sections: a set of reference and LO2 dividers, a phase/frequency detector with charge pump, and a lock detector.

The dividers for both the reference and LO2 signals in the PLL section are programmable to accomodate the most popular DECT reference frequencies and also to enable the use of higher 1st IF frequencies if desired. Figure 3 illustrates the logic states necessary to program both the reference and LO2 dividers.

The reference divider ratios were selected to conform to the three most popular DECT reference frequencies of 10.368 MHz, 13.824 MHz, and 18.432 MHz. The LO2 divider values allow the use of either a 110.592 MHz or 112.32 MHz 1st IF with a divide value of 90 (which yields a LO2 of 103.68 MHz). In addition, the divide by 216 value permits the use of a much higher 1st IF (222.91 MHz, with a corresponding LO2 of 248.832 MHz), which enables the use of much smaller SAW filters and relaxes the image filtering requirements.

The phase/frequency detector also incorporates a lock detection feature. The user must supply a decoupling capacitor (recommended value of 1 nF) from the LKFIL pin to ground. If the loop is not in phase lock, the LKDET pin will sink up to 1 mA. This open collector output is utilized so that this signal can be wire-ORed with other lock detection circuits, such as from the 1LO portion of the system. The pullup resistor can also be tied to the CMOS positive supply, thus eliminating potential problems with CMOS logic high voltages when different positive supplies are used between the radio and the baseband processor. When the PLL loop phase error is less than approximately 0.3 radians, the LKDET current sink goes to zero.

VCO Section

The VCO section has two major components, a sustaining amplifier and a buffered external output. The sustaining amplifer is designed to be used with an external tank circuit, and incorporates a force (VCOA) and sense (VCOB) architecture to reduce the effects of package parasitics. As described earlier, the VCOB pin may be overdriven by an external LO, in which case the on-chip sustaining amplifier acts as a buffer stage before the downconverting mixer.

The buffered external output is a differential signal (OSCOP, OSCOPB). The buffer also incorporates an AGC loop in order to provide a sinusoidal output signal with constant amplitude which is insensitive to variations in tank Q and loading. This helps to suppress harmonics and eliminates therefore the need for an upconversion filter if the HPMX-5002 is used in a system together with the 2.5 GHz upconverter/downconverter HPMX-5001. The AGC requires an external compensation capacitor (recommended value 1 nF) from the AGC pin to ground.

Signal Path

The input to the HPMX-5002 is an AC-coupled IF signal (IP1). The input buffer before the downconverting mixer requires a decoupling capacitor from the IPDC pin to ground (recommended value 10 pF).

The buffered input is then mixed with the LO2, and the output of the mixer (IF1) drives an off-chip bandpass filter centered at the IF2 frequency (6.9 MHz for a 110.592 MHz 1IF). The filtered signal is then fed to the IFIP1 pin, which is the input to the limiting amplifier chain. The limiting amplifier requires two external decoupling capacitors from pins DC1A and DC1B to ground (recommended value 10 nF).

The limiting amplifier chain also feeds the Received Signal Strength Indicator (RSSI) block. The RSSI signal is monotonic over a 75 dB dynamic range, and in its linear range varies at 17 mV/dB. The RSSI signal is designed to be digitized by the CMOS burst mode controller.

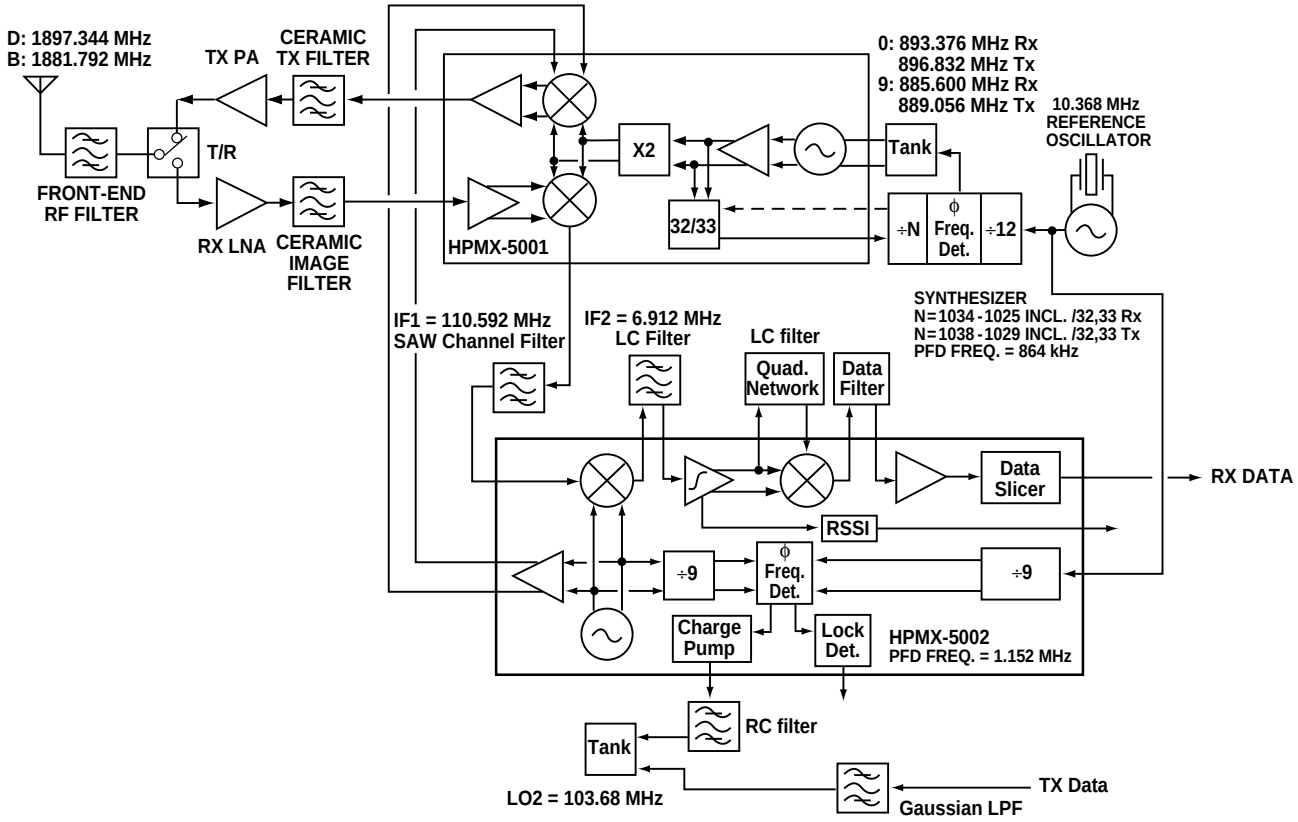
The output of the limiting amplifier (IFOP1) drives the discriminator circuit. This signal is fed directly to one of the input ports of a Gilbert cell mixer, and it also drives an external quadrature network (with a recommended Q of 8 for optimum performance). The output of the external quadrature network is then fed into the other input port of the Gilbert cell (via the DMOD pin). The output of the Gilbert cell is taken at the DMODOP pin, which drives an external lowpass filter. To aid in the construction of the filter, a buffer stage is included on-chip. The BUF1 pin is the noninverting input of the buffer, and BUF2 is the output, which is also connected to the input of the data slicer.

The data slicer operates on a dual time constant architecture, controlled via the TCSET pin. During the preamble portion of a DECT timeslot (with TCSET set to 1), the data slicer quickly acquires the midpoint voltage of the incoming data stream, correcting any DC offsets that may have occurred due to frequency deviations within the DECT specification. The value of this initial time

constant is determined by an internal resistor of 250 Ω (Figure 7) and an external capacitor connected between TCNT and ground. A 10 nF capacitor allows the accurate acquisition of the midpoint voltage within half of the 16-bit DECT preamble.

Once the midpoint voltage has been acquired, TCSET is then forced to a 0, and the time constant of the midpoint voltage tracking circuit is increased by a factor of 80 due to the increase of the internal resistor to 20 kΩ (Figure 7). This effectively freezes the midpoint voltage from any variations due to normal data transitions, but still allows for some correction of frequency drifts during the data burst.

The output of the data slicer (DATOP) is a CMOS-compatible bitstream. However, it is recommended that an external NPN amplifier stage be used to drive the CMOS baseband processor, in order to minimize the amount of ground and supply currents in the HPMX-5002 which might desensitize the chip.



All other connections go to Burst Mode Controller, power source, or ground.

Figure 3. Typical HPMX-5002 Application with HPMX-5001 T/R Chip.

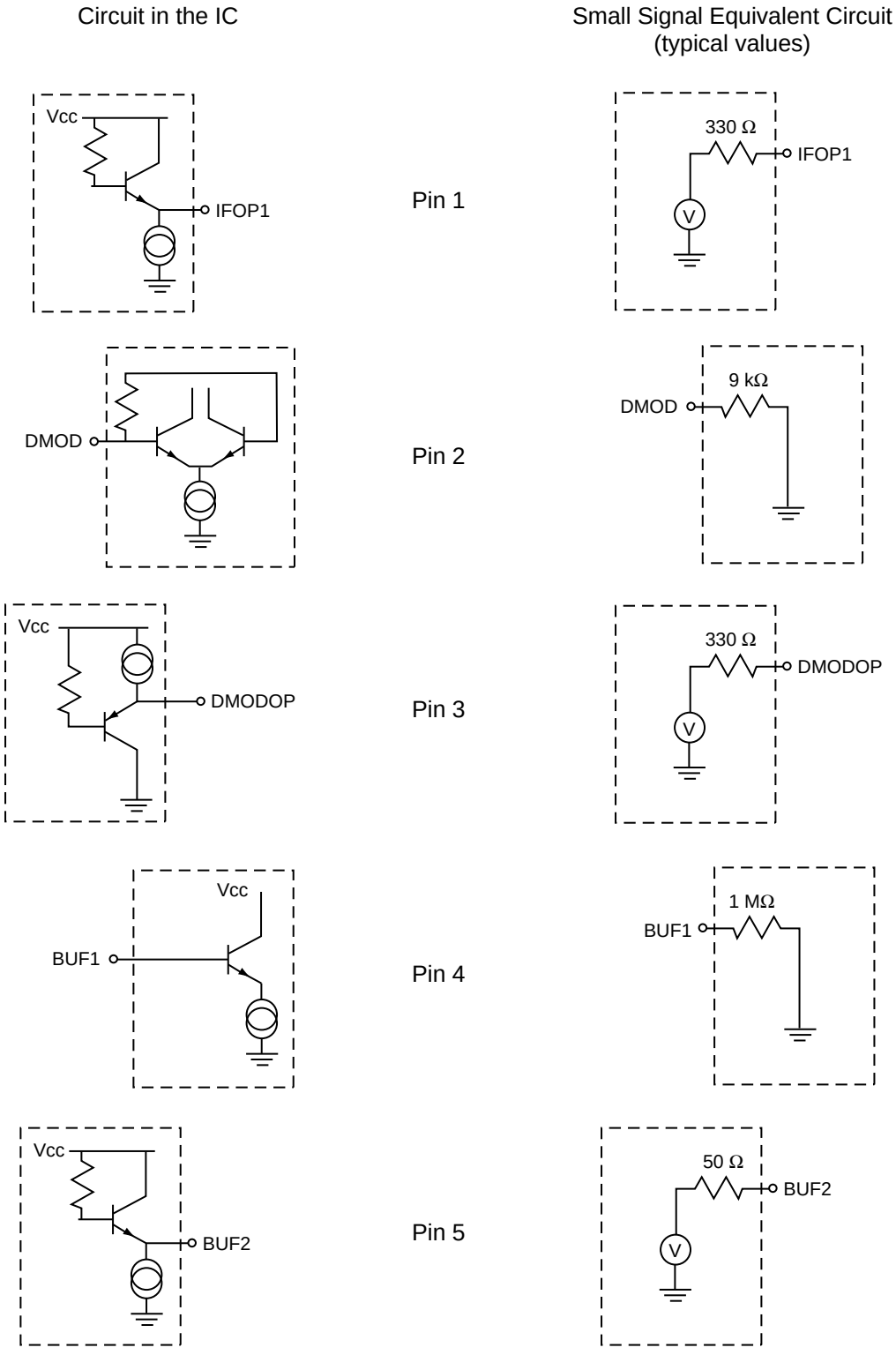


Figure 4. HPMX-5002 Internal and Equivalent Circuits, Pins 1-5.

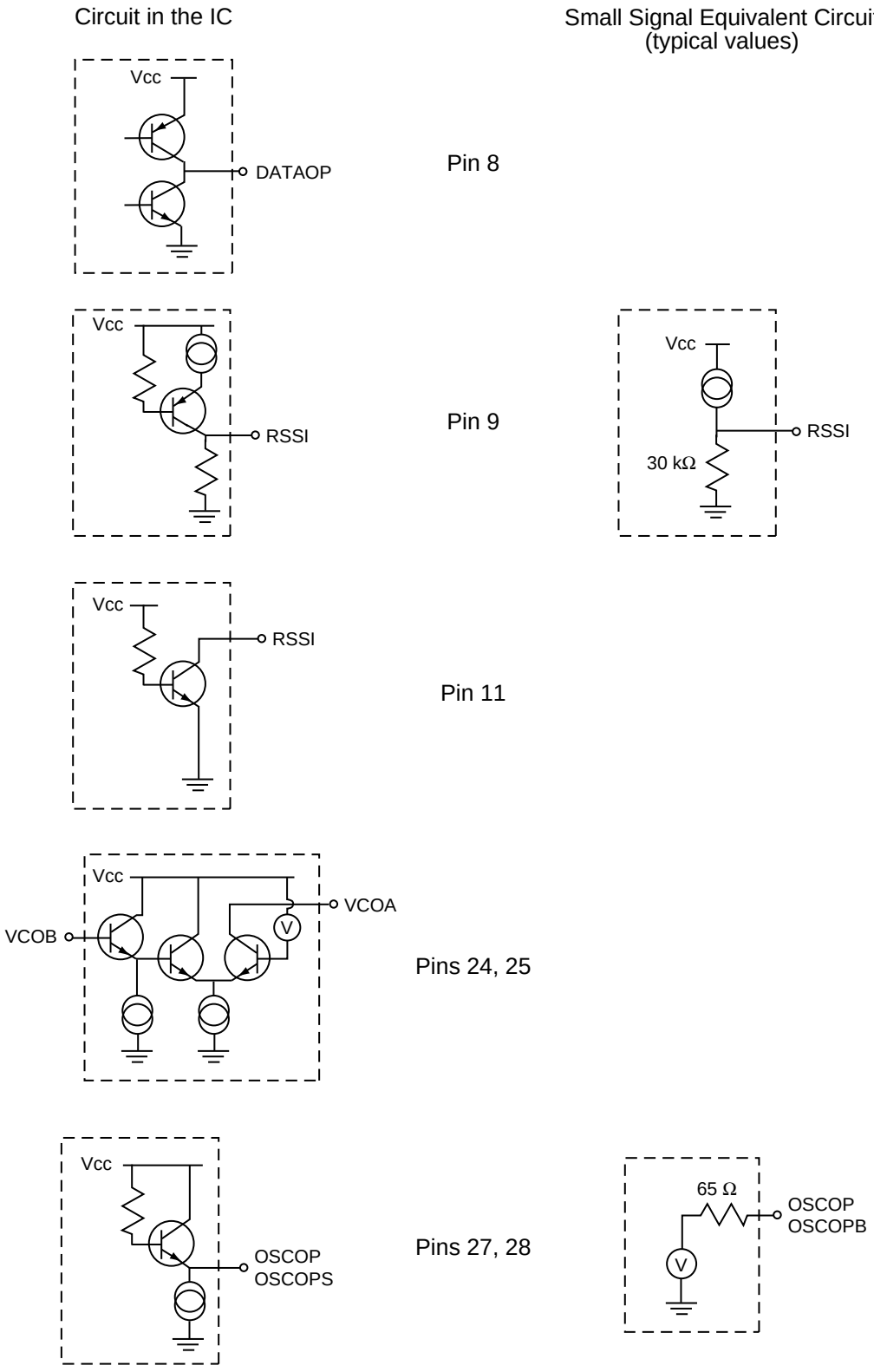


Figure 5. HPMX-5002 Internal and Equivalent Circuits, Pins 8, 9, 11, 24, 25, 27, and 28.

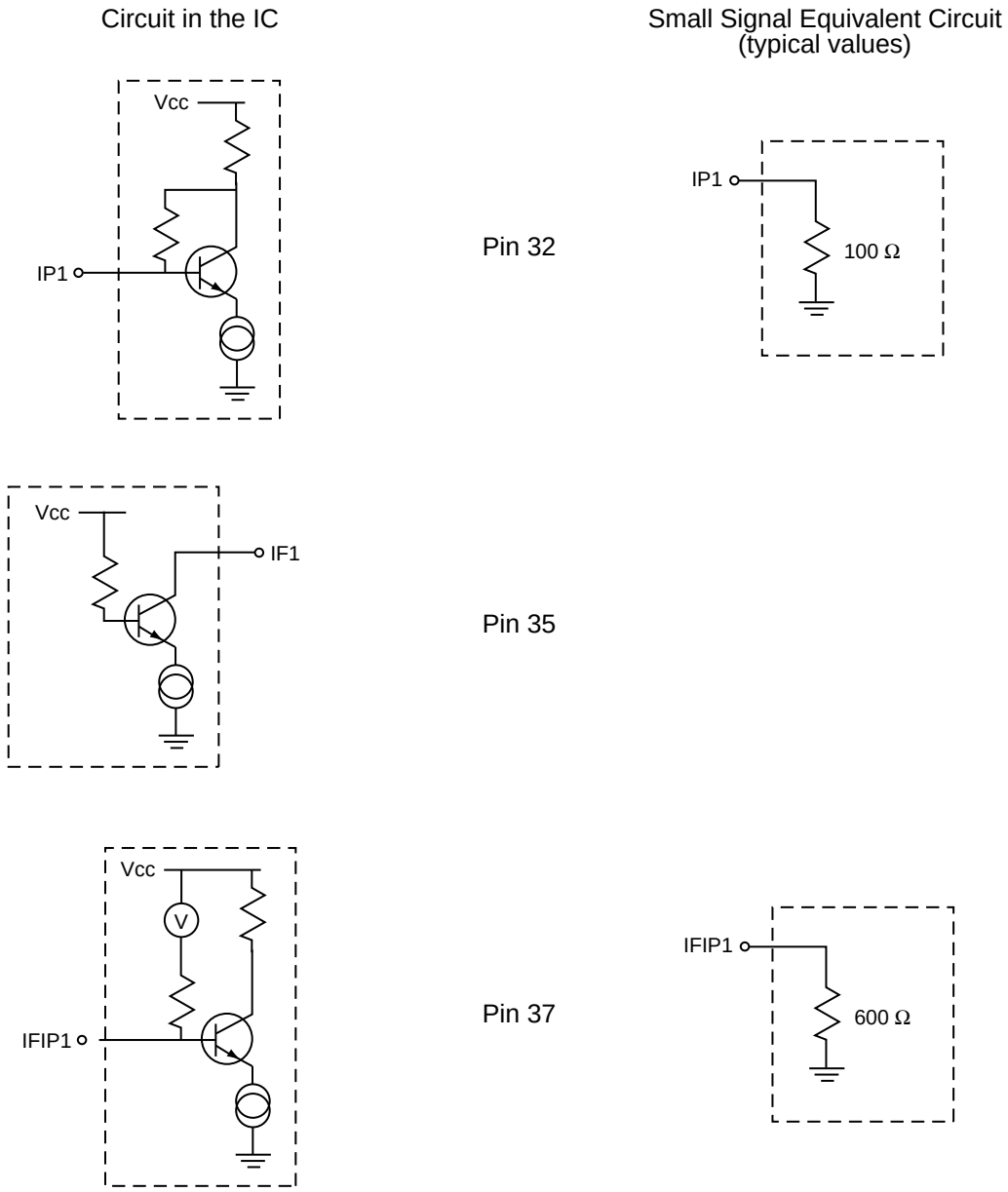
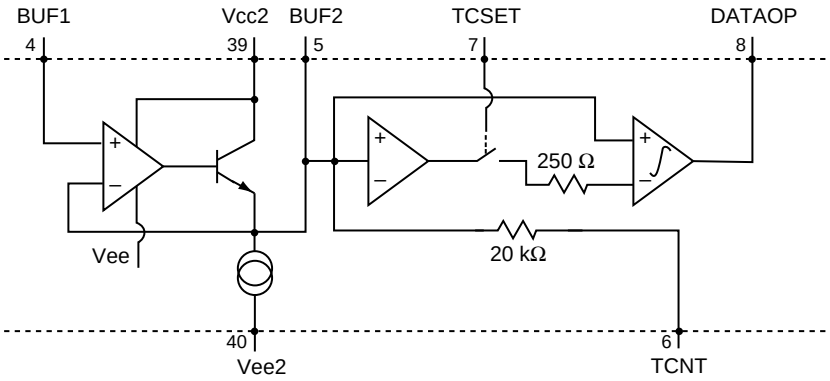
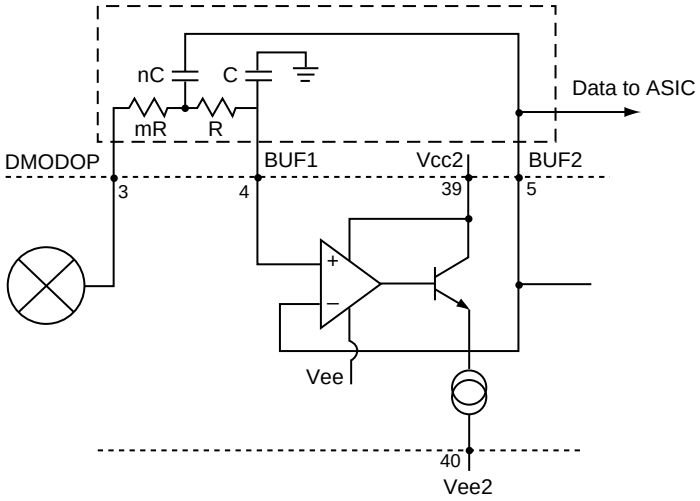


Figure 6. HPMX-5002 Internal and Equivalent Circuits, Pins 32, 35, and 37.



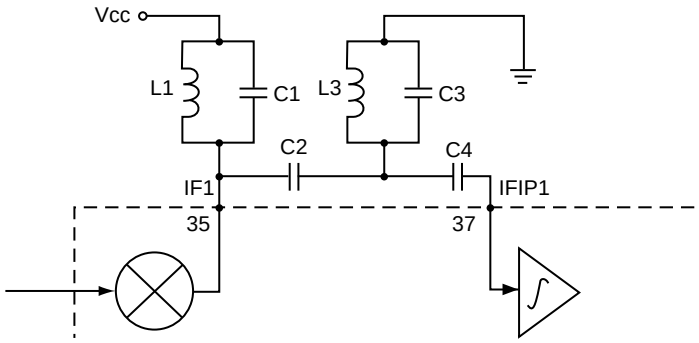


$$H = \frac{BUF2}{DMODOP} = \frac{1}{1 - \left(\frac{f}{f_0}\right)^2 + j\left(\frac{f}{Qf_0}\right)}$$

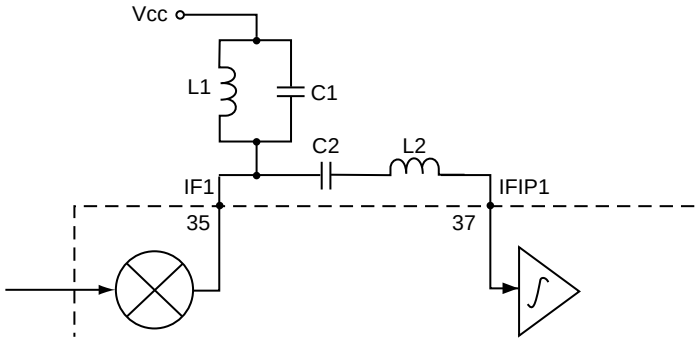
$$|H| = \frac{1}{\sqrt{\left(1 - \left(\frac{f}{f_0}\right)^2\right)^2 + \left(\frac{f}{Qf_0}\right)^2}}$$

$$\text{where } f_0 = \frac{1}{2\pi\sqrt{(mn)RC}} \quad \text{and } Q = \frac{\sqrt{mn}}{m+1}$$

Figure 7. HPMX-5002 Data Filter and Bit Slicer Circuits.



(a)



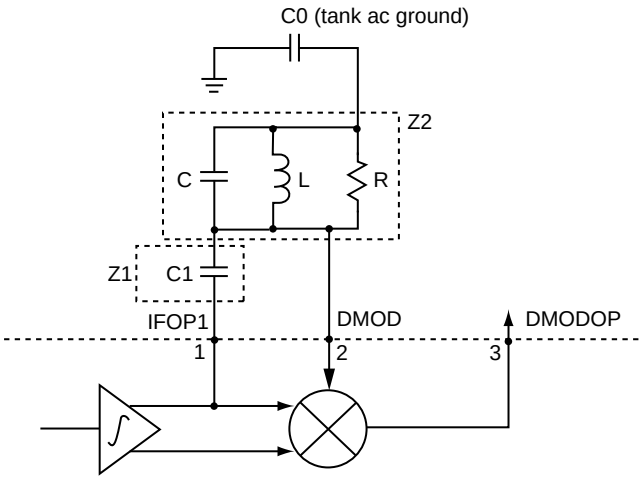
(b)

Example: component values for the filter topology in (b) are:

C1 = 24 pF L1 = 27 µH
C2 = 82 pF L2 = 82 µH

Filter Z_o = 600 Ω, in/out

Figure 8. Typical 2-element filter topologies for the 2nd IF stage at 6.912 MHz.



$$\frac{DMOD}{IFOP1}(s) = \frac{Z_2}{Z_2 + Z_1} \quad \text{where } Z_2 = \frac{1}{\frac{1}{sL} + \frac{1}{R} + sC} \quad \text{and } Z_1 = \frac{1}{sC_1}$$

$$\frac{DMOD}{IFOP1} = \frac{\frac{1}{\frac{1}{sL} + \frac{1}{R} + sC}}{\frac{1}{\frac{1}{sL} + \frac{1}{R} + sC} + \frac{1}{sC_1}} = \frac{sC_1}{\frac{1}{sL} + \frac{1}{R} + sC + sC_1} = \frac{sRC_1}{1 + sR\left[(C + C_1) + \frac{1}{s^2L}\right]}$$

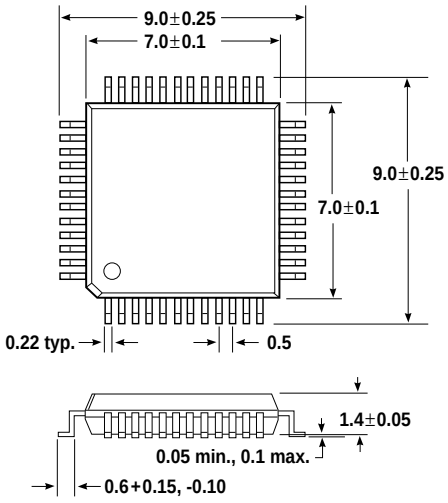
$$\text{Let } \omega_c^2 = \frac{1}{L(C + C_1)} \quad \text{and } Q = \frac{R}{\omega_c L} = R\omega_c (C + C_1)$$

$$\frac{DMOD}{IFOP1}(\omega) = \frac{j\omega RC_1}{1 + jQ\left(\frac{\omega}{\omega_c} - \frac{\omega_c}{\omega}\right)} \quad \text{and } \phi = \frac{\pi}{2} + \tan^{-1}\left[Q\left(\frac{\omega}{\omega_c} - \frac{\omega_c}{\omega}\right)\right]$$

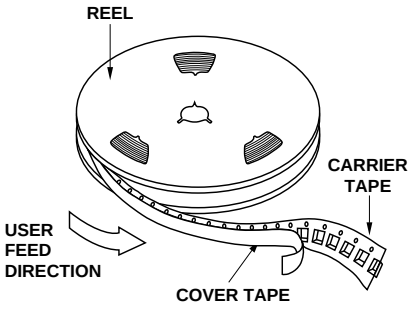
Figure 9. Typical Topology for the Quadrature Network.

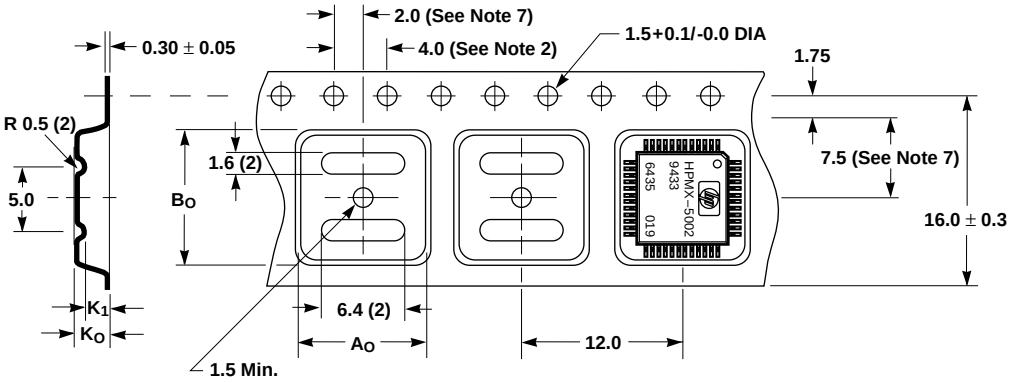
Package Dimensions 48 Pin Thin Quad Flat Package

All dimensions shown in mm.



Tape Dimensions and Product Orientation for Outline TQFP-48





Cover tape width = 13.3 ± 0.1 mm
Cover tape thickness = 0.051 mm (0.002 inch)

A_O = 9.3 mm
B_O = 9.3 mm
K_O = 2.2 mm
K_1 = 1.6 mm

NOTES:
1. Dimensions are in millimeters
2. 10 sprocket hole pitch cumulative tolerance ±0.2
3. Chamber not to exceed 1 mm in 100 mm
4. Material: black conductive Advantek™ polystyrene
5. A_O and B_O measured on a plane 0.3 mm above the bottom of the pocket.
6. K_O measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Part Number Ordering Information

Part Number	No. of Devices	Container
HPMX-5002-STR	10	Strip
HPMX-5002-TR1	1000	Tape and Reel
HPMX-5002-TY1	250	Tray

www.hp.com/go/rf

For technical assistance or the location of your nearest Hewlett-Packard sales office, distributor or representative call:

Americas/Canada: 1-800-235-0312 or 408-654-8675

Far East/Australasia: Call your local HP sales office.

Japan: (81 3) 3335-8152

Europe: Call your local HP sales office.

Data subject to change.

Obsoletes 5967-5488E
Printed in U.S.A. 5967-6372E (6/98)