# HR1215

## Multi-Mode PFC and Current Mode LLC Controller without Shutdown during X-Capacitor Discharge Period

## DESCRIPTION

The HR1215 is a multi-mode PFC and current mode LLC combo controller that is configurable via a UART interface. Power-saving technology optimizes efficiency across the entire operating range.

The PFC controller employs a patented, digital average current control scheme to achieve hybrid continuous conduction mode and discontinuous conduction mode (CCM/DCM). At heavy loads, CCM reduces the peak MOSFET current so that the controller can be used across a wider load range. At light loads, DCM reduces the switching frequency ($f_{SW}$) for improved efficiency. Burst mode has configurable, digital soft switching that can improve both light-load efficiency and audible noise.

Current mode control is implemented in the LLC stage for improved system stability and fast transient response. Three operation modes are implemented based on the different load conditions: steady state, skip mode, and burst mode. This allows different load conditions to be optimized independently for improved efficiency. At light loads, digital, frequency-controlled burst mode is applied to reduce both switching power loss and audible noise. Adaptive dead time adjustment (ADTA) and capacitive mode protection (CMP) are also applied to guarantee zero-voltage switching (ZVS) without capacitive mode.

The HR1215 has an internal, high-voltage current source for start-up. This means that a traditional start-up resistor or external circuit is not required. The high-voltage (HV) current source can be implemented as an X-capacitor discharger while the AC input is in dropout, so a capacitor resistor is not required.

Full protection features include thermal shutdown, open-loop protection (OLP), over-voltage protection (OVP), over-current limit (OLC), over-current protection (OCP), SO pin protection, and over-power protection (OPP).

The HR1215 is available in a SOIC-20 package.

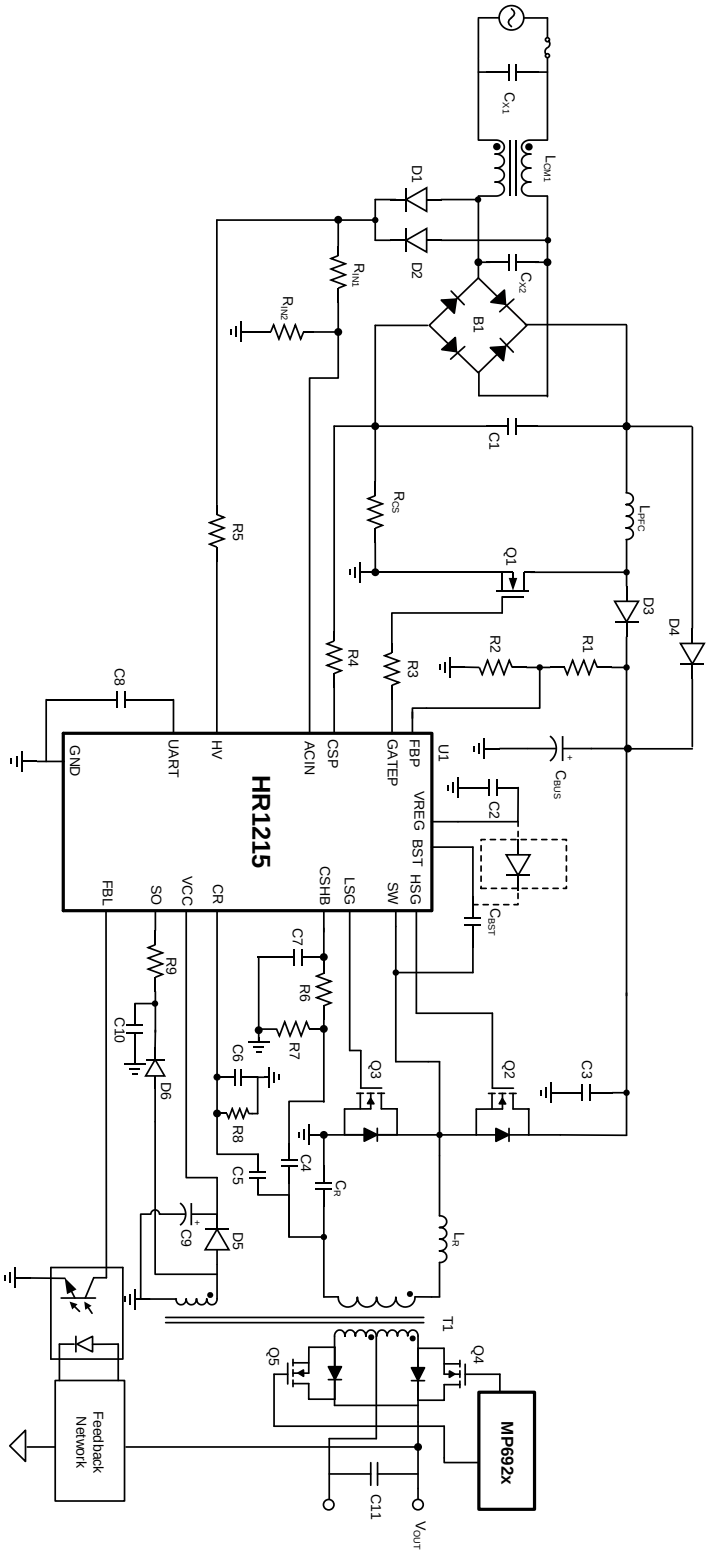
## FEATURES

- General System Features:
  - HV Current Source for Start-Up
  - Smart X-Capacitor Discharge during AC Dropout, Approved by IEC62368
  - UART Interface for Configurations
  - User-Friendly GUI for Digital PFC
- PFC Controller:
  - CCM/DCM Multi-Mode PFC Control with High Efficiency across All Loads
  - Up to 250kHz Operating Frequency
  - High PF due to Input Capacitor ($C_{IN}$) Current Compensation
  - Configurable Frequency Jittering
  - Configurable Soft Start (SS)
  - Configurable Burst On
  - Configurable AC Input Brown-In/Out
  - Cycle-by-Cycle Current Limiting
  - OLP and OVP
- LLC Controller:
  - 600V High-Side MOSFET (HS-FET) Gate Driver with Bootstrap (BST) Diode and High dV/dt Immunity
  - Current Mode Control
  - Up to 500kHz in Steady State
  - ADTA with Min and Max Limit
  - Burst Mode/Skip Mode Switching at Light Loads
  - Configurable Burst Frequency with Low Audible Noise
  - Configurable SS
  - Configurable DC Input Brown-In/Out
  - Capacitive Mode Protection
  - OCP/OPP with Auto-Restart or Latch
  - Configurable Protection on SO Pin

## APPLICATIONS

- Desktop PCs and ATX Power Supplies
- All-in-One and Gaming Power Supplies
- Notebook Adapters
- LCD TV and Plasma TV Power Supplies
- Power Tools Power Supply LED Drivers

## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Rating |
|---|---|---|---|
| HR1215GY-xxxx | SOIC-20 | *See Below* | 3 |

* For Tape & Reel, add suffix -Z (e.g. HR1215GY-xxxx-Z).

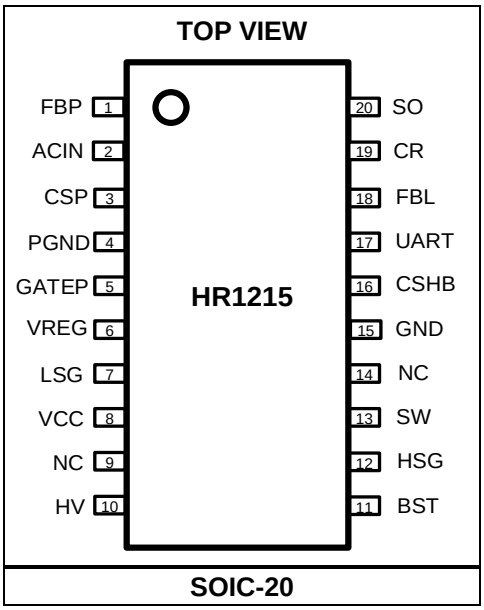
*xxxx is for internal code version control. For customer-specific projects, MPS will assign a special 4-digit number.

## TOP MARKING

MPSYYWW
HR1215
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
HR1215: Part number
LLLLLLLLL: Lot number

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | FBP | **PFC output voltage sense.** The FBP pin senses the PFC output voltage ($V_{OUT}$) to calculate the PFC switch on time ($t_{ON}$), to monitor for over-voltage protection (OVP) and open-loop protection (OLP), and to calculate the digital current reference ($I_{REF}$ (n)). $I_{REF}$ (n) determines the PFC switching frequency ($f_{PFC}$). A 3.3MΩ pull-down resistor is connected to FBP internally. It is recommended to connect a capacitor (about 4.7nF) to FBP for noise immunity. |
| 2 | ACIN | **AC input voltage sense.** The ACIN pin senses the AC input voltage ($V_{ACIN}$) to calculate the PFC switch $t_{ON}$, to monitor for brown-in/brown-out protection, and to calculate $I_{REF}$ (n) . $I_{REF}$ (n) determines $f_{PFC}$. It is recommended to connect a capacitor (about 2.2nF) to ACIN for noise immunity. |
| 3 | CSP | **PFC switching current sense.** The CSP pin defines the PFC switch $t_{ON}$, $f_{PFC}$, and cycle-by-cycle over-current limit (OCL). Connect a 500Ω resistor in series between the current-sense resistor (R1) and the CSP pin via the internal ESD clamping capability. This resistor prevents CSP from overstress under AC plug-in or surge conditions. Another solution is to add an external clamping component to CSP. |
| 4 | PGND | **Ground reference for the PFC and LLC low-side MOSEFT (LS-FET) gates.** |
| 5 | GATEP | **PFC gate driver output.** |
| 6 | VREG | **Provides a regulated voltage for the PFC and LLC gate drivers and internal circuits.** |
| 7 | LSG | **LLC LS-FET gate driver output.** |
| 8 | VCC | **IC supply power.** The VCC pin can be charged by an internal current source via the HV pin or an external power supply. |
| 9 | NC | **Not connected.** |
| 10 | HV | **High-voltage supply input for the internal HV start-up source and X-capacitor discharger while $V_{ACIN}$ drops out.** |
| 11 | BST | **Bootstrap voltage.** An internal bootstrap diode is connected between the BST and VCC pins. Connect an external capacitor between the BST and SW pins to drive the high-side MOSFET of the half-bridge LLC. |
| 12 | HSG | **LLC high-side gate driver output.** |
| 13 | SW | **HS-FET source.** The SW pin is the current return for the high-side gate (HSG) driver current. SW requires additional layout considerations to avoid creating large spikes below ground. |
| 14 | NC | **Not connected.** |
| 15 | GND | **Ground reference for the digital PFC core.** |
| 16 | CSHB | **Half-bridge current sense.** Use a current-sense resistor or a capacitive divider to sense the primary current. The CSHB pin has the following functions:<br>• Over-current protection (OCP): If the current continues to rise despite the increasing frequency, the CSHB voltage ($V_{CSHB}$) exceeds the OCP threshold ($V_{OCP}$), then OCP is triggered and the IC initiates its configured protection mode (auto-retry or latch-off mode).<br>• Capacitive mode protection (CMP): $V_{CSHB}$ is compared to the current polarity reference while the HS-FET gate is on ($V_{CS\_PR}$) and while LS-FET gate is on ($V_{CS\_NR}$) to determine whether the LLC current is in a positive or negative polarity. If the current goes into negative polarity ($V_{CSHB} < V_{CS\_PR}$), then the IC terminates the HS-FET gate driver. If the current goes into positive polarity ($V_{CSHB} > V_{CS\_NR}$), then the IC terminates the LS-FET gate driver. |
| 17 | UART | **Half-duplex communication I/O interface.** The UART pin provides a half-duplex communication I/O interface. UART is pulled up to 3.3V internally via a 1.6kΩ resistor ($R_{UART}$). It is not recommended to rely on real-time communication in application. Do not pull UART high if the VCC voltage ($V_{CC}$) drops below the second under-voltage protection (UVP) threshold ($V_{CC\_UVP2}$). |

## PIN FUNCTIONS *(continued)*

| Pin # | Name | Description |
|---|---|---|
| 18 | FBL | **LLC output voltage feedback input.** The FBL pin is pulled up internally via a voltage source with an internal resistor. FBL defines the LLC switching frequency ($f_{LLC}$) according to the load condition. The LLC feedback voltage ($V_{FBL}$) activates LLC skip mode, burst mode, and over-power protection (OPP). |
| 19 | CR | **LLC capacitor voltage-sense input.** The CR pin senses the divided resonant capacitor voltage to determine $f_{LLC}$. |
| 20 | SO | **External protection input.** If the sensed SO voltage ($V_{SO}$) exceeds the OVP threshold ($V_{OVP}$), then OVP is triggered and the IC initiates its configured mode (auto-retry or latch-off mode). To achieve external over-temperature protection (OTP), attach an external NTC to this pin (see Figure 40). |

## ABSOLUTE MAXIMUM RATINGS (1)

$V_{HV}$ to $V_{PGND}$ ..... -0.3V to +700V
$V_{BST}$ to $V_{PGND}$ ..... -0.3V to +618V
$V_{SW}$ to $V_{PGND}$ ..... -3V to +618V (2)
$V_{HSG}$ to $V_{PGND}$ ..... 618V
$V_{LSG}$ to $V_{PGND}$ ..... -0.3V to +14V
$V_{BST}$ to $V_{SW}$ ..... -0.3V to +14V
$V_{HSG}$ to $V_{SW}$ ..... -0.3V to +14V
SW to PGND maximum slew rate ..... 50V/ns
$V_{CC}$ to $V_{PGND}$ ..... -0.3V to +38V
$V_{REG}$ to $V_{PGND}$ ..... -0.3V to +14V
$V_{GATEP}$ to $V_{PGND}$ ..... -0.3V to +14V
$V_{CR}$, $V_{CSHB}$ to $V_{GND}$ ..... -3.3V to +3.6V (2)
$V_{CSP}$ to $V_{GND}$ ..... -5V to +3.6V
$V_{PGND}$ to $V_{GND}$ ..... -0.3V to +0.3V
All other pins to $V_{PGND}$ ..... -0.3V to +3.6V
VREG supply current ..... 40mA
BST internal diode average forward current (3) ..... 0.2A
CSP input current limit at negative voltage overstress (clamped by internal ESD device) (2)
2ms single pulse ..... -0.15A
100µs single pulse ..... -0.17A
20µs single pulse ..... -0.20A
Continuous power dissipation ($T_A$ = 25°C) (4)
SOIC-20 ..... 1.92W
TSSOP-20 ..... 1.38W
Storage temperature ..... -55°C to +150°C
Junction temperature ..... -40°C to +150°C
Lead temperature ..... 260°C

### *ESD Ratings* (1)

Human body model (HBM) ..... 2000V
Charged device model (CDM) ..... 1500V

### *Recommended Operating Conditions* (5)

Supply voltage ($V_{CC}$) ..... 12V to 35V
Operating junction temp ($T_J$) ..... -40°C to +125°C

### *Thermal Resistance* (6) $\theta_{JA}$ $\theta_{JC}$

| | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| SOIC-20 | 65 | 30 | °C/W |
| TSSOP-20 | 90 | 40 | °C/W |

**Notes:**

1) The device is not guaranteed to function outside of its operating conditions.
2) Guaranteed by characterization.
3) Guaranteed by design.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J$ (MAX), the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) Exceeding these ratings may damage the device.
6) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

**$V_{CC}$ = 25V, $T_J$ = -40°C to +125°C, min and max values are guaranteed by characterization, typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **High-Voltage Start-Up Current Source (HV Pin)** | | | | | | |
| Breakdown voltage | $V_{BR}$ | | 700 | | | V |
| HV normal charge current | $I_{HV\_NOR}$ | $V_{SCP} < V_{CC} < 15V$, $T_J$ = 25°C | 5.9 | 7 | 9 | mA |
| Charge current from VCC | $I_{VCC}$ | $V_{CC} = V_{CC\_SU\_HV}$ - 0.1V, $T_J$ = 25°C | 2 | | | mA |
| HV supply current limit when a fault occurs | $I_{HV\_LIMIT}$ | $V_{CC} < V_{SCP}$ | 1.5 | 2.2 | 3 | mA |
| Leakage current threshold during the off state | $I_{LKG\_HV\_OFF}$ | $V_{HV}$ = 400V, $V_{CC}$ = 24V | | 4.5 | 10 | µA |
| **IC Power Supply (VCC Pin)** | | | | | | |
| IC start-up voltage while HV is detected | $V_{CC\_SU\_HV}$ | | 20 | 21.5 | 23 | V |
| Under-voltage protection (UVP) threshold 1 | $V_{CC\_UVP1}$ | | 10 | 10.8 | 11.5 | V |
| UVP threshold 2 | $V_{CC\_UVP2}$ | | 13.5 | 14.4 | 15.2 | V |
| IC restart (RST) threshold | $V_{RST}$ | | 8 | 8.8 | 9.3 | V |
| X-capacitor discharge regulation voltage (7) | $V_{CC\_XCD}$ | | | 17 | | V |
| Short-circuit protection threshold | $V_{SCP}$ | | 0.76 | 0.94 | 1.4 | V |
| Normal operating current | $I_{VCC\_NOR}$ | $C_{GATEP}$ = 1nF, $f_{PFC}$ = 100kHz, $C_{HSG}$ = 1nF, $C_{LSG}$ = 1nF, $f_{LLC}$ = 200kHz | | 15 | | mA |
| | | No switching, $T_J$ = 25°C | | 8 | 10 | |
| Start-up current | $I_{VCC\_SU}$ | $V_{CC}$ = 20V | | 2.1 | 3 | mA |
| Burst mode current | $I_{BURST}$ | Burst mode off, $T_J$ = 25°C | | 2.2 | 2.7 | mA |
| **X-Capacitor Discharger (HV Pin)** | | | | | | |
| Discharge current | $I_{DISCHARGE}$ | $T_J$ = 25°C | 5.9 | 7 | 9 | mA |
| Discharge clock time | $t_{DISCHARGE}$ | | 0.8 | 1.6 | 2.6 | ms |
| **PFC Gate Driver (GATEP Pin)** | | | | | | |
| Minimum gate high voltage | $V_{OUT\_HIGH}$ | $C_{GATEP}$ = 1nF, 20mA source, $V_{REG}$ = 11.5V | 11.3 | | | V |
| Maximum gate low voltage | $V_{OUT\_LOW}$ | $C_{GATEP}$ = 1nF, 20mA sink, $V_{REG}$ = 11.5V | | | 0.1 | V |
| Gate on resistance | $R_{DS(ON)\_HIGH}$ | 20mA source | | 4.5 | 7.5 | Ω |
| | $R_{DS(ON)\_LOW}$ | 20mA sink | | 2.5 | 5 | Ω |
| Voltage fall time | $t_{FALL\_GATEP}$ | $C_{GATEP}$ = 1nF | | 20 | 40 | ns |
| Voltage rise time | $t_{RISE\_GATEP}$ | $C_{GATEP}$ = 1nF | | 20 | 40 | ns |
| Source capacity (7) | $I_{SOURCE}$ | | | 650 | | mA |
| Sink capacity (7) | $I_{SINK}$ | | | 800 | | mA |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{CC}$ = 25V, $T_J$ = -40°C to +125°C, min and max values are guaranteed by characterization, typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Regulated Power Supply (VREG Pin)** | | | | | | |
| Regulated output voltage | $V_{REG}$ | $I_{REG}$ = 0mA | 11 | 12 | 13 | V |
| | | $I_{REG}$ = 20mA | 10.8 | 11.9 | 12.8 | V |
| Start-up threshold | $V_{REG\_SU}$ | | 9 | 10 | 10.9 | V |
| UVP threshold | $V_{REG\_UVP}$ | | 6.5 | 7.3 | 8.1 | V |
| **System Clock** | | | | | | |
| Normal operating clock frequency | $f_{OSC\_LLC}$ | LLC normal operation | 180 | 200 | 223 | MHz |
| | $f_{OSC\_PFC}$ | PFC normal operation | 16.6 | 17.5 | 18.7 | MHz |
| Burst mode clock frequency (7) | $f_{OSC\_NOPWM}$ | While burst mode is off or if a fault occurs | | 1 | | MHz |
| **AC Input Voltage Sensing (ACIN Pin)** | | | | | | |
| Voltage range | | | 0 | | 1.6 | V |
| **PFC Feedback (FBP Pin)** | | | | | | |
| Voltage range | | | 0 | | 1.6 | V |
| **Current Sense (CSP Pin)** | | | | | | |
| Voltage range | | | -1.4 | | 0 | V |
| Internal voltage bias | $V_{BIAS}$ | $V_{CSP}$ = 0V | 0.19 | 0.2 | 0.21 | V |
| **UART Interface (UART Pin)** | | | | | | |
| Internal pull-up voltage | | | | 3.3 | | V |
| Internal pull-up resistor | | | | 1.6 | | kΩ |
| **Analog-to-Digital Converter (ADC) for CSP Pin** | | | | | | |
| ADC reference voltage | | | 1.585 | 1.6 | 1.61 | V |
| | | $T_J$ = 25°C | 1.595 | 1.6 | 1.605 | V |
| ADC resolution (8) | | | | 12 | | bits |
| Acquisition time (7) | | | | 300 | | ns |
| Offset error (8) | | | | ±0.5 | | LSB |
| Gain error (8) | | | | ±1.5 | | LSB |
| **ADC for ACIN, FBP, and FBL Pins** | | | | | | |
| ADC reference voltage | | | 1.585 | 1.6 | 1.61 | V |
| | | $T_J$ = 25°C | 1.595 | 1.6 | 1.605 | V |
| ADC resolution (8) | | | | 10 | | bits |
| Acquisition time (7) | | | | 300 | | ns |
| Offset error (8) | | | | ±0.5 | | LSB |
| Gain error (8) | | | | ±1.5 | | LSB |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{CC}$ = 25V, $T_J$ = -40°C to +125°C, min and max values are guaranteed by characterization, typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Digital-to-Analog Converter (DAC) for PFC Over-Voltage Protection (OVP), Over-Current Protection (OCP), and Brown-In/Brownout (BI/BO) Protection; DAC for LLC Over-Power Protection (OPP) and Ultra-Low Power Mode** | | | | | | |
| DAC reference voltage | | | 1.585 | 1.6 | 1.61 | V |
| | | $T_J$ = 25°C | 1.595 | 1.6 | 1.605 | V |
| DAC resolution (8) | | | | 8 | | bits |
| Offset error (8) | | | | ±0.2 | | LSB |
| Gain error (8) | | | | ±1.5 | | LSB |
| **DAC for PFC Set Signal** | | | | | | |
| DAC reference voltage | | | 1.585 | 1.6 | 1.61 | V |
| | | $T_J$ = 25°C | 1.595 | 1.6 | 1.605 | V |
| DAC resolution (8) | | | | 10 | | bits |
| Offset error (8) | | | | ±0.5 | | LSB |
| Gain error (8) | | | | ±1.5 | | LSB |
| **DAC for LLC Set Signal** | | | | | | |
| DAC voltage reference | | | 1.77 | 1.8 | 1.825 | V |
| | | $T_J$ = 25°C | 1.788 | 1.8 | 1.812 | V |
| DAC resolution (8) | | | | 10 | | bits |
| Offset error (8) | | | | ±0.5 | | LSB |
| Gain error (8) | | | | ±1.5 | | LSB |
| **High-Side MOSFET (HS-FET) Floating Gate Driver Supply (BST and SW Pins)** | | | | | | |
| BST pin leakage current | $I_{LKG\_BST}$ | $V_{BST}$ = 600V | | | 10 | µA |
| SW pin leakage current | $I_{LKG\_SW}$ | $V_{SW}$ = 582V | | | 10 | µA |
| **Half-Bridge Current Sense (CSHB Pin)** | | | | | | |
| OCP threshold | $V_{OCP}$ | | 1.475 | 1.5 | 1.52 | V |
| Current polarity comparator reference when HSG is on | $V_{CS\_PR}$ | $T_J$ = 25°C | 60 | 80 | 100 | mV |
| Current polarity comparator reference when LSG is on | $V_{CS\_NR}$ | $T_J$ = 25°C | -100 | -80 | -60 | mV |
| **Output Voltage Sense (SO Pin)** | | | | | | |
| Over-voltage protection (OVP) on SO | $V_{OVP}$ | | 1.475 | 1.5 | 1.52 | V |
| **Adaptive Dead-Time Adjustment (ADTA) (SW Pin)** | | | | | | |
| Minimum detectable voltage slew rate (7) | $dV_{MIN}/dt$ | | | 85 | | V/µs |
| Start-up delay (7) | $t_{DELAY\_SU}$ | Slope is complete to start-up delay | | 150 | | ns |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{CC}$ = 25V, $T_J$ = -40°C to +125°C, min and max values are guaranteed by characterization, typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

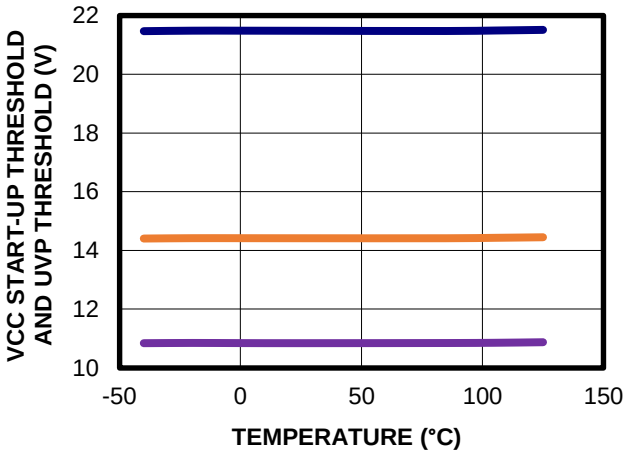
| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **LLC Feedback (FBL Pin)** | | | | | | |
| FBL internal pull-up resistor | $R_{FBL\_LS}$ | $T_J$ = 25°C | 7 | 8 | 9.6 | kΩ |
| FBL internal pull-up resistor in power-save mode | $R_{FBL\_HS}$ | | 38 | 47 | 56 | kΩ |
| Internal reference voltage | $V_{REF}$ | $T_J$ = 25°C | 2.35 | 2.41 | 2.5 | V |
| Comp voltage ($V_{COMP}$) offset voltage from FBL | $V_{FBL\_OFFSET}$ | | 0.995 | 1 | 1.005 | V |
| **Current-Sense Input (CR Pin)** | | | | | | |
| Slope compensation amplitude per LSB | $V_{SLOPE}$ | $T_J$ = 25°C | 1.54 | 2.35 | 3.16 | mV/µs |
| Zero-voltage switching (ZVS) threshold | $V_{ZERO}$ | | 15 | 20 | 25 | mV |
| On-time comparator delay to HG driver off (7) | $t_{DELAY\_CR}$ | | | 150 | | ns |
| Current-sense input leakage current | $I_{LKG\_CR}$ | $V_{CR}$ = 2V | | | ±1 | µA |
| Leading-edge blanking time (7) | $t_{LEB}$ | | | 300 | | ns |
| **Low-Side Gate Driver (LSG Pin)** | | | | | | |
| Peak source current (7) | $I_{SOURCE\_LSG}$ | | | 0.75 | | A |
| Peak sink current (7) | $I_{SINK\_LSG}$ | | | 0.87 | | A |
| Source resistor | $R_{SOURCE\_LSG}$ | | | 5 | 8 | Ω |
| Sink resistor | $R_{SINK\_LSG}$ | | | 2.5 | 5 | Ω |
| Fall time | $t_{FALL\_LSG}$ | | | 20 | 40 | ns |
| Rise time | $t_{RISE\_LSG}$ | | | 20 | 40 | ns |
| **High-Side Gate Driver (HSG Pin, Referenced to the SW Pin)** | | | | | | |
| Peak source current (7) | $I_{SOURCE\_HSG}$ | | | 0.74 | | A |
| Peak sink current (7) | $I_{SINK\_HSG}$ | | | 0.87 | | A |
| Source resistor | $R_{SOURCE\_HSG}$ | | | 5 | 8 | Ω |
| Sink resistor | $R_{SINK\_HSG}$ | | | 2.5 | 5 | Ω |
| Fall time | $t_{FALL\_HSG}$ | | | 20 | 40 | ns |
| Rise time | $t_{RISE\_HSG}$ | | | 20 | 40 | ns |
| **Voltage Bootstrap (BST Pin, Referenced to the SW Pin)** | | | | | | |
| VREG to BST internal diode forward voltage (7) | $V_{FWD}$ | $I_{FWD}$ = 1mA, $T_J$ = 25°C | | 1.2 | | V |
| **Thermal Shutdown** | | | | | | |
| Thermal shutdown threshold (7) | $T_{SD}$ | | | 145 | | °C |
| Thermal shutdown recovery threshold (7) | | | | 120 | | °C |

**Notes:**

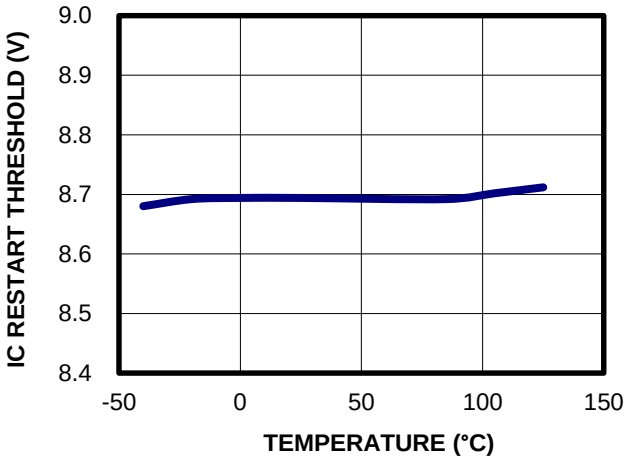
7) Guaranteed by design.
8) Guaranteed by characterization.

## TYPICAL CHARACTERISTICS

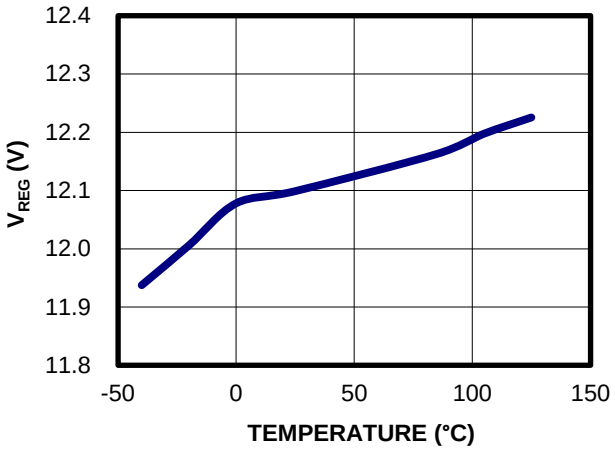
### VCC Start-Up Threshold and UVP Threshold vs. Temperature



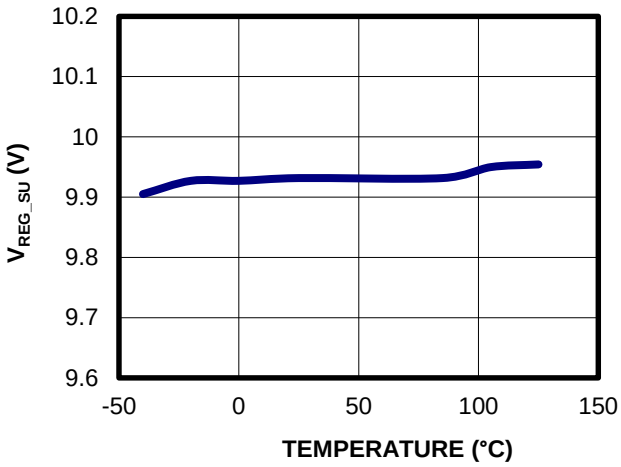

### IC Restart Threshold vs. Temperature



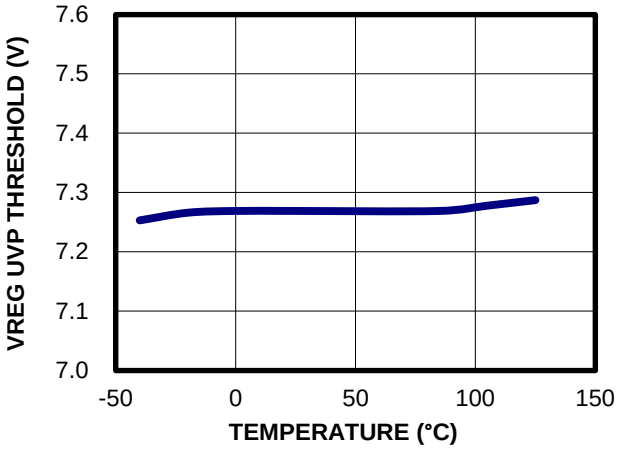

### $V_{REG}$ vs. Temperature



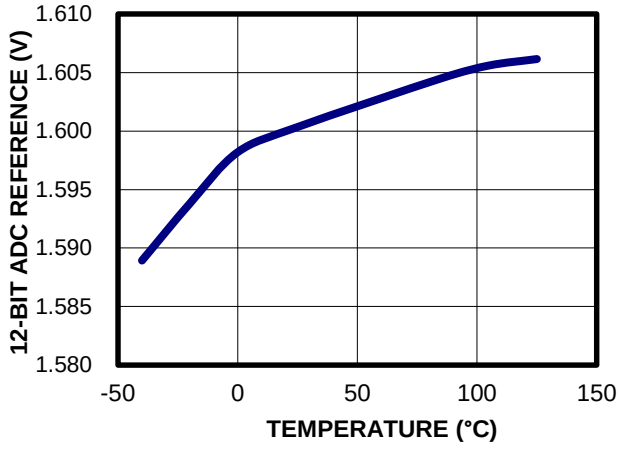

### VREG Start-Up Threshold vs. Temperature




### VREG UVP Threshold vs. Temperature

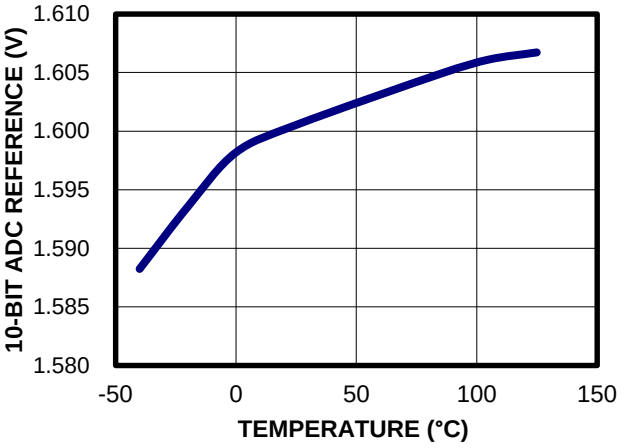



### 12-Bit ADC Reference vs. Temperature

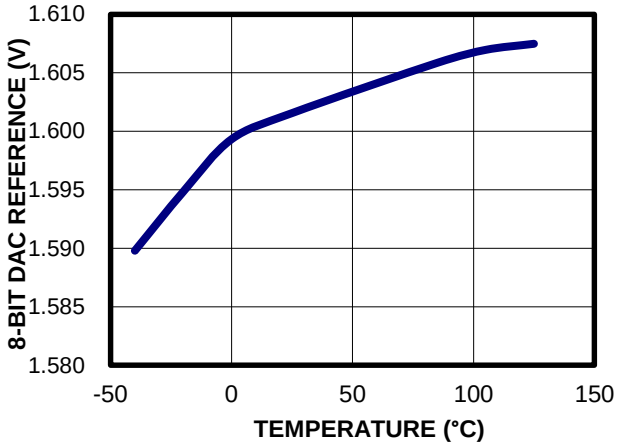


## TYPICAL CHARACTERISTICS *(continued)*

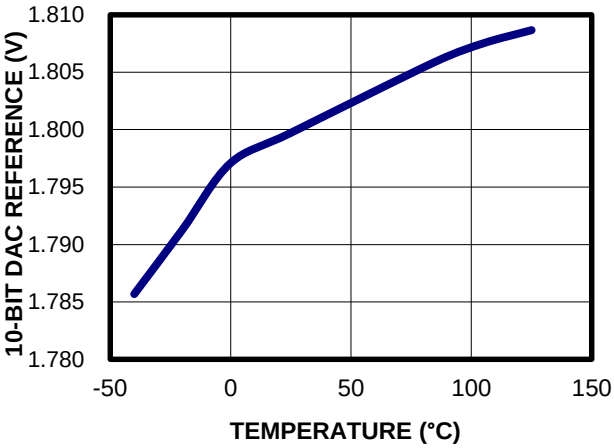
**10-Bit ADC Reference vs. Temperature**



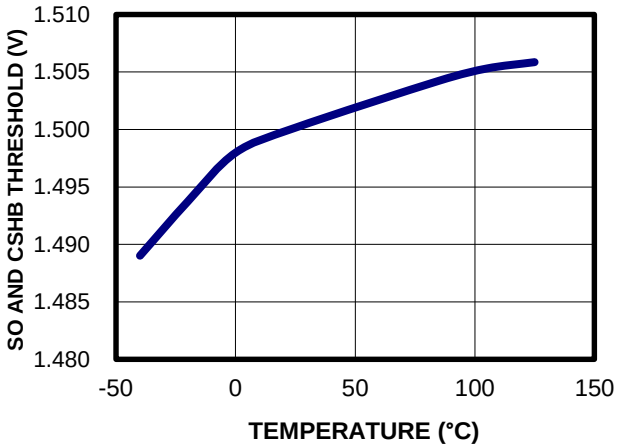

**8-Bit DAC Reference vs. Temperature**



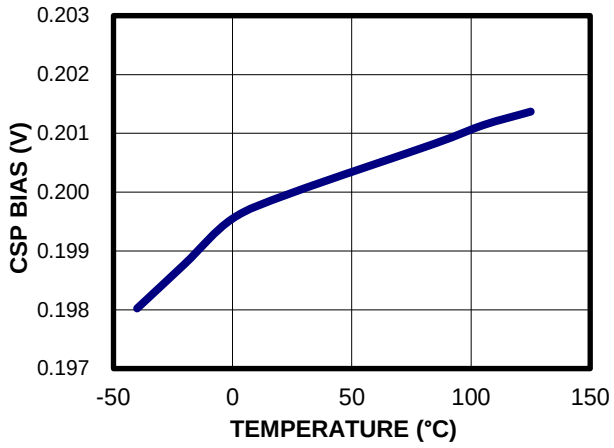

**10-Bit DAC Reference vs. Temperature**



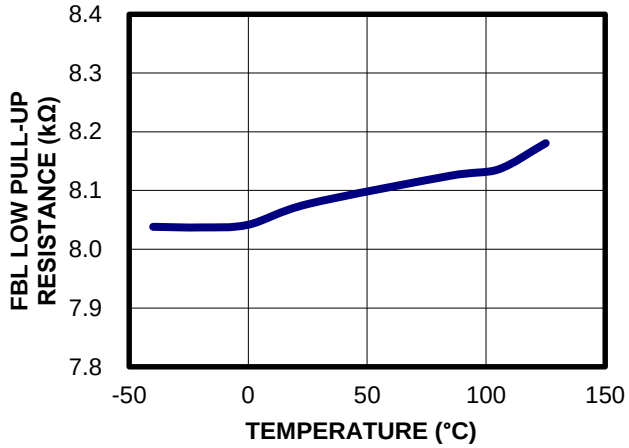

**SO and CSHB Threshold vs. Temperature**




**CSP Bias vs. Temperature**

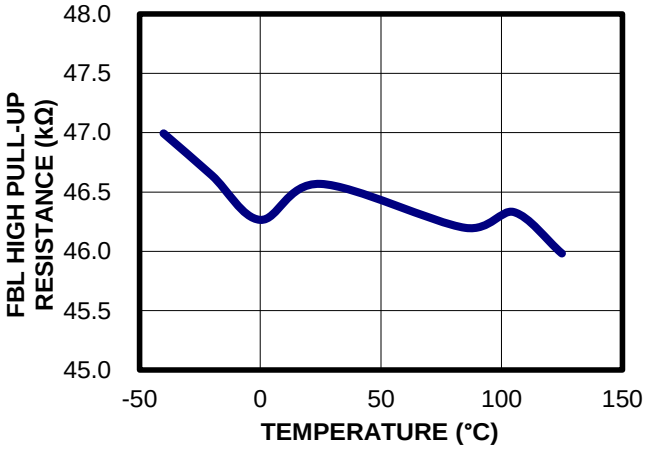



**FBL Low Pull-Up Resistance vs. Temperature**

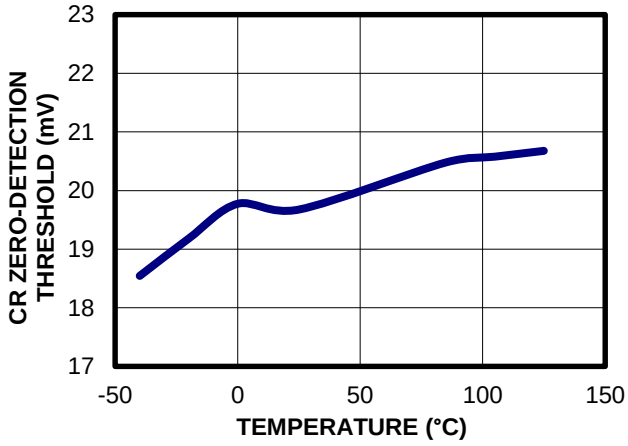


## TYPICAL CHARACTERISTICS *(continued)*

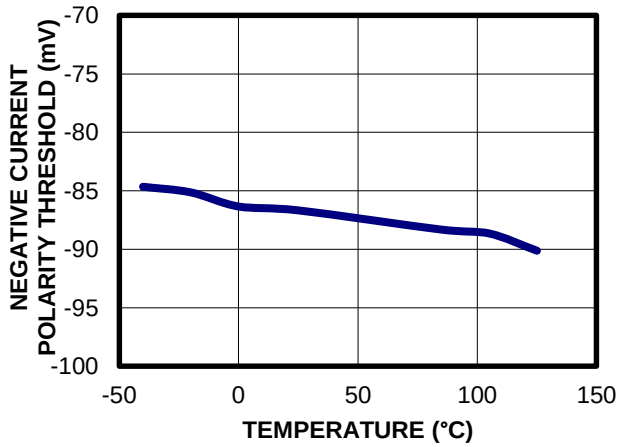
**FBL High Pull-Up Resistance vs. Temperature**



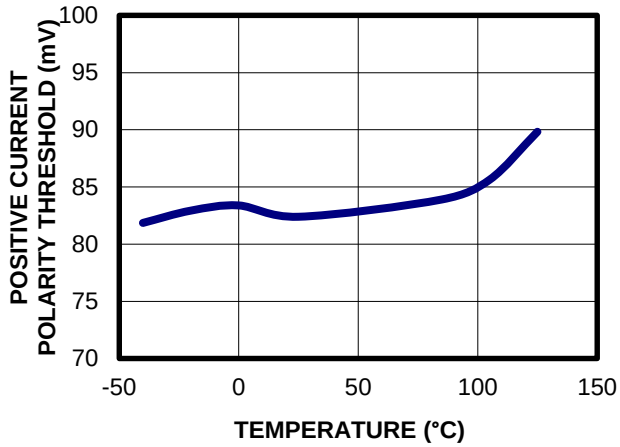

**CR Zero-Detection Threshold vs. Temperature**




**Negative Current Polarity Threshold vs. Temperature**




**Positive Current Polarity Threshold vs. Temperature**

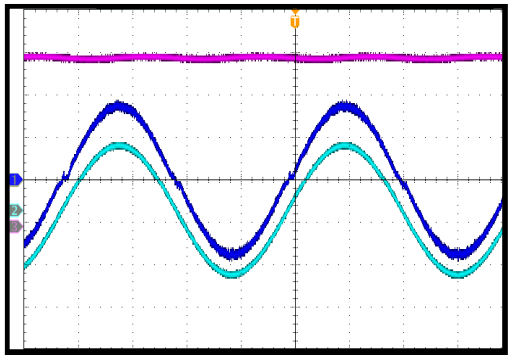


# TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 85$V_{AC}$ to 265$V_{AC}$, $V_{OUT}$ = 12V, $I_{OUT}$ = 20A, $T_A$ = 25°C, unless otherwise noted.**

### Steady State at Input

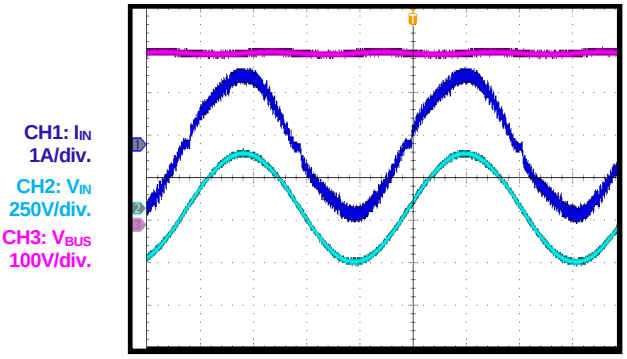
$V_{IN}$ = 110$V_{AC}$, $P_{OUT}$ = 240W




4ms/div.

### Steady State at Input

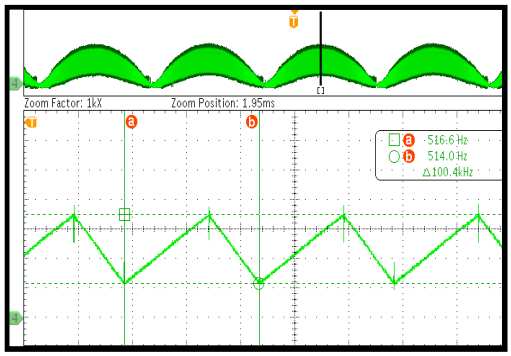
$V_{IN}$ = 230$V_{AC}$, $P_{OUT}$ = 240W




4ms/div.

### Steady State at PFC Choke

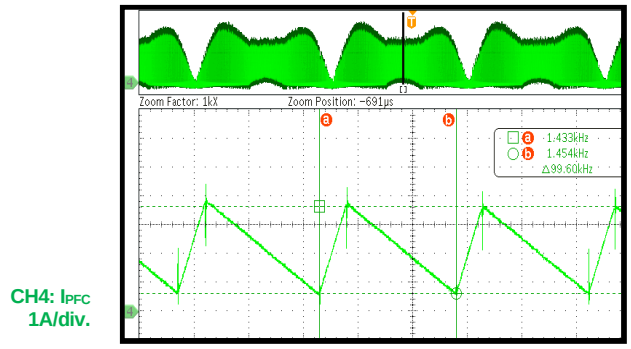
$V_{IN}$ = 110$V_{AC}$, $P_{OUT}$ = 240W




4µs/div.

### Steady State at PFC Choke

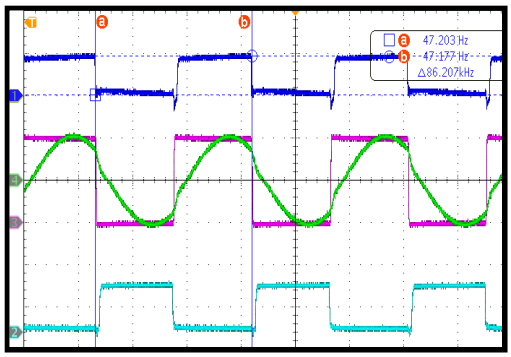
$V_{IN}$ = 230$V_{AC}$, $P_{OUT}$ = 240W




4µs/div.

### Steady State at LLC

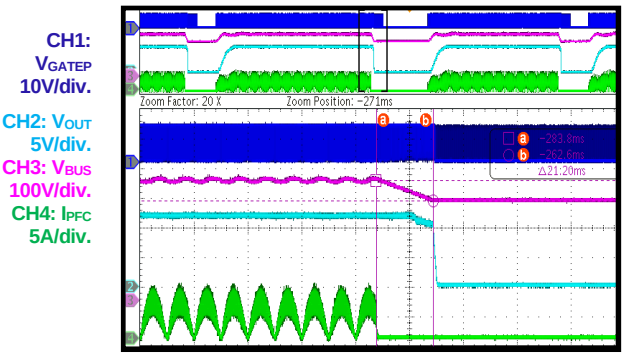
$P_{OUT}$ = 240W




4µs/div.

### Start-Up and Shutdown through $V_{IN}$ at PFC

$V_{IN}$ = 110$V_{AC}$, $P_{OUT}$ = 240W




20ms/div.

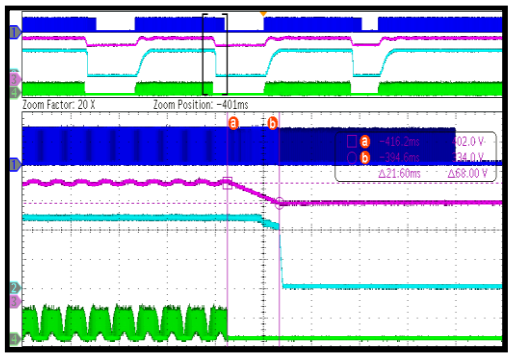
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 85$V_{AC}$ to 265$V_{AC}$, $V_{OUT}$ = 12V, $I_{OUT}$ = 20A, $T_A$ = 25°C, unless otherwise noted.**

### Start-Up and Shutdown through $V_{IN}$ at PFC

$V_{IN}$ = 230$V_{AC}$, $P_{OUT}$ = 240W

CH1: $V_{GATEP}$ 10V/div.
CH2: $V_{OUT}$ 5V/div.
CH3: $V_{BUS}$ 100V/div.
CH4: $I_{PFC}$ 5A/div.

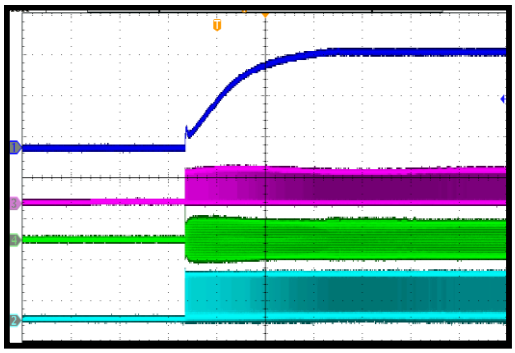


2ms/div.

### Start-Up through $V_{IN}$ at LLC

$P_{OUT}$ = 240W

CH1: $V_{OUT}$ 5V/div.
CH3: $V_{SW}$ 500V/div.
CH4: $I_R$ 5A/div.
CH2: $V_{LSG}$ 10V/div.

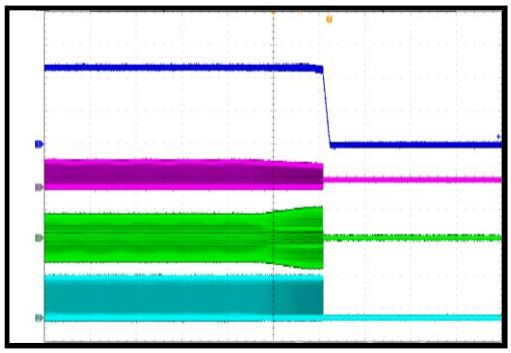


40ms/div.

### Shutdown through $V_{IN}$ at LLC

$P_{OUT}$ = 240W

CH1: $V_{OUT}$ 5V/div.
CH3: $V_{SW}$ 500V/div.
CH4: $I_R$ 5A/div.
CH2: $V_{LSG}$ 10V/div.

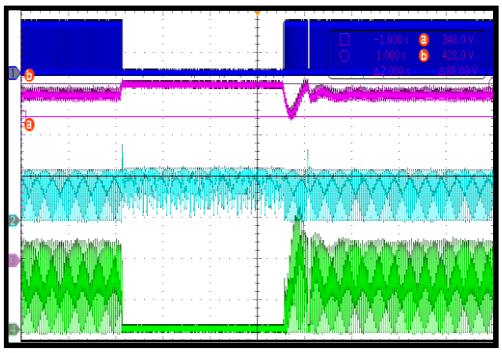


10ms/div.

### Load Dynamic at PFC

$V_{IN}$ = 85$V_{AC}$, $P_{OUT}$ = 0W to 240W, 1A/µs

CH1: $V_{GATEP}$ 10V/div.
CH2: $V_{IN\_REC}$ 100V/div.
CH3: $V_{BUS}$ 100V/div.
CH4: $I_{PFC}$ 5A/div.

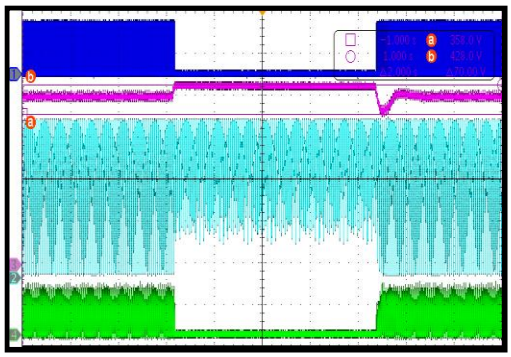


200ms/div.

### Load Dynamic at PFC

$V_{IN}$ = 265$V_{AC}$, $P_{OUT}$ = 0W to 240W, 1A/µs

CH1: $V_{GATEP}$ 10V/div.
CH3: $V_{BUS}$ 100V/div.
CH2: $V_{IN\_REC}$ 100V/div.
CH4: $I_{PFC}$ 5A/div.

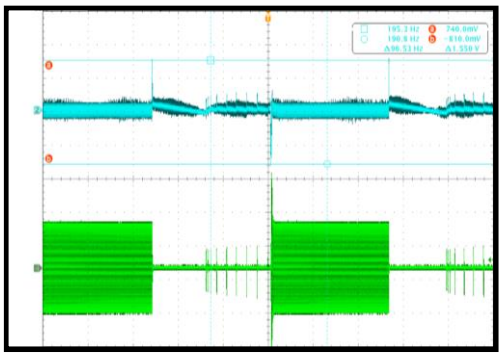


200ms/div.

### Load Dynamic at LLC

$P_{OUT}$ = 0W to 240W, 6A/µs

CH2: $V_{OUT}$/AC Coupled 500mV/div.
CH4: $I_R$ 2A/div.



4ms/div.

# FUNCTIONAL BLOCK DIAGRAM

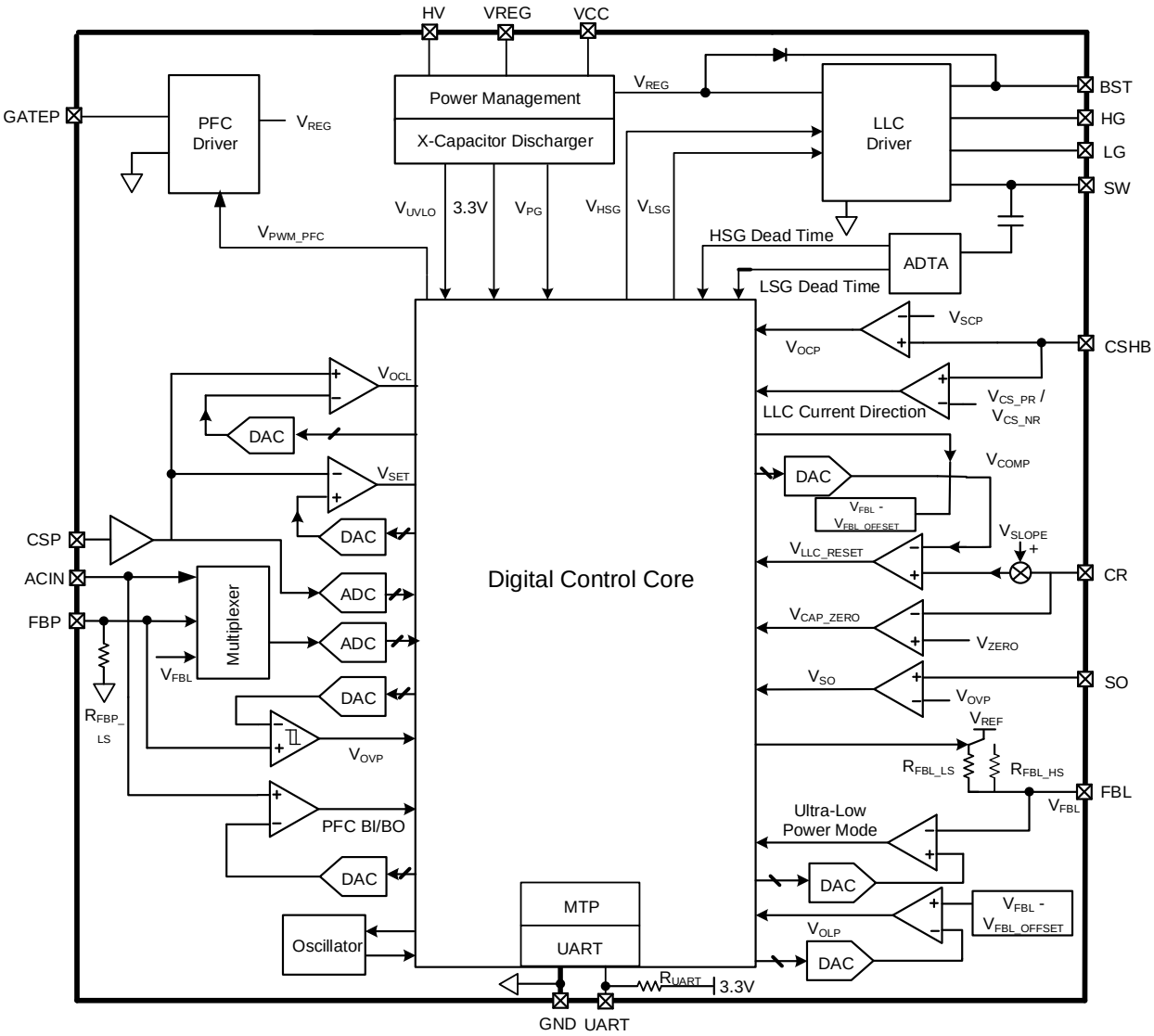



**Figure 1: Functional Block Diagram**

## OPERATION

The HR1215 is a high-performance combo controller that integrates a digital PFC controller and a digital half-bridge LLC controller.

### Multiple-Time Programmable (MTP) Memory and UART Interface Communication

The HR1215 implements a multiple-time programmable (MTP) memory as the non-volatile memory (NVM) for user data storage. The MTP memory is 128bits x 16bits, which can store a maximum 256 bytes of data. The MTP can be erased and rewritten 1,000 times.

If the digital core and the MTP are on, then the HR1215 loads all of the data from the MTP to the corresponding random access memory (RAM) automatically to configure the device's parameters. User data is also written to the MTP via the RAM.

The HR1215 provides a standard UART interface for communication. UART communication is accomplished with the HR1215's dedicated graphic user interface (GUI). The HR1215 and the HR1211 share the same GUI, as the digital controls are identical (see Figure 2).

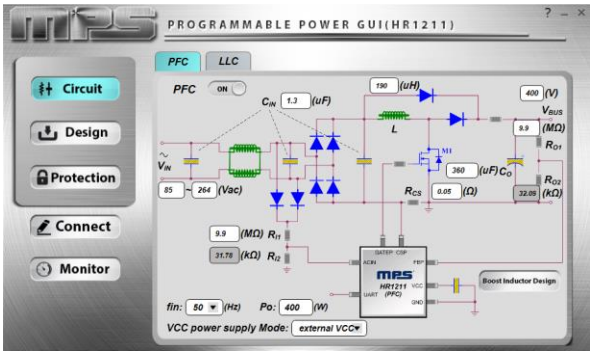



**Figure 2: HR1211 and HR1215 GUI**

The HR1215 can protect the MTP data from accidental reading and writing with a password. Once a non-zero, 16-bit password is written to the password register (address 01h), the MTP enters read-write protection. Data cannot be read or written until the user inputs the correct password into the specific unlock register (address 7Dh). This unlocks the read-write protection status.

### Power Supply Management

Power supply management is provided by the HV, VCC, and VREG pins. Figure 3 shows the IC's power supply block diagram.

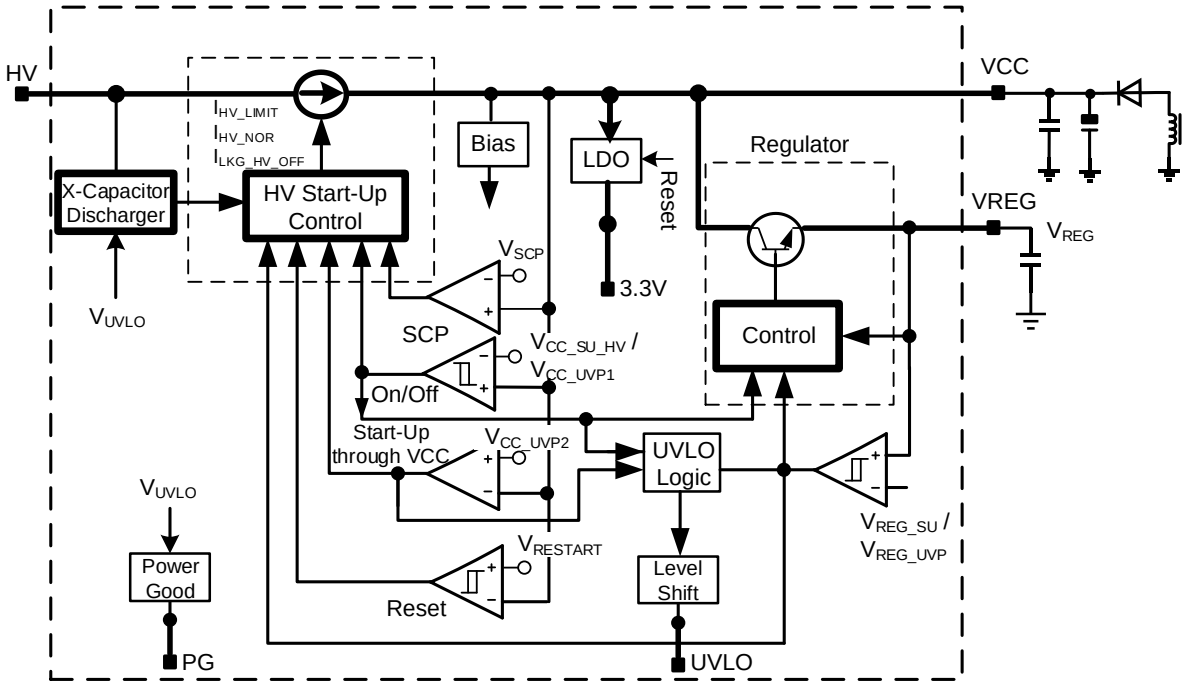



**Figure 3: Power Supply Block Diagram**

Figure 4 shows the power supply operation waveform.

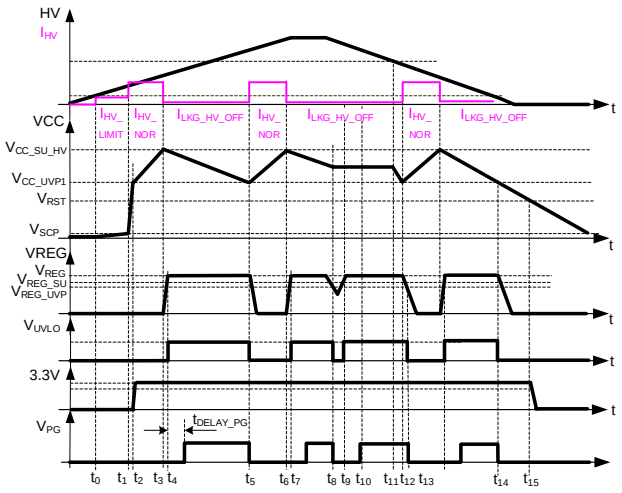



**Figure 4: Power Supply Operation Waveform**

### High-Voltage Start-Up Input (HV)

An internal, high-voltage current source charges VCC while a voltage input is applied to HV. If the VCC voltage ($V_{CC}$) drops below the short-circuit protection threshold ($V_{SCP}$), then the HV charge current ($I_{HV\_NOR}$) is limited to 2.2mA (typically). This prevents excessive power dissipation during start-up caused by a VCC short-circuit condition.

During normal operation, $V_{CC}$ rises to $V_{SCP}$, and the HV current ($I_{HV}$) transitions to its normal operating current ($I_{HV\_NOR}$). The HV current source turns off once $V_{CC}$ reaches the start-up voltage ($V_{CC\_SU\_HV}$). If the current source turns off, then the leakage current ($I_{LKG}$) flowing to HV should be below the $I_{LKG}$ threshold ($I_{LKG\_HV\_OFF}$).

The current source turns on once $V_{CC}$ drops below the under-voltage protection (UVP) threshold ($V_{UVPx}$).

### IC Supply Voltage (VCC)

The VCC pin provides power to all of the internal circuitry, including the VREG pin and the V3.3 internal supply.

VCC can be powered by the half-bridge transformer's auxiliary winding or by an external power supply.

If $V_{CC}$ drops below $V_{UVPx}$, then the IC is disabled and the PFC driver stops switching. The half-bridge LLC continues to operate until the low-side MOSFET (LS-FET) turns on. Then the VREG low-dropout (LDO) regulator is disabled.

There are two VCC UVP thresholds ($V_{UVP1}$ and $V_{UVP2}$, respectively). If the LLC does not start switching, then $V_{UVP2}$ is used. If the LLC starts switching, then $V_{UVP1}$ is used.

If the IC enters latch-off mode, the device remains latched until $V_{CC}$ drops below the IC restart (RST) threshold ($V_{RST}$).

### Regulated Output (VREG)

An internal LDO regulator stabilizes the VREG pin so that it can provide power to the internal PFC driver and the internal half-bridge LLC's LS-FET driver. The VREG voltage ($V_{REG}$) also charges the bootstrap (BST) capacitor ($C_{BST}$), and is used as the reference voltage ($V_{REF}$) for the external circuits.

If $V_{CC}$ exceeds $V_{CC\_SU\_HV}$, then the internal LDO turns on to charge the VREG capacitor ($C_{VREG}$). Once $C_{VREG}$ is charged, the IC starts up. The LDO can only turn on once $V_{CC}$ exceeds $V_{CC\_SU\_HV}$ to ensure that any optional external circuitry connected to VREG does not dissipate additional current before the IC starts up.

Once $V_{REG}$ exceeds its start-up threshold ($V_{REG\_SU}$), the HR1215 starts up and begins normal operation. If $V_{REG}$ drops below its UVP threshold ($V_{REG\_UVP}$), then the IC is disabled and the PFC controller stops switching. The half-bridge LLC controller turns off once the LS-FET gate turns on.

### 3.3V Power Supply (V3.3) for Digital Logic

V3.3 is an internal, stabilized 3.3V power supply for digital circuits. It is derived from VCC via an internal LDO. If $V_{CC}$ exceeds $V_{RESTART}$ plus a hysteresis, then the V3.3 LDO turns on. The V3.3 LDO can be turned off once $V_{CC}$ drops below $V_{RESTART}$.

V3.3 can also be used as the input for an internal 1.8V LDO. This LDO is the power supply for the digital core.

### Internal Under-Voltage Lockout (UVLO) Protection

Both the PFC controller and the LLC controller have an internal under-voltage lockout (UVLO) protection signal. If $V_{CC}$ exceeds $V_{CC\_UVP1}$ and $V_{REG}$ exceeds $V_{REG\_SU}$, then the UVLO signal is pulled high. If $V_{REG}$ drops below $V_{REG\_UVP}$, then

the UVLO signal is pulled low, and UVLO protection is triggered.

### Internal Power Good (PG) Indication

The internal power good (PG) signal indicates to the digital core whether $V_{CC}$ is regulated. If the UVLO signal is pulled high, then the PG signal is pulled high after a delay time ($t_{DELAY\_PG}$) (200µs).

# SYSTEM FUNCTIONS

## X-Capacitor Discharge

The X-capacitors are critical components placed at the power supply input terminals to filter out differential EMI noise. If the AC line is removed, then the energy stored in the X-capacitor can pose risks to the user. Safety standards require that the voltage must be discharged to a safe level within a certain timeframe.

Resistors are typically placed in parallel with the X-capacitor across the AC line to provide a discharge path; however, additional resistors can lead to continuous power consumption while the AC input voltage ($V_{ACIN}$) is connected. This is a significant contributor to the power consumption under no-load or standby conditions.

The HV current source in the HR1215 acts as a smart X-capacitor discharger while $V_{ACIN}$ is removed. Traditional discharge resistors are not required. Figure 5 shows the X-capacitor operating waveform.

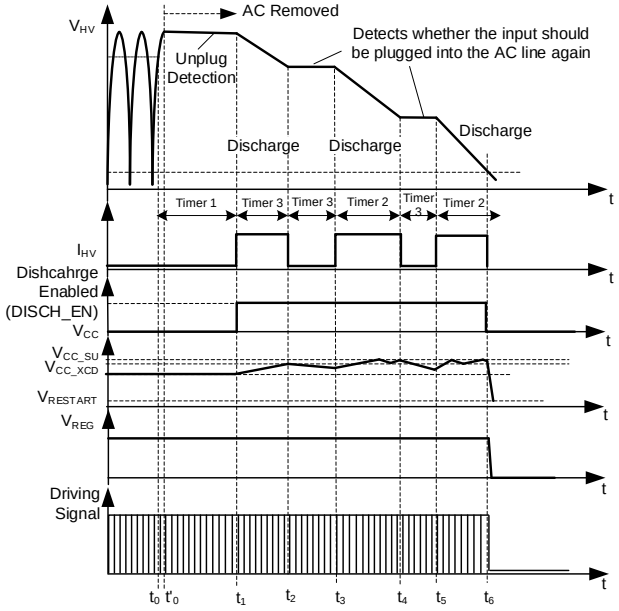



**Figure 5: Operating Waveform of the X-Capacitor Discharger while the AC Line is Removed**

If the AC line is present during normal operation, then the HV current source is off. The HV leakage current ($I_{LKG\_HV}$) is very small, and the power consumption is reduced significantly. Once the AC line is disconnected, a timer (timer 1) begins with a detection time window of 60 x $t_{XCD}$.

Once the timer is finished, the IC controls $I_{HV\_NOR}$ automatically to discharge energy from the X-capacitor to VCC within a time period (30 x $t_{XCD}$) (timer 3).

The IC is stops discharging for an additional timer 3 period to detect the AC. If no AC is detected during this time, then the IC continues to discharge the X-capacitor during the next timer (90 x $t_{XCD}$) (timer 2) until the HV voltage ($V_{HV}$) drops below 35V. Once $V_{HV}$ drops below 35V, $V_{CC}$ is discharged quickly by the internal current source until it drops below $V_{RESTART}$. $V_{RESTART}$ is used to release the latch of the IC if it is in latch-off mode.

If the AC is removed in HV again during the timer 3 period, then the IC starts up (see Figure 6).

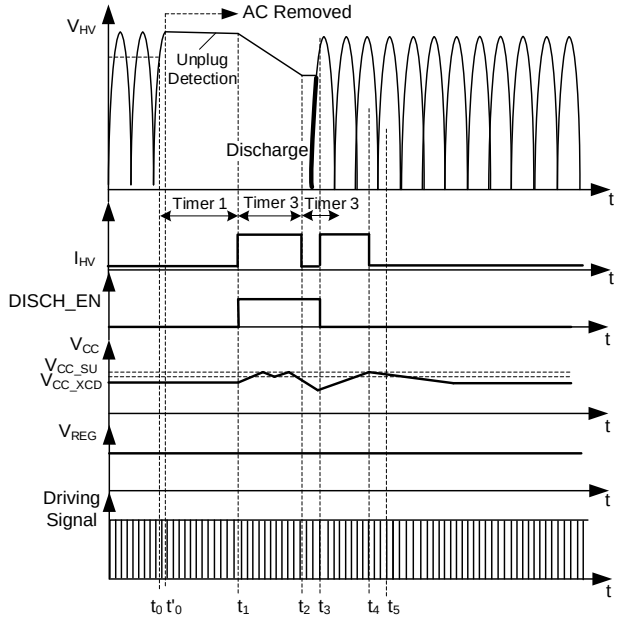



**Figure 6: Operating Waveform of the X-Capacitor Discharger once the AC Line Recovers**

If the X-capacitor discharge function is active, then $V_{CC}$ is regulated between $V_{CC\_SU\_HV}$ and the X-capacitor discharge regulation voltage ($V_{CC\_XCD}$) to avoid overstressing VCC.

The X-capacitor discharge function allows users to choose any X-capacitor value to optimize differential mode EMI filtering. Users can do this without considering the effect of the required bleed resistors on the standby power budget, or under system no-load conditions.

### Over-Temperature Protection (OTP)

If the internal thermal sensor detects that the IC temperature has exceeded the over-temperature protection (OTP) threshold, then the IC stops switching. In OTP mode, the high-voltage current source is disabled. VCC is not charged, and the internal LDOs for VREG and V3.3 are disabled. If the IC temperature drops below the OTP recovery threshold and $V_{CC}$ drops below $V_{RESTART}$, then the IC can start up again once $V_{CC}$ exceeds $V_{CC\_SU\_HV}$.

### IC Enable/Disable Control

The IC can be enabled and disabled for both PFC and LLC operation by configuring the MTP via the GUI.

### Digital PFC Controller

The continuous conduction mode (CCM) and discontinuous conduction mode (DCM) control scheme reduces the RMS current drawn from the AC mains. The control scheme ensures good input current shaping during both CCM and DCM. It reduces the switching frequency ($f_{SW}$) as the load decreased, which achieves higher efficiency and higher power factors under light-load conditions.

### Timing Sequence of the Digital PFC

Figure 7 shows the digital PFC block power supply timing sequence.

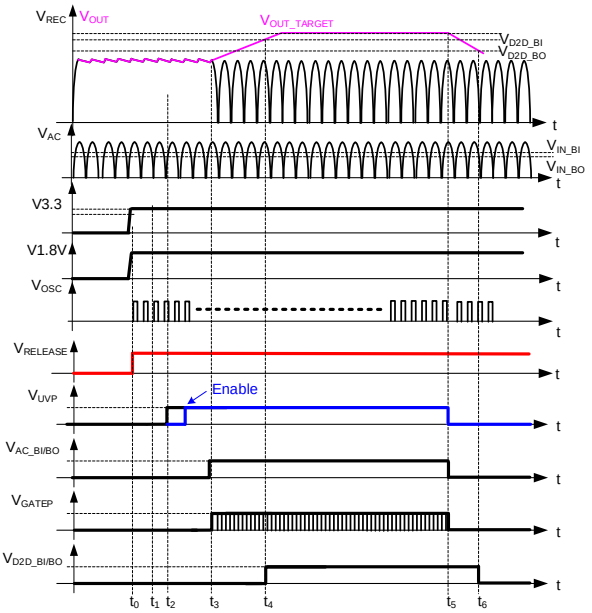



**Figure 7: Digital PFC Block Power Supply Timing Sequence**

### *Internal Power Supply Timing Sequence*

Once $V_{CC}$ exceeds $V_{RESTART}$ plus a hysteresis, the V3.3 LDO turns on and an internal LDO downstream produces a stable 1.8V power supply for the internal digital core and system clocks. Once both 3.3V and 1.8V are stable, the restart (RST) signal goes high. If the UVLO signal is high, the IC enables the oscillator, the analog-to-digital converter (ADC), the digital-to-analog converter (DAC), and the related comparators. The enable (EN) signal is pulled high after the delay time ($t_{DELAY\_SU}$) (20µs), which indicates whether the digital core is ready to start-up.

### *Digital Core Timing*

If both the RST signal and the UVLO signal are high, then the digital system monitors the PG signal within a 150µs detection time window, which determines whether the PFC and the LLC start up via a soft start (SS). If no PG signal is detected, then an SS is initiated; otherwise, an SS is not used for PFC and LLC switching.

After this PG detection time ($t_{DELAY\_PG}$), the digital system starts up. First, the ADC starts sampling $V_{ACIN}$ and $V_{FBP}$. If the AC brown-in condition is met, and there is no open-loop fault on the FBP pin, then the AC brown-in/brownout signal is pulled high and the PFC starts switching until the output voltage ($V_{OUT}$) reaches the preset value. The LLC starts up once the PFC $V_{OUT}$ ($V_{FBP}$) reaches the LLC brown-in threshold.

### *Oscillator*

The system clock frequency for PFC is $f_{OSC1\_NOR}$, and the system clock frequency for LLC is $f_{OSC2\_NOR}$. If the system is in ultra-low power mode (burst mode is off for both the PFC and the LLC), then the PFC clock frequency ($f_{OSC\_PFC}$) and the LLC clock frequency ($f_{OSC\_LLC}$) drop to the burst mode clock frequency ($f_{OSC\_NOPWM}$). Then then pulse-width modulation (PWM) clock frequency ($f_{OSC\_PWM}$) drops to $f_{OSC\_LLC}$ to reduce the IC's power consumption.

### Analog-to-Digital Converter (ADC) Sampling

The HR1215 has two independent ADCs that sample $V_{AC}$, $V_{FBP}$, the LLC feedback voltage ($V_{FBL}$), and PFC peak switching current. The digital PFC controller receives the PFC peak inductor current ($I_{L\_PEAK}$) information from CSP via a 12-bit ADC.

A 3-channel, high-speed analog switch is used to switch between the AC input signal (ACIN), the PFC $V_{OUT}$ signal (FBP), and the LCC feedback signal (FBL) for the other 10 bits of ADC sampling.

Figure 8 shows the ADC module block diagram.

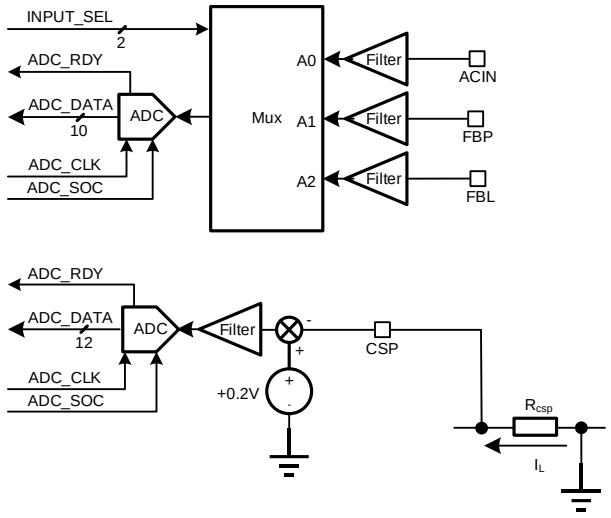



**Figure 8: ADC Block Diagram**

Figure 9 shows the sampling sequence of the 10-bit ADC. The ADC samples ACIN, FBL, and FBP with a fixed frequency, which can be adjusted by setting the idle time in the GUI.

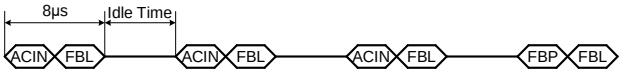



**Figure 9: ADC Sampling Sequence**

$V_{FBL}$ is sampled during each sampling period. $V_{AC}$ is sampled three out of four sampling periods. $V_{FBP}$ is sampled one out of four sampling periods.

### Input Voltage Sensing

The input voltage ($V_{IN}$) is rectified and attenuated via a resistor divider with a fixed ratio (0.0032) before being provided to the ACIN input. The ADC samples $V_{ACIN}$ for the instantaneous value, peak value, and the frequency of $V_{IN}$. This data is used to calculate the on time ($t_{ON}$), to monitor for AC brown-in and brownout protection, and to determine the input capacitor ($C_{IN}$) current compensation.

Figure 10 shows the $V_{IN}$ level for different functions. All of the IC's parameters can be configured via the GUI.

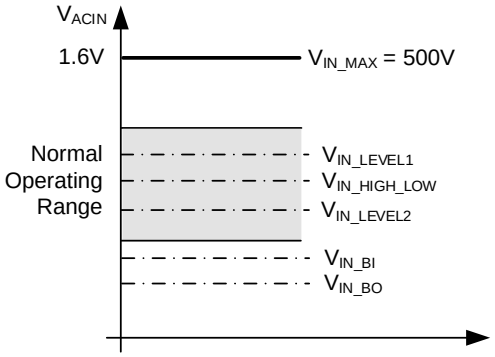



**Figure 10: Input Voltage Level for Different Functions**

### Input Brown-In and Brownout Protection

If the peak $V_{ACIN}$ exceeds the brown-in threshold ($V_{IN\_BI}$) for the brown-in time set by the BI the timer ($t_{BI}$), then the PFC starts switching. If the peak $V_{ACIN}$ drops below the brownout threshold ($V_{IN\_BO}$) for the brownout time set by the BO timer ($t_{BO}$), then the PFC stops switching. Figure 11 shows brown-in and brownout control.

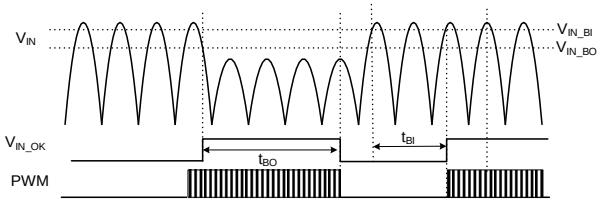



**Figure 11: AC Brown-In and Brownout Control**

### High/Low Line

If $V_{IN}$ drops below $V_{IN\_HIGH\_LOW}$, then the system defines the input as a low-line condition. If $V_{IN}$ exceeds $V_{IN\_HIGH\_LOW}$ plus a hysteresis, then the input is defined as a high-line condition. Both the soft-start time ($t_{SS}$) and the resonant time for PFC valley start-up are implemented independently according to the high-line or low-line input condition. $V_{FBP}$ and PFC over-voltage protection (OVP) can be regulated at different levels according to this high-line or low-line input condition to optimize the PFC stage efficiency.

There are two configurable thresholds for $V_{IN}$: $V_{IN\_LEVEL1}$ and $V_{IN\_LEVEL2}$. Together with $V_{IN\_HIGH\_LOW}$, $V_{IN}$ is divided into four ranges. The input capacitor current ($I_{CIN}$) compensation values can be set to different values at different $V_{IN}$ ranges to improve the power factor.

These three thresholds are comprised of 8 bits of data in the MTP, which can be configured via the GUI.

### Output Voltage Sensing

Similar to $V_{IN}$ sensing, $V_{OUT}$ is also sampled via a resistor divider with a fixed ratio (0.0032) on FBP. $V_{FBP}$ is sampled by the 10-bit ADC. The results are used for $t_{ON}$ calculation, open-loop protection (OLP), and OVP.

The internal pull-down resistor (about 3.3MΩ) should be considered when designing the external resistor divider. The total divider ratio (about 0.0032) can be calculated with Equation (1):

$$\frac{R_{FBL\_LS} // 3.3M\Omega}{R_{FBL\_HS} + R_{FBL\_LS} // 3.3M\Omega} = 0.0032 \quad (1)$$

Where $R_{FBL\_HS}$ is the high-side (HS) external resistor divider, and $R_{FBL\_LS}$ is the low-side (LS) external divider resistor.

Figure 12 shows the $V_{OUT}$ level for different functions.

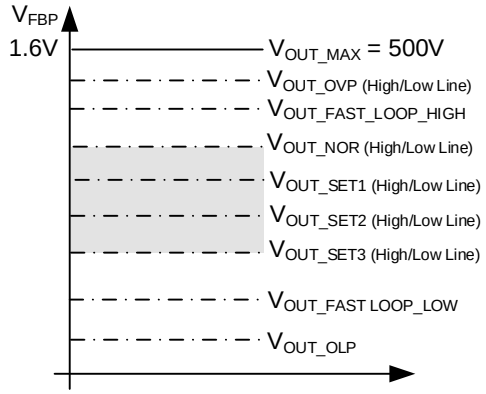



**Figure 12: Output Voltage Level for Different Functions**

### Output Regulation

To optimize efficiency, $V_{OUT}$ can be auto-regulated according to $V_{IN}$ and the output power. $V_{OUT}$ has two different settings according to $V_{IN\_HIGH\_LOW}$, and four different settings according to the power levels. There are a total of eight different setting for PFC output regulation. These settings can be configured via the GUI.

### Output Over-Voltage Protection (OVP)

The output over-voltage protection (OVP) threshold ($V_{OVP}$) can be configured by the MTP register via the GUI. The digital value is converted to an analog signal via a DAC. This value is compared to $V_{FBP}$. If $V_{OUT}$ exceeds $V_{OVP}$, then the PFC stops switching. If $V_{OUT}$ returns to the regulated target voltage ($V_{OUT\_TARGET}$), then the PFC resumes normal operation. Figure 13 shows the internal OVP circuit.

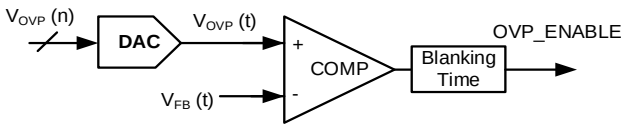



**Figure 13: PFC OVP Circuit**

A blanking time is also inserted during OVP to reduce switching noise interference (see Figure 14). This blanking time can be configured via the GUI.

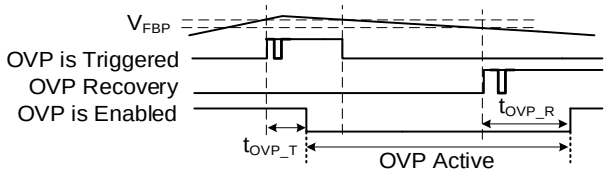



**Figure 14: Output OVP**

### Fast Loop

During a dynamic load event, $V_{FBP}$ may drop or rise significantly due to the low bandwidth of the PFC control loop. $V_{FBP}$ may exceed or drops below its specification. A fast loop can be enabled to improve PFC dynamic performance. The fast loop is active once $V_{OUT}$ drops below the $V_{OUT}$ low-level specification ($V_{OUT\ FAST\_LOOP\_LOW}$) or exceeds the high-level specification ($V_{OUT\_FAST\_LOOP\_HIGH}$). If fast loop is active, then the integral coefficient ($K_I$) and proportional coefficient ($K_P$) switch to the fast loop settings. The fast loop function can be enabled and disabled via the GUI. The fast loop parameters can also be set via the GUI.

### Open-Loop Protection (OLP)

An open-loop condition is defined as $V_{FBP}$ dropping below $V_{OLP}$ for more than a set timer. If an open-loop fault occurs, then the IC enters auto-retry or latch-off mode (selectable via the GUI).

If the IC is in latch-off mode, the switching is latched off. The device can restart once $V_{CC}$ drops below $V_{CC\_RST}$, and then is charged above $V_{CC\_SU\_HV}$.

If the IC is in auto-retry mode, switching is paused for an auto-restart timer that can be set via the GUI. The device restarts once the timer finishes.

If the device is set to self-power mode in the GUI (i.e. the device uses auxiliary winding to power VCC), then $V_{CC}$ must be charged above $V_{CC\_SU\_HV}$ to restart.

### Peak Current Sensing

The PFC inductor current ($I_L$) is sensed by the current-sense resistor (R1), which produces a negative voltage ($V_{CSP}$). This value is converted internally to a positive voltage with a bias ($V_{CS\_S}$) (see Figure 15 and Figure 16). The ADC samples $V_{CS\_S}$ once the PFC gate turns off. $V_{CS\_S}$ can be calculated with Equation (2):

$$V_{CS\_S}(t) = V_{BIAS}(t) - V_{CSP}(t) \quad (2)$$

Figure 15 shows the current-sense circuit on the CSP pin.

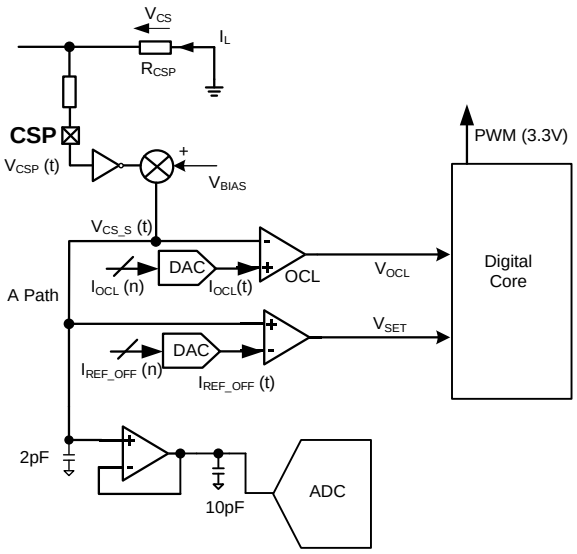



**Figure 15: CSP Pin Current-Sense Circuit**

Figure 16 shows the $V_{CS\_S}$ waveforms.

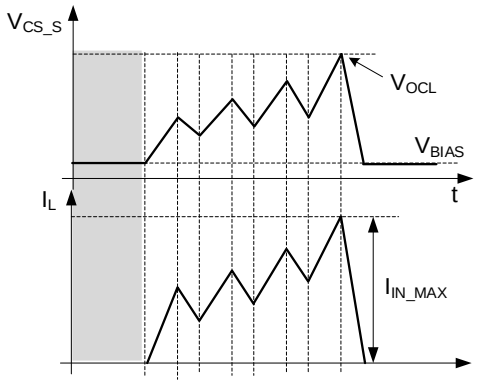



**Figure 16: $V_{CS\_S}$ Waveforms**

### Over-Current Limit (OCL)

The HR1215's cycle-by-cycle over-current limit (OCL) protects the PFC MOSFET from overstress. OCL is implemented by comparing $V_{CS\_S}$ to the internal OCL threshold ($V_{OCL}$). $V_{OCL}$ is an analog signal output from an 8-bit DAC. The internal $V_{OCL}$ can be calculated with Equation (3):

$$V_{OCL} = V_{BIAS} - I_{OCL\_SETTING} \times R1 \quad (3)$$

A leading edge blanking time ($t_{LEB}$) is inserted to reduce switching noise. $V_{OCL}$ can be configured via the GUI.

### Digital PFC Control Scheme

Figure 17 shows the digital control flowchart.

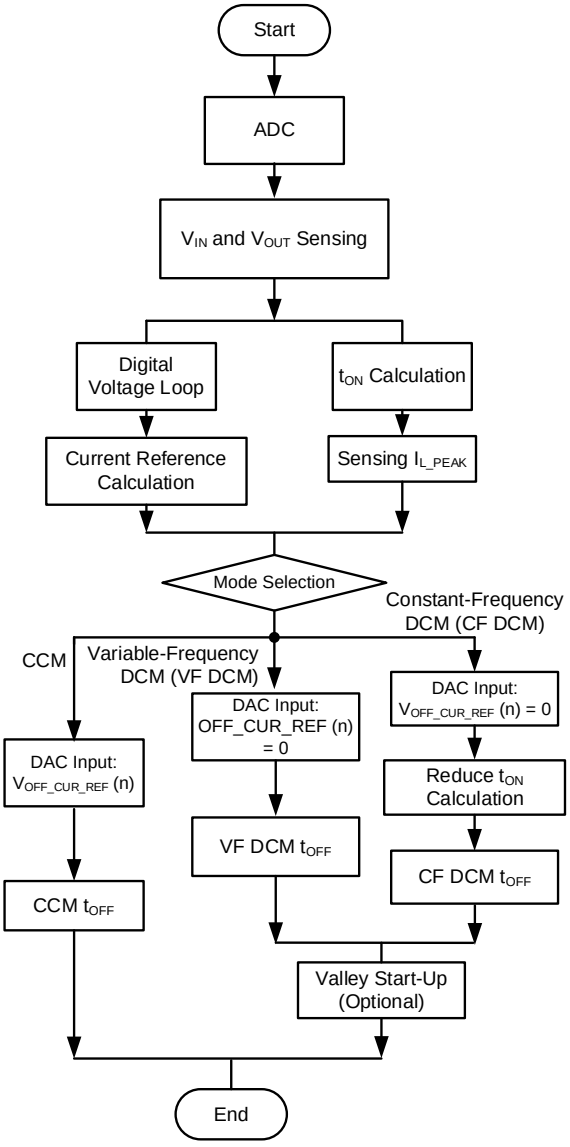



**Figure 17: PFC Control Scheme Flowchart**

### Digital Current Reference

The HR1215 adopts a digital PI that compensates for the voltage control loop. Its output ($V_{COMP}$ (n)) is sent to the multiplier for the current reference calculation (see Figure 18).

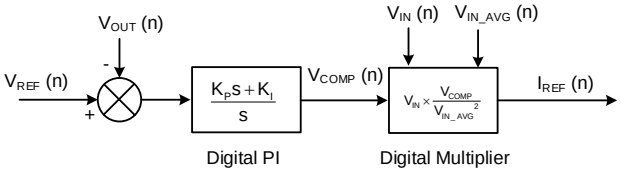



**Figure 18: Current Reference Calculation**

The digital current reference ($I_{REF}$ (n)) can be calculated with Equation (4):

$$I_{REF}(n) = V_{IN}(n) \frac{V_{COMP}(n)}{(0.5 \times V_{IN\_PEAK}(n))^2} \quad (4)$$

### On Time ($t_{ON}$) Calculation

The on time ($t_{ON}$) can be estimated with Equation (5):

$$t_{ON}(n) = \frac{V_{OUT\_REF} - V_{IN}(n)}{V_{OUT\_REF}} \times t_S \quad (5)$$

Where $t_S$ is the switching period that can be configured via the GUI.

### PFC Mode Selection

The HR1215 has three operation modes for the PFC: CCM, variable-frequency DCM (VF DCM), and constant-frequency DCM (CF DCM). The IC sensing current ($I_{PK}$) in CCM can be estimated with Equation (6):

$$I_{PK}(n) < 2I_{REF}(n) \quad (6)$$

$I_{PK}$ in VF DCM can be estimated with Equation (7):

$$2I_{REF}(n) < I_{PK}(n) < 2I_{REF}(n) \times \frac{t_{S\_MAX}}{t_S} \quad (7)$$

Where $t_{S\_MAX}$ is the maximum switching time set via the GUI.

$I_{PK}$ in CF DCM can be estimated with Equation (8):

$$I_{PK}(n) > 2I_{REF}(n) \times \frac{t_{S\_MAX}}{t_S} \quad (8)$$

#### *Continuous Conduction Mode (CCM)*

In CCM, the shutdown current ($I_{SD}$) reference ($V_{ISD\_REF}$ (n)) is calculated and sent to the DAC. There is a digital filter with a configurable cross frequency for off current reference output. The DAC output has an analog signal ($V_{ISD\_REF}$ (t)) that is compared to $V_{CS}$ (t). If $V_{CS}$ (t) drops below $V_{ISD\_REF}$ (t), then the set signal is high. The PWM signal is also set high (see Figure 19).

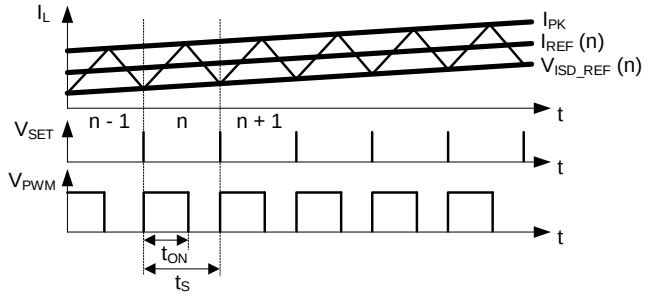



**Figure 19: CCM Control Signals**

$V_{ISD\_REF}$ (n) in CCM can be calculated with Equation (9):

$$V_{ISD\_REF}(n) = 2I_{REF}(n) - I_{PK}(n) \quad (9)$$

#### *Variable-Frequency DCM (VF DCM)*

In VF DCM, the off-current reference is set to 0A. This set signal represents the VF DCM boundary (see Figure 20).

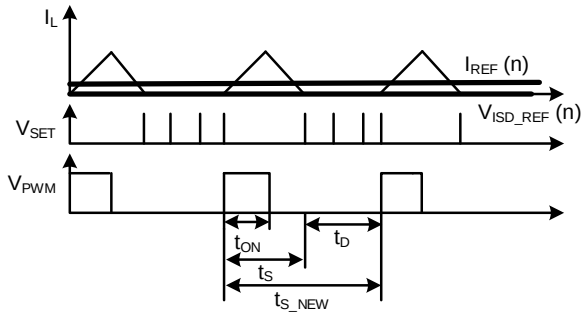



**Figure 20: VF DCM Control Signals**

The new switching period can be estimated with Equation (10):

$$t_{S\_NEW}(n) = \frac{I_{PK}(n)}{2I_{REF}(n)} \times t_S \quad (10)$$

The delay time ($t_{DELAY}$ (n)) can be calculated with Equation (11):

$$t_{DELAY}(n) = t_{S\_NEW}(n) - t_S = \left( \frac{I_{PK}(n)}{2I_{REF}(n)} - 1 \right) \times t_S \quad (11)$$

The calculated delay time has a digital filter with a configurable cross-frequency.

### *Constant-Frequency DCM (CF DCM)*

In CF DCM, the off-current reference is set to 0A.

In this mode, the switching frequency ($f_{SW}$) is limited to the minimum $f_{SW}$ ($f_{SW\_MIN}$), which can be set via the GUI. The PWM duty is modulated to achieve average current control.

Figure 21 shows the CF DCM control signals.

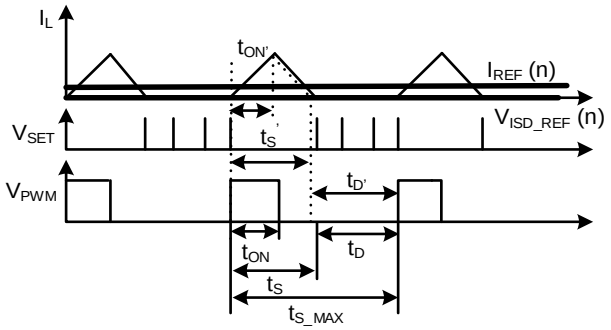



**Figure 21: CF DCM Control Signals**

The new switching period ($t_S'$) can be calculated with Equation (12):

$$t_S'(n) = \frac{I_{REF}(n) \times t_{S\_MAX}}{\frac{1}{2} I_{PK}'(n)} \quad (12)$$

As $t_{ON}$ changes, $I_{L\_PEAK}$ (t) remains relatively unchanged. $I_{L\_PEAK}'$ (t) can be estimated with Equation (13):

$$I_{L\_PEAK}'(t) = I_{L\_PEAK}(t) \quad (13)$$

The switching period ($t_S'$ (n)) can be calculated with Equation (14):

$$t_S'(n) = \frac{2 I_{REF}(n)}{I_{L\_PEAK}(n)} \times t_{S\_MAX} \quad (14)$$

The new on time ($t_{ON}'$ (n)) can be estimated with Equation (15):

$$t_{ON}'(n) = \frac{V_{OUT\_REF} - V_{IN}(n)}{V_{OUT\_REF}} \times t_S'(n) \quad (15)$$

The delay time ($t_{DELAY}'$ (n)) can be calculated with Equation (16):

$$t_D'(n) = t_{S\_MAX} - t_S'(n) = \left(1 - \frac{2 I_{REF}(n)}{I_{PK}(n)}\right) \times t_{S\_MAX} \quad (16)$$

$t_{DELAY}'$ (n) also has a digital filter with a configurable cross-frequency.

### Soft Start (SS)

Once AC brown-in protection is triggered, the VIN_OK signal is pulled high and the HR1215 initiates an SS (see Figure 22).

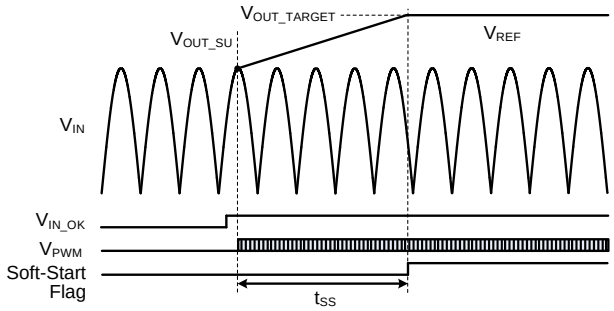



**Figure 22: Soft Start**

During an SS, the internal reference voltage ($V_{REF}$) ramps up slowly until it reaches $V_{OUT\_TARGET}$. The ramp's slew rate is determined by the $t_{SS}$ high and low lines, which can be configured via the GUI. If $V_{REF}$ reaches $V_{OUT\_TARGET}$, then the soft-start flag (SOFT_START_FLAG) is set high and SS is complete. Typically, $V_{OUT}$ cannot rise during $t_{SS}$, so $V_{OUT}$ is regulated after SS is complete.

Note that the slew rate is different for the high line and the low line.

### Burst Mode

At light loads, the IC is designed to operate in burst mode for increased efficiency and for decreased no-load power consumption. Once the output load drops below the threshold (a percentage of the rated load), the PFC enters burst mode. The threshold can be configured via the GUI for both the high line and the low line.

In burst mode, the switching duty is calculated according to the set threshold, and the output is regulated to $V_{OUT\_TARGET}$ with a 5V hysteresis. The PFC stops switching once $V_{OUT}$ reaches $V_{OUT\_TARGET}$ + 5V. It resumes switching once $V_{OUT}$ drops below $V_{OUT\_TARGET}$.

The HR1215 is designed to exit burst mode at the peak point of the AC line to minimize current stress. A threshold voltage can be selected via the GUI to prevent the bus voltage ($V_{BUS}$) from dropping too low under transient. If $V_{BUS}$ drops below the threshold, the IC exits burst mode without waiting for peak point detection.

### Power Factor Compensation (PFC)

Traditional power factor compensation (PFC) control schemes only regulate the inductor current ($I_L$) to match $V_{IN}$; however, $I_{CIN}$ is not controlled. This can cause the power factor (PF) deterioration, and a sub-optimal phase delay. With a larger capacitor or a higher $V_{IN}$, the PF worsens (especially under light-load conditions).

To improve the PF, the HR1215 implements a patented method to compensate $I_{CIN}$. There are four $V_{IN}$ ranges and four input capacitors for the compensation setting, which can be configured via the GUI and stored in the MTP. This function improves the PF across the entire $V_{IN}$ range.

### Frequency Jittering

The HR1215 implements a frequency jittering function that reduces EMI noise. If frequency jittering is enabled, then $f_{SW}$ is modulated via a triangular waveform with a modulation frequency ($f_M$). This frequency is modulated to the maximum value at the peak of the triangle, and to the minimum value at the valley of the triangle. Figure 23 shows the frequency jittering modulation. The modulation amplitude and $f_M$ can be configured via the GUI.

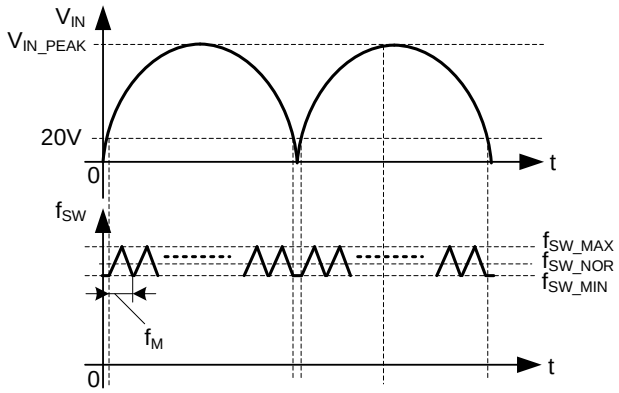



**Figure 23: Frequency Jittering Modulation**

### Digital LLC Controller

#### *LLC Brown-In and Brownout Protection*

The LLC starts to work when the bus voltage exceeds the brown-in threshold. The LLC shuts down when the bus voltage drops below the brownout threshold. There is a configurable timer delay set via the GUI for both brown-in and brownout LLC switching.

#### *Soft Start (SS)*

During LLC SS, the internal $V_{COMP}$ is overridden by a soft-start generator output voltage. The soft-start timer can be set via the GUI to define the soft-start duration.

Once an SS is initiated, the low-side gate (LSG) turns on for a configurable time to charge the $C_{BST}$. Then the high-side gate (HSG) and the LSG turn on and off alternately.

Because of resonant capacitor ($C_R$) voltage imbalance during start-up, the current slew rate in the resonant tank is different between the HSG and LSG turn-on periods.

The HR1215's LSG driver does not turn off until the resonant tank current drops below zero ($V_{CSHB} < V_{CSNR}$) to avoid hard switching during SS (see Figure 24).

If both the HSG and LSG are driven with a 50% duty cycle, the resonant tank current may not reverse in a switching half-cycle, which can lead to hard switching.

Figure 24 shows the waveform difference between a 50% duty cycle and the HR1215's logic.

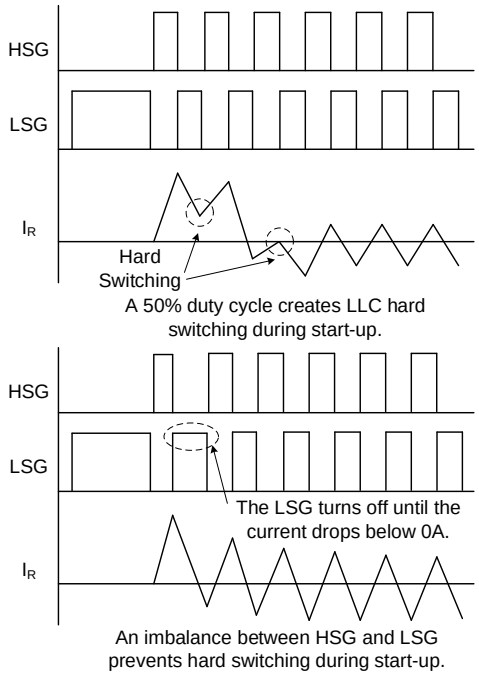



**Figure 24: LLC Start-Up to Avoid Hard Switching**

#### *Current Mode Control*

The on-time comparator determines the HSG $t_{ON}$ by comparing the voltage derived from the current sense (CR) with $V_{COMP}$. $V_{COMP}$ is generated from $V_{FBL}$ on an optocoupler.

The LSG follows the HSG $t_{ON}$. A digital counter with a minimum step (about 1 / $f_{OSC1\_NOR}$) is implemented to ensure that $t_{ON}$ between HSG and LSG matches. Figure 25 shows the current mode control block diagram of the half-bridge LLC.

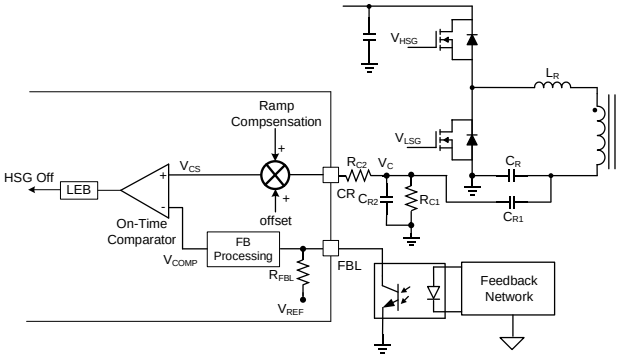



**Figure 25: LLC Current Mode Control Block Diagram**

Figure 26 shows the LLC current mode control waveform.

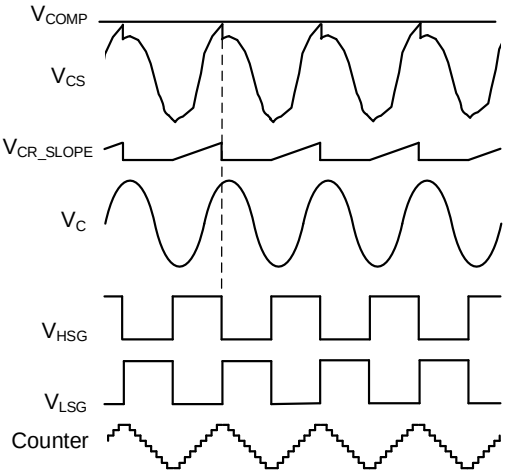



**Figure 26: LLC Current Mode Control Waveform**

The current-sense voltage ($V_C$) is proportional to the voltage on the resonant tank capacitor ($C_R$). The proportion is determined by the external capacitor divider ($C_{R1}$ + $C_{R2}$). Set the capacitor dividing ratio to ensure that the maximum output power (primary current) of the LLC stage can be delivered.

To prevent subharmonic oscillation, a configurable, 4-bit digital slope compensation can be added. The compensation voltage ($V_{CR\_SLOPE}$) is the product of the slope and $t_{ON}$. This value is added to the sensed voltage ($V_C$) to generate $V_{CS}$.

The HR1215 senses the optocoupler voltage on FBL, which generates the internal on-time comparator voltage ($V_{COMP}$). The LSG follows the previous HSG $t_{ON}$; however, the LSG does not turn off until $V_{CS}$ drops below $V_{COMP}$. There is an internal pull-up resistor ($R_{FBL}$), $V_{FBL}$ increases as the output load increases. The sensed $V_{FBL}$ is also used for skip mode detection, burst mode detection, and over-power protection (OPP).

### *Operation Mode*

The LLC can operate in three modes: continuous mode, skip mode, and burst mode. The controller samples the $V_{FBL}$ via the 10-bit ADC to determine which operation mode (see Figure 27).

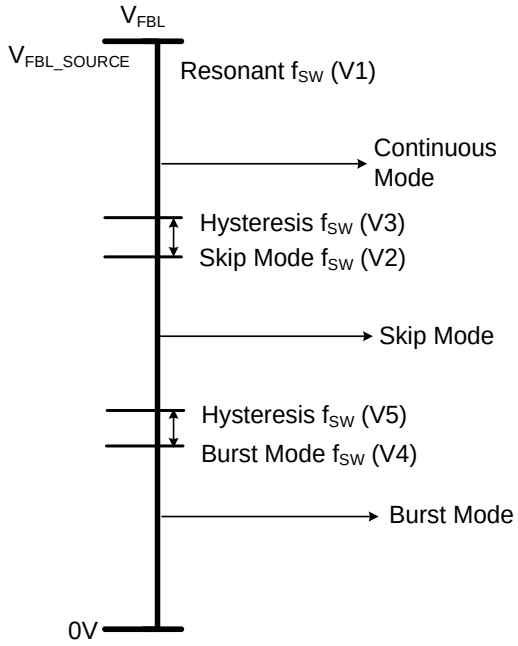



**Figure 27: LLC Operation Mode Determined by FBL**

If $V_{FBL}$ exceeds the skip mode entry threshold (V2), then the LLC system enters skip mode. If $V_{FBL}$ drops below the burst mode entry threshold (V4), then the LLC enters burst mode. Both the skip mode and burst mode thresholds have exit levels with a hysteresis (V3 and V5). If the LLC exceeds V3 in skip mode, then it enters continuous mode. If the LLC exceeds V5 in burst mode, then it enters skip mode. V2, V3, V4, and V5 can be configured via the GUI.

In skip mode and burst mode, $V_{COMP}$ can be calculated with Equation (17):

$$V_{COMP} = A_X \times V_{FBL} + B_X \quad (17)$$

Where $A_X$ is the proportional coefficient, and $B_X$ is an offset for $V_{COMP}$. $A_X$ and $B_X$ can be set via the GUI.

In continuous mode, $V_{COMP}$ can be estimated with Equation (18):

$$V_{COMP} = V_{FBL} - V_{FBLOFFSET} \quad (18)$$

Figure 28 shows the $V_{COMP}$ generation block diagram.

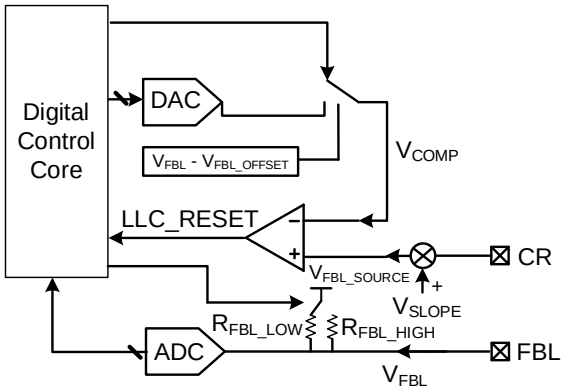



**Figure 28: $V_{COMP}$ Generation Block Diagram**

### *Skip Mode*

For the half-bridge LLC topology frequency control, $f_{SW}$ increases as the load decreases. This means that the magnetization losses and switching losses increase under light-load conditions. To reduce power consumption while keeping the output under regulation, the HR1215 implements skip mode to reduce the average $f_{SW}$, which reduces the magnetic loss.

In skip mode, an idle time ($t_{SKIP}$) is inserted between every N switching cycle. N is configurable via the GUI. $t_{SKIP}$ is kept at the configured value for stability. The first HSG after the idle time turns on at the zero-voltage switching (ZVS) point to minimize the switching losses (see Figure 29).

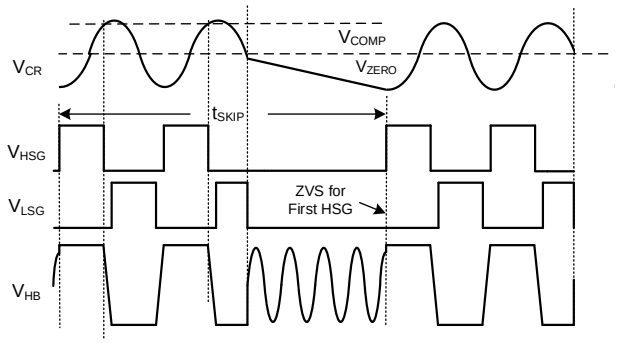



**Figure 29: LLC Skip Mode**

The switching frequencies for HSG and LSG follows the current mode control scheme, except for the last LSG $t_{ON}$ during a skip cycle. This LSG ends once $V_{CR}$ drops to $V_{ZERO}$.

### *Burst Mode*

To further limit the average $f_{SW}$ as the load decreases, a longer $t_{SKIP}$ is inserted in skip mode. This is called burst mode (see Figure 30).

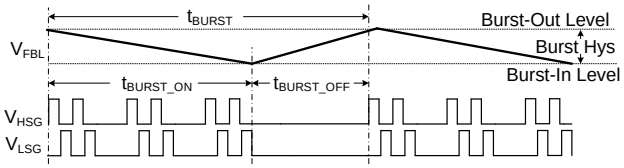



**Figure 30: LLC Burst Mode**

During the burst on period ($t_{BURST\_ON}$), the LLC operates in skip mode. During the burst off period ($t_{BURST\_OFF}$), the LLC stops switching. If $V_{FBL}$ exceeds the configurable burst-out threshold, then $t_{BURST\_OFF}$ ends and the LLC starts switching.

To minimize the audible noise created during burst mode, users can activate burst frequency control function via the GUI. This function allows users to limit the burst frequency ($f_{BURST}$) to a low value. The burst frequency (1 / $t_{BURST}$) can be adjusted to a preset range by increasing or decreasing the switching pulses during $t_{BURST\_ON}$.

The HR1215 has a switchable pull-up resistor on FBL to reduce the optocoupler current in deep burst mode. If the switching counts during one $t_{BURST\_ON}$ is below the set value (indicating that the load is light enough), then the HR1215 switches the FBL pull-up resistor from $R_{FBL\_LOW}$ to $R_{FBL\_HIGH}$ gradually.

The HR1215 features an ultra-low power mode. The IC enters ultra-low power mode once both the PFC and LLC are in burst off mode. The device can also operate in ultra-low power mode if the PFC is in burst off mode and $V_{FBL}$ is below the ultra-low power mode entry threshold ($V_{ULTRA-LOW}$).

In ultra-low power mode, IC power consumption is reduced by shutting down some of the internal circuitry. This is implemented via an internal logic comparator that compares $V_{FBL}$ to a configurable reference from the 8-bit DAC.

If $C_{BST}$ is deeply discharged during burst off mode, then the LSG turns on for a configurable time period ($t_{HSG\_INI}$). $t_{BURST\_OFF}$ can exceed the timer set via the GUI to charge $C_{BST}$.

### *Burst Frequency Control*

The HR1215 incorporates $f_{BURST}$ control to reduce the acoustic noise during burst mode. Typically, the acoustic noise is reduced while $f_{BURST}$ is low. $f_{BURST}$ control increases the switching counts in each burst cycle, so that $t_{BURST\_OFF}$ is extended. This reduces the overall $f_{BURST}$.

If $f_{BURST}$ drops below the set target frequency, then the device operates at the normal burst level. To increase the switching counts once $f_{BURST}$ exceeds the target voltage, the normal burst level is ignored until the switching count exceeds the internal calculation result, or until $V_{FBL}$ drops below $V_{ULTRA-LOW}$.

If the device drops below $V_{ULTRA-LOW}$, the then IC stops switching. This prevents $V_{OUT}$ from overshooting under light- to heavy-load transients; however, this may lead to a higher $f_{BURST}$. Make the difference between the burst level and $V_{ULTRA-LOW}$ as large as possible to increase the $V_{FBL}$ range in burst mode.

Figure 31 shows $f_{BURST}$ control waveforms.

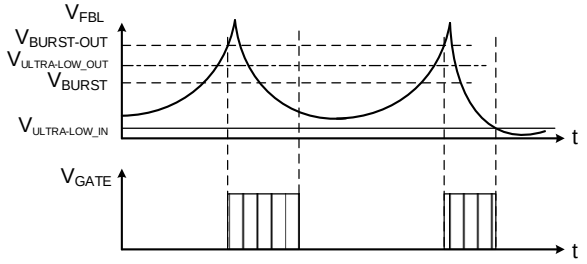



**Figure 31: Burst Frequency Control Waveforms**

### *Adaptive Dead Time Adjustment (ADTA)*

A dead time (DT) between the HS-FET gate driver and the LF-SET gate driver is required in half-bridge topologies to prevent cross-conduction through the power stage MOSFETs. This prevents excess current, reduces high EMI noise, and prevents damage to the IC. Traditional fixed DT control schemes are widely used in resonant converters due to their simple implementation; however, fixed DT control schemes can lead to hard switching at light loads or large $L_M$ design conditions. This can cause thermal issues and reliability issues.

The HR1215 incorporates an intelligent adaptive dead time adjustment (ADTA) logic circuit that is capable of detecting the SW dV/dt via an internal high-voltage capacitor. This capacitor inserts the proper DT automatically according to the converter's operating conditions. Figure 32 shows the simplified ADTA block diagram.

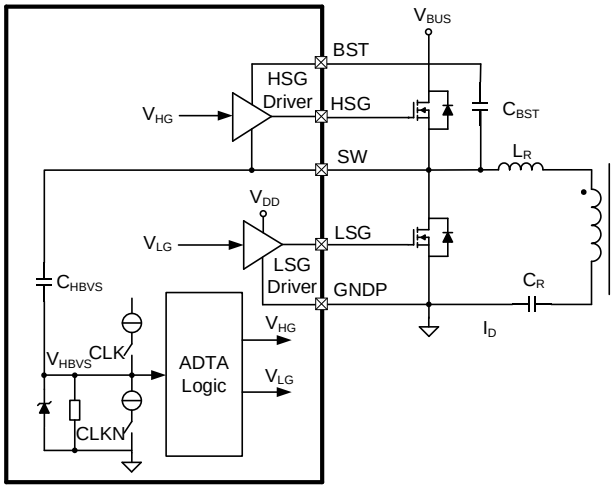



**Figure 32: ADTA Block Diagram**

Once the HSG switches off, SW is driven from a high voltage to a low voltage via the resonant tank current ($I_R$). A negative dV/dt draws a current from the half-bridge voltage sense (HBVS) capacitor ($C_{HBVS}$), which pulls the HBVS voltage ($V_{HBVS}$) down. If the current exceeds the internal bias current, then $V_{HBVS}$ is pulled down and clamped at 0V.

If the SW slew rate decreases, then the current decreases and $V_{HBVS}$ ramp ups. This change in $V_{HBVS}$ is used for DT detection, so that the LSG switches on after a delay.

The DT is defined as the time between when the HSG tuns off and when the LSG turns on. This relies on the completion of SW's transition. If the LSG turns off, then SW transitions from low to high, creating an input current from $C_{HBVS}$. The DT is automatically adjusted using the opposite process of HSG switching off.

Note that there are three possible dead times: a minimum DT ($t_{DT\_MIN}$), a maximum DT ($t_{DT\_MAX}$), and an adaptive DT. The adaptive DT is between $t_{DT\_MIN}$ and $t_{DT\_MAX}$. If the SW transition time is shorter than $t_{DT\_MIN}$, then the next HSG or LSG

should not turn on until the DT exceeds $t_{DT\_MIN}$. This prevents shoot-through between the high-side and low-side MOSFETs. A DT that is too long may cause duty cycle losses and soft switching losses. An SW transition time that is too long may cause an extended DT; therefore, $t_{DT\_MAX}$ is set to force the gate to turn on under these conditions. Both $t_{DT\_MIN}$ and $t_{DT\_MAX}$ can be configured via the GUI.

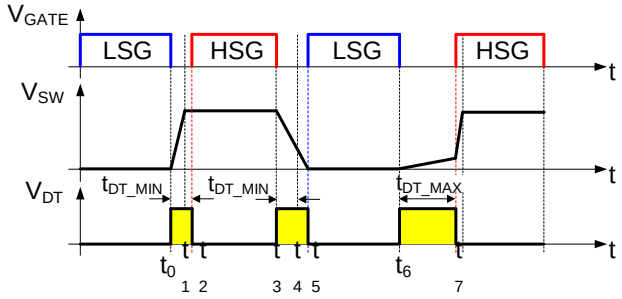



**Figure 33: Minimum, Maximum, and Adaptive Dead Time**

Figure 34 shows the ADTA operation waveform.

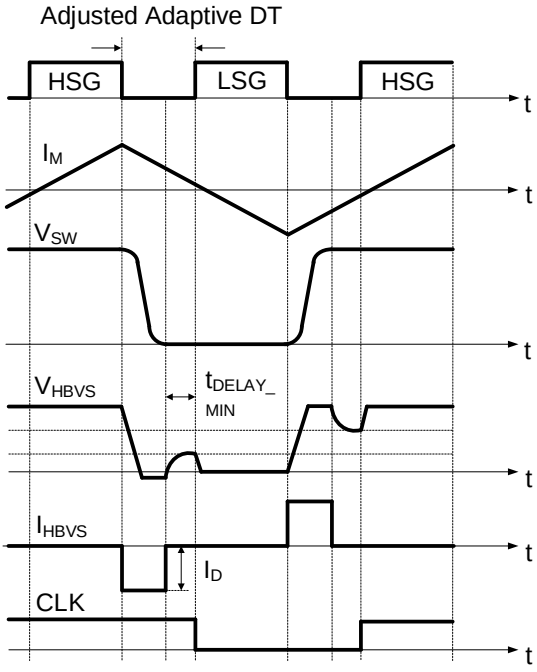



**Figure 34: ADTA Operation Waveform**

### *Capacitive Mode Protection (CMP)*

If a fault occurs (e.g. an overload fault, a short circuit, or a load transient condition), the LLC converter may operate in capacitive mode. In capacitive mode, the voltage applied on the resonant tank lags behind the current, which makes the MOSFETs lose their ZVS capability. It is recommended to avoid capacitive mode, as it can damage the device.

Figure 35 shows the principles of capacitive mode protection (CMP).

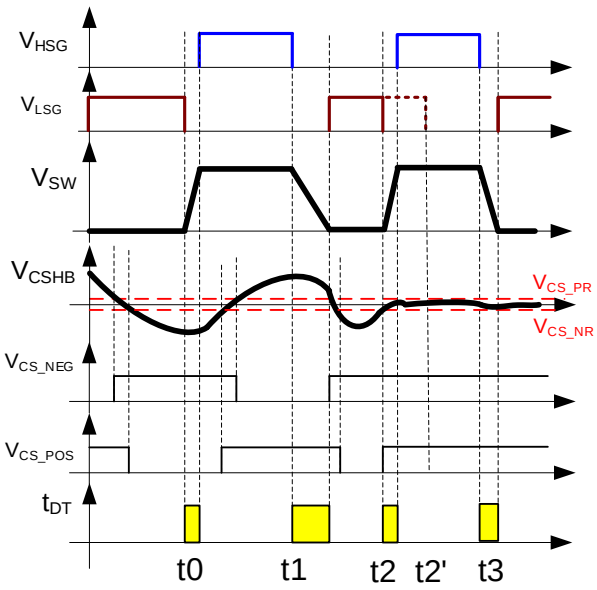



**Figure 35: Operating Principles of CMP**

$V_{CS\_POS}$ and $V_{CS\_NEG}$ are the current polarity flags, which are generated by comparing the voltage on the CSHB pin ($V_{CSHB}$) with internal $V_{CS\_PR}$ and $V_{CS\_NR}$ thresholds.

At t0, the converter operates in inductive mode. $V_{CS\_NR}$ exceeds $V_{CSHB}$ once the LSG driver turns off. This indicates that the current is flowing at the correct polarity (negative). CMP is not triggered.

At t1, the converter operates in inductive mode. $V_{CSHB}$ exceeds $V_{CS\_PR}$ once the HSG driver turns off. This also indicates that the current is flowing at the correct polarity (positive). CMP is not triggered.

At t2, the LLC converter operates in capacitive mode, and $V_{CSHB}$ exceeds $V_{CS\_NR}$. The LSG is forced off in order to avoid operating in capacitive mode. If CMP is not enabled, then theLSG does not turn off until t2.

If $V_{CSHB}$ never exceeds $V_{CS\_PR}$ while the HSG is on, then CMP is not triggered when the HSG turns off. If $V_{CSHB}$ never drops below $V_{CS\_NR}$ while the LSG is on, then CMP is not triggered when the LSG turns off.

### *Over-Current Protection (OCP)*

The HR1215 provides over-current protection (OCP) once $V_{CSHB}$ exceeds $V_{OCP}$. An internal counter begins each time $V_{OCP}$ is exceeded. OCP is triggered once the counter reaches its set value (configured via the GUI). OCP is typically triggered when $V_{CSHB}$ continues to rise during a short circuit (see Figure 36).

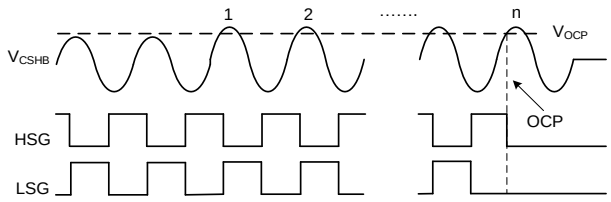



**Figure 36: OCP Timing Sequence**

The IC can be set for latch-off or auto-retry mode if LLC OCP occurs. The GUI can be used to select the protection mode.

For details on the latch-off and auto-retry protection modes, see the Open-Loop Protection section.

### *Over-Power Protection (OPP)*

Over-power protection (OPP) protects the LLC converter from excessive over-power conditions.

If $V_{FBL}$ exceeds $V_{OPP\_LLC}$ (configurable via the GUI), an internal configurable timer turns on. This timer is reset once $V_{FBL}$ falls below $V_{OPP\_LLC}$. OPP is triggered if the timer counts to the end without resetting. $V_{OPP\_LLC}$ should not exceed the minimum value of $V_{FBL\_SOURCE}$.

OPP can activate latch-off mode or auto-retry mode. This parameter is configured via the GUI.

For details on the latch-off and auto-retry protection modes, see the Open-Loop Protection section.

# APPLICATION INFORMATION

### Current Sensing (CSHB)

Both CMP and OCP detect the current signal on the CSHB pin; therefore, a proper current-sense circuit should be designed on CSHB.

There are two kinds of current-sense circuits. The first is a lossless current-sense circuit that sensed the current via a small capacitor in parallel with the resonant capacitor. The second is a current-sense circuit that senses the resonant tank current directly via a series-sensing resistor. Lossless current sensing is typically recommended for most applications (see Figure 37).

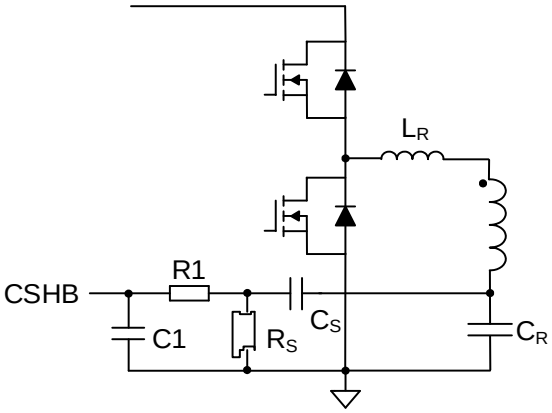



**Figure 37: Lossless Current-Sense Network**

To design the lossless current-sense network, follow the equations listed below:

The current-sense capacitor ($C_S$) can be calculated with Equation (19):

$$C_S \le \frac{C_R}{100} \quad (19)$$

To avoid triggering the capacitive detection threshold accidentally (for $V_{CS\_PR}$ or $V_{CS\_NR}$) during light-load operation, the current-sense resistor ($R_S$) should fulfill the following condition, which can be estimated with Equation (20):

$$R_S > \frac{V_{CSPR}}{I_M} \times (1 + \frac{C_R}{C_S}) \quad (20)$$

Where $I_M$ is the peak magnetizing current.

$I_M$ can be calculated with Equation (21):

$$I_M = \frac{V_{BUS}}{8L_M \times f_{MAX}} \quad (21)$$

Where $V_{BUS}$ is the LLC $V_{IN}$, $L_M$ is the transformer winding inductance, and $f_{MAX}$ is the maximum $f_{SW}$.

$R_S$ should also meet the following condition, which can be estimated with Equation (22):

$$R_S < \frac{V_{OCP}}{I_{CR\_PK}} \times (1 + \frac{C_R}{C_S}) \quad (22)$$

Where $I_{CR\_PK}$ is the peak current of the resonant tank at low $V_{IN}$ and full loads.

$I_{CR\_PK}$ can be calculated with Equation (23):

$$I_{CR\_PK} = \sqrt{\left(\frac{N \times V_{OUT}}{4L_M \times f_{SW}}\right)^2 + \left(\frac{I_{OUT} \times \pi}{2N}\right)^2} \quad (23)$$

Where N is the turn ratio of the transformer, and $L_M$ is the magnetizing inductance.

The R1 and C1 network reduces the switching noise on CSHB.

The current-sense resistor circuit uses a current-sense resistor ($R_S$) placed in series with the resonant tank (see Figure 38). This method is simpler, and requires fewer external components; however, it can cause excessive power consumption on $R_S$.

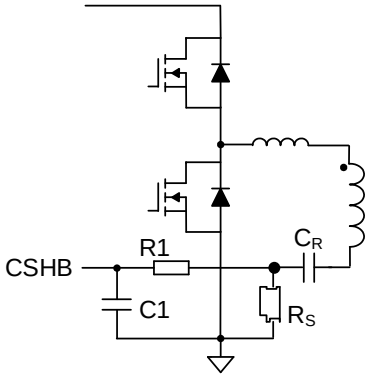



**Figure 38: Current-Sense Circuit with a Sense Resistor**

$R_S$ can be calculated with Equation (24):

$$R_S < \frac{V_{OCP}}{I_{CR\_PK}} \quad (24)$$

### High-Side Gate Driver (HSG)

An external bootstrap (BST) capacitor ($C_{BST}$) is required to provide energy to the HSG. An integrated BST diode charges this capacitor via

the VREG pin. This diode simplifies the external driving circuit for the HS-FET, and allows $C_{BST}$ to be charged while the LS-FET is on.

Choose $C_{BST}$ to be between 100nF and 470nF to ensure enough gate driver energy.

Figure 39 shows the HSG driver circuit.

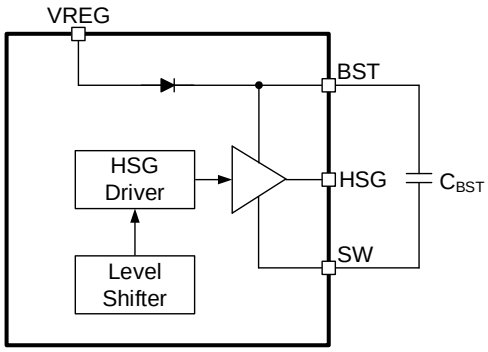



**Figure 39: HSG Driver Circuit**

### External Protections (SO)

The HR1215 monitors the SO pin voltage ($V_{SO}$) and provides a protection function if $V_{SO}$ exceeds $V_{OVP}$ for a set timer ($t_{OVP\_STABLE}$).

Connect SO to the primary auxiliary winding via a resistor divider to sense $V_{OUT}$. $V_{OUT}$ is used to determine whether OVP is triggered. $V_{SO}$ can be calculated with Equation (25):

$$V_{SO} = \frac{R_{SO1}}{R_{SO1}+R_{SO2}} \times \frac{N_{PAU}}{N_S} \times (V_O + V_{FWD}) \quad (25)$$

Where $N_{PAU}$ is the turns of the auxiliary winding, $N_S$ is the turns of the secondary winding, $V_{FWD}$ is the forward voltage drop of the output rectifier or synchronous rectifier, and $R_{SO1}$ + $R_{SO2}$ is the voltage divider for sampling.

The secondary-side OVP has an optocoupler, and is simple and accurate. If the optocoupler turns on, then $V_{SO}$ exceeds $V_{OVP}$ and OVP is triggered. $V_{SO}$ can be calculated with Equation (26):

$$V_{SO} = \frac{R_{SO1}}{R_{SO1}+R_{SO2}} \times (V_{REG} - V_{OPTO}) \quad (26)$$

An external NTC can also be used on SO for external over-temperature protection (OTP). Pull the SO pin up to a constant voltage source (e.g. VREG) via an NTC resistor. Then $V_{SO}$ can be

Where $R_{SO}$ is the external pull-down resistor connected between the SO and GND pins.

Figure 40 shows the SO application circuits for OVP and external OTP.

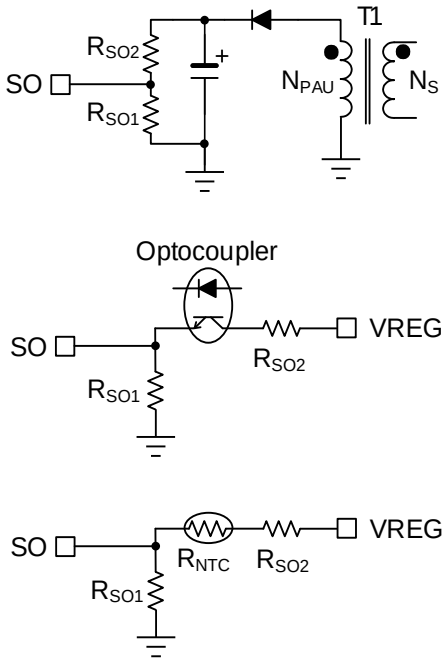



**Figure 40: SO Application Circuits for OVP and External OTP**

### Protecting CSP from Negative Voltage Stress

The HR1215's PFC current-sense resistor ($R_S$) is in the input power loop, and senses the full waveform of the PFC inductor. This means that the current from the input bridge to the output capacitor flows through $R_S$. Typically, there is inrush current during start-up and a surge current during a surge condition. This means that there may be a large voltage drop on $R_S$ that leads to an over-voltage (OV) fault on the CSP pin.

The CSP pin's internal ESD device is capable of clamping in the event of an OV fault, though only for a short time. For more details on the current limit of the CSP pin's internal ESD device under different OV conditions, see the Absolute Maximum Ratings section on page 5. Connect a 500Ω resistor between $R_S$ and the CSP pin.

If clamping on $R_S$ is required, connect two diodes in series, and place them in parallel with the $R_S$ (see Figure 41 on page 34).

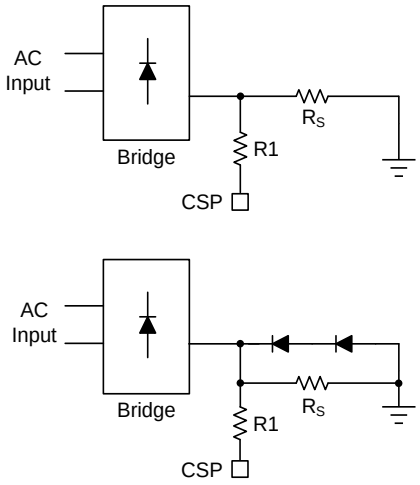



**Figure 41: CSP Pin Protection from Overstress**

The voltage is clamped by diodes once the $R_S$ voltage drop exceeds the $V_{FWD}$ drop of the two diodes. These two diodes should be carefully chosen so that the $V_{FWD}$ drop is high enough under a small forward current and high temperatures. Do not use a Schottky diode. $V_{OCL}$ should not exceed the diode clamping voltage.

## PCB Layout Guidelines

For the best results, refer to Figure 42 and follow the guidelines below:

1. Use the bulk capacitor's negative terminal as the ground for the PFC, LLC power loop, and the IC's ground. Ensure that the ground layout overlap is as small as possible.
2. Keep the IC ground trace short and wide to reduce its voltage drop.
3. Keep all the areas of the power loop and signal loop as small as possible.
4. Keep the signal traces far away from the switching node.
5. CSP and CSHB are key signals that should be treated with the highest priority.

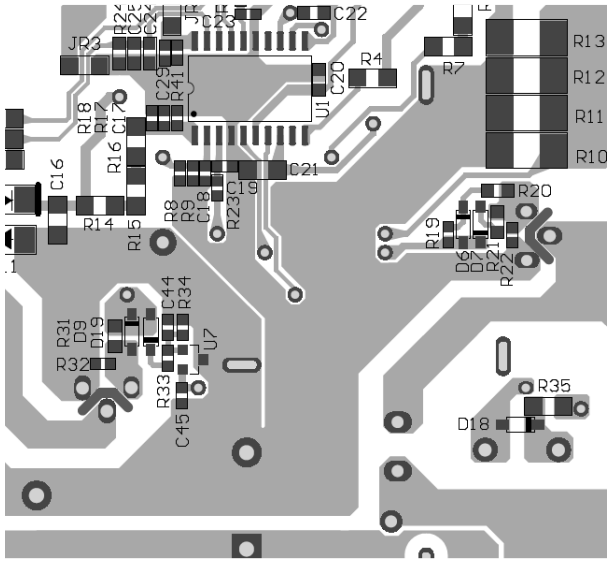



**Figure 42: Recommended PCB Layout**

## TYPICAL APPLICATION CIRCUIT

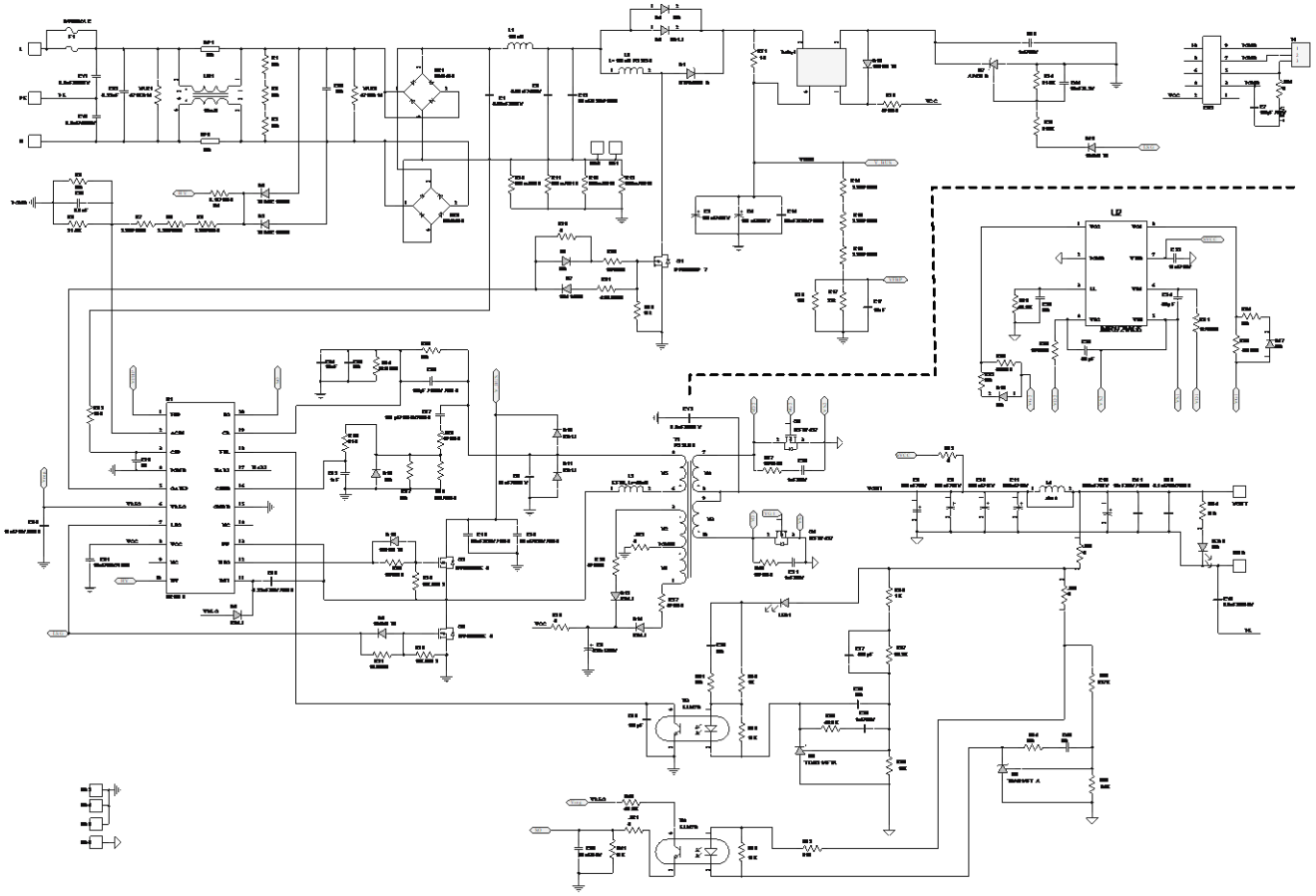
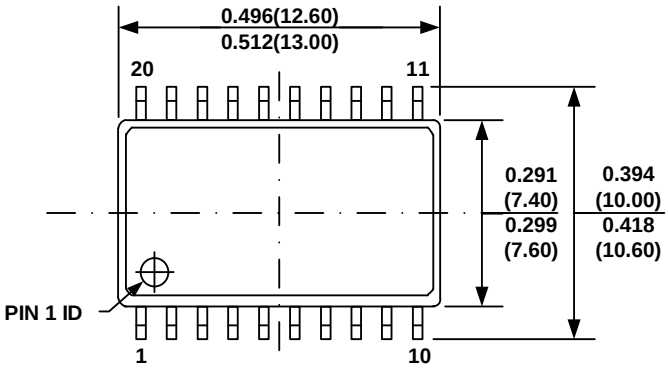


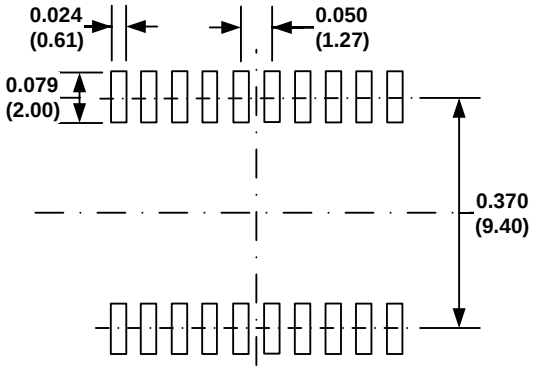
**Figure 43: Typical Application Circuit ($V_{IN}$ = 90$V_{AC}$ to 265$V_{AC}$, $V_{OUT}$ = 12V/34A)**

# PACKAGE INFORMATION

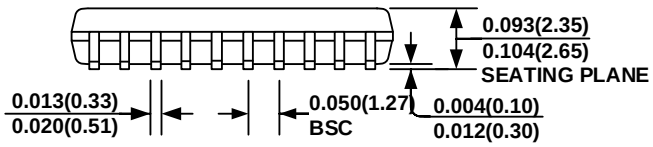
## SOIC-20 Package



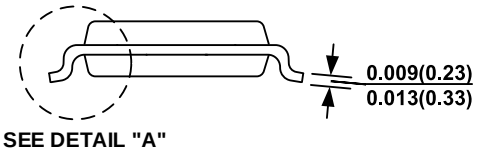

TOP VIEW



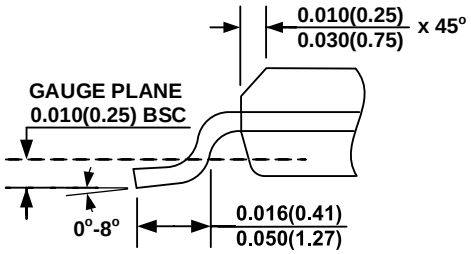

RECOMMENDED LAND PATTERN




FRONT VIEW




SIDE VIEW

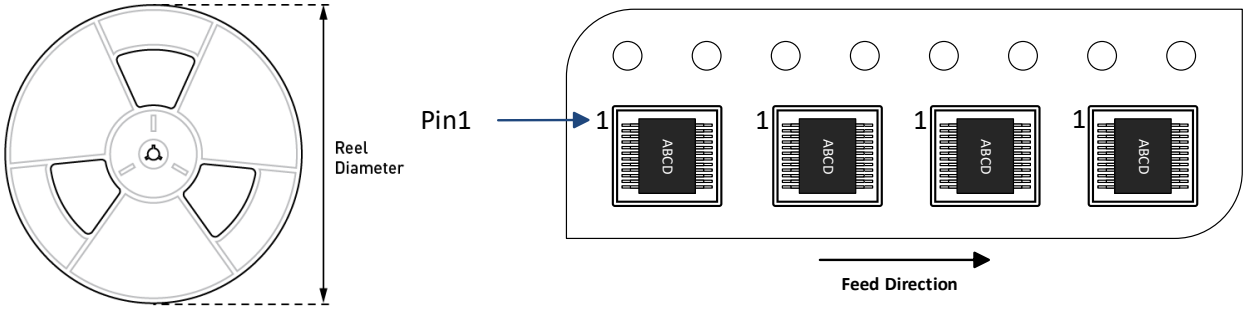



DETAIL "A"

**NOTES:**

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
6) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|---|
| HR1215GY-xxxx-Z | SOIC-20 (wide body) | 1000 | 37 | N/A | 13in | 24mm | 12mm |

## REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 1/30/2023 | Initial Release | - |