

**Description**

The HR3988 is a quad DMOS full-bridge driver capable of driving up to two stepper motors or four DC motors. Each full-bridge output is rated up to 1.2 A and 36 V. The HR3988 includes fixed off-time pulse width modulation (PWM) current regulators, along with 2-bit nonlinear DACs (digital-to-analog converters) that allow stepper motors to be controlled in full, half, and quarter steps, and DC motors in forward, reverse, and coast modes. The PWM current regulator uses the mixed decay mode for reduced audible motor noise, increased step accuracy, and reduced power dissipation.

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation.

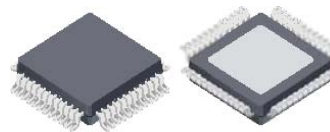
Protection features include thermal shutdown with hysteresis, under voltage lockout (UVLO) and crossover current protection. Special power up sequencing is not required.

The HR3988 is supplied in one package, TQFP48 (7 mm × 7 mm), with exposed power tabs for enhanced thermal performance. The package is lead (Pb) free, with 100% matte tin lead frame plating.

**Features and Benefits**

- 36 V output rating.
- 4 full bridges.
- Dual stepper motor driver.
- High current outputs.
- 3.3 and 5 V compatible logic supply.
- Synchronous rectification.
- Internal under voltage lockout (UVLO).
- Thermal shutdown circuitry.
- Crossover-current protection.

**Packages**



TQFP48 with exposed thermal pad

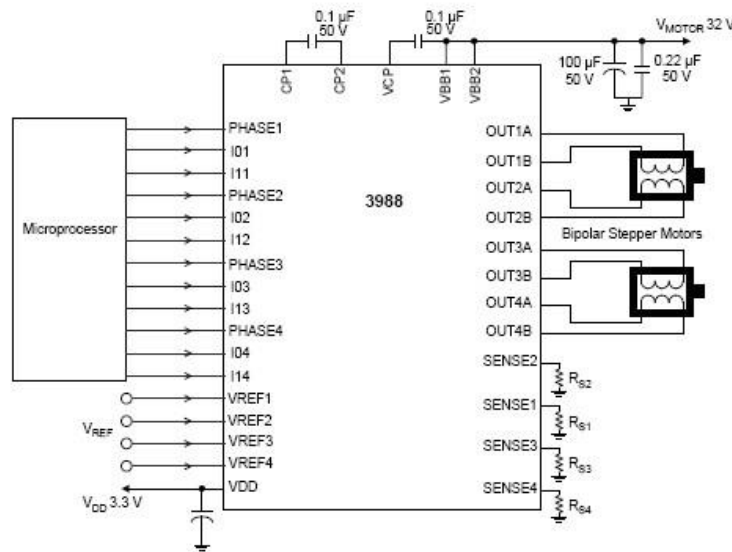


Figure 1. Typical application circuit

**Selection Guide**

Part Number	Package	Packing
HR3988	48 pin TQFP with exposed thermal pad	2500 pieces per tray

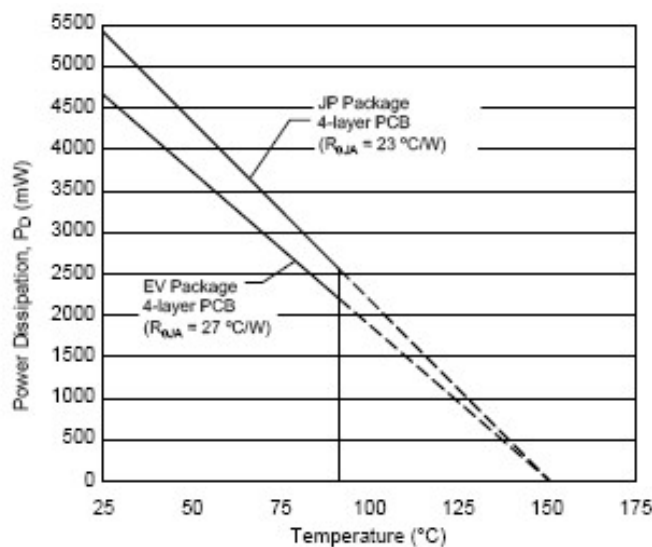
**Absolute Maximum Ratings**

Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	$V_{BB}$		-0.5 to 36	V
		Pulsed $t_w < 1 \mu s$	38	V
Logic Supply Voltage	$V_{DD}$		-0.4 to 7	V
Output Current	$I_{OUT}$	May be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a Junction Temperature of 150°C.	1.2	A
		Pulsed $t_w < 1 \mu s$	2.8	A
Logic Input Voltage Range	$V_{IN}$		-0.3 to 7	V
SENSE <sub>x</sub> Pin Voltage	$V_{SENSEx}$		0.5	V
		Pulsed $t_w < 1 \mu s$	2.5	V
VREF <sub>x</sub> Pin Voltage	$V_{REFx}$		2.5	V
Operating Temperature Range	$T_A$	Range S	-20 to 85	°C
Junction Temperature	$T_J(max)$		150	°C
Storage Temperature Range	$T_{stg}$		-40 to 125	°C

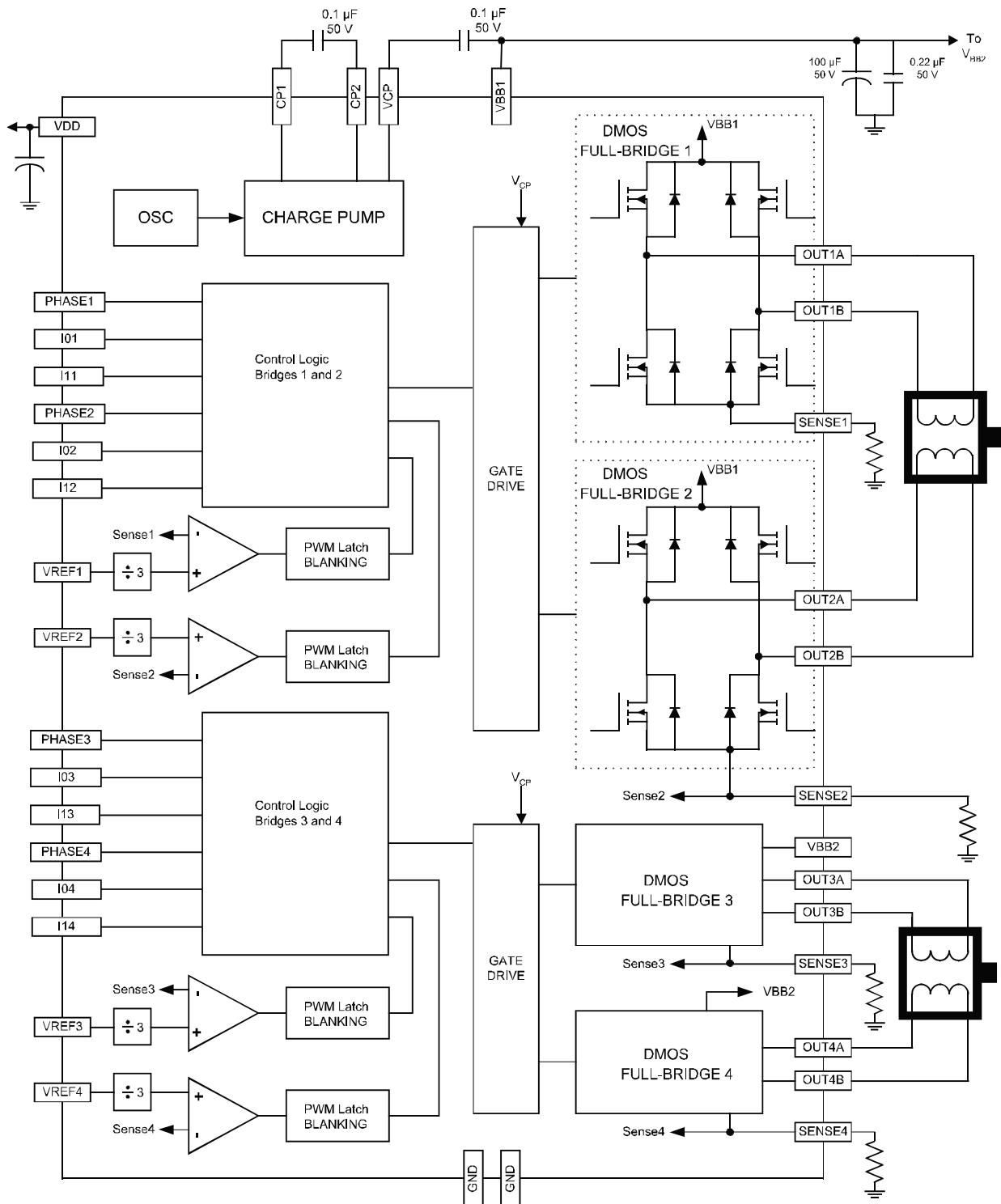
**Thermal Characteristics (may require derating at maximum conditions)**

Characteristic	Symbol	Test Conditions	Min.	Units
Package Thermal Resistance	$R_{\theta JA}$	TQFP48PP, 4 layer PCB based on JEDEC standard	23	°C/W

**Power Dissipation versus Ambient Temperature**



### Functional Block Diagram



**ELECTRICAL CHARACTERISTICS<sup>1</sup>**, valid at  $T_A = 25^\circ\text{C}$ ,  $V_{BB} = 36\text{ V}$ , unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. <sup>2</sup>	Max.	Units
Load Supply Voltage Range	$V_{BB}$	Operating	8.0	–	36	V
Logic Supply Voltage Range	$V_{DD}$	Operating	3.0	–	5.5	V
VDD Supply Current	$I_{DD}$		–	5	10	mA
Output On Resistance	$R_{DS(on)}$	Source driver, $I_{OUT} = -1.2\text{ A}$ , $T_J = 25^\circ\text{C}$	–	700	800	m $\Omega$
		Sink driver, $I_{OUT} = 1.2\text{ A}$ , $T_J = 25^\circ\text{C}$	–	700	800	m $\Omega$
$V_f$ , Outputs		$I_{OUT} = 1.2\text{ A}$	–	–	1.3	V
Output Leakage	$I_{DSS}$	Outputs, $V_{OUT} = 0$ to $V_{BB}$	–20	–	20	$\mu\text{A}$
VBB Supply Current	$I_{BB}$	$I_{OUT} = 0\text{ mA}$ , outputs on, PWM = 50 kHz, DC = 50%	–	–	8	mA
<b>Control Logic</b>						
Logic Input Voltage	$V_{IN(1)}$		$0.7 \times V_{DD}$	–	–	V
	$V_{IN(0)}$		–	–	$0.3 \times V_{DD}$	V
Logic Input Current	$I_{IN}$	$V_{IN} = 0$ to $5\text{ V}$	–20	<1.0	20	$\mu\text{A}$
Input Hysteresis	$V_{hys}$		150	300	500	mV
Propagation Delay Times	$t_{pd}$	PWM change to source on	350	550	1000	ns
		PWM change to source off	35	–	300	ns
		PWM change to sink on	350	550	1000	ns
		PWM change to sink off	35	–	250	ns
Crossover Delay	$t_{COD}$		300	425	1000	ns
Blank Time	$t_{BLANK}$		0.7	1	1.3	$\mu\text{s}$
VREFx Pin Input Voltage Range	$V_{REFx}$	Operating	0.0	–	1.5	V
VREFx Pin Reference Input Current	$I_{REF}$	$V_{REF} = 1.5$	–	–	$\pm 1$	$\mu\text{A}$
Current Trip-Level Error <sup>3</sup>	$V_{ERR}$	$V_{REF} = 1.5$ , phase current = 100%	–5	–	5	%
		$V_{REF} = 1.5$ , phase current = 67%	–5	–	5	%
		$V_{REF} = 1.5$ , phase current = 33%	–15	–	15	%
<b>Protection Circuits</b>						
VBB UVLO Threshold	$V_{UV(VBB)}$	$V_{BB}$ rising	7.3	7.6	7.9	V
VBB Hysteresis	$V_{UV(VBB)hs}$		100	500	600	mV
VDD UVLO Threshold	$V_{UV(VDD)}$	$V_{DD}$ rising	2.65	2.8	2.95	V
VDD Hysteresis	$V_{UV(VDD)hy}$		75	105	125	mV
Thermal Shutdown Temperature	$T_{JTSD}$		155	165	175	$^\circ\text{C}$
Thermal Shutdown Hysteresis	$T_{JTSDhys}$		–	15	–	$^\circ\text{C}$

<sup>1</sup>For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

<sup>2</sup>Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

<sup>3</sup> $V_{ERR} = [(V_{REF}/3) - V_{SENSE}] / (V_{REF}/3)$ .

## Functional Description

**Device Operation** The HR3988 is designed to operate two stepper motors, four DC motors, or one stepper and two DC motors. The currents in each of the output full-bridges, all N-channel DMOS, are regulated with fixed off-time pulse width modulated (PWM) control circuitry. Each full-bridge peak current is set by the value of an external current sense resistor,  $R_{Sx}$ , and a reference voltage,  $V_{REFx}$ .

If the logic inputs are pulled up to  $V_{DD}$ , it is good practice to use a high value pull-up resistor in order to limit current to the logic inputs, should an overvoltage event occur. Logic inputs include: PHASEx, I0x, and I1x.

**Internal PWM Current Control** Each full-bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a desired value,  $I_{TRIP}$ . Initially, a diagonal pair of source and sink DMOS outputs are enabled and current flows through the motor winding and  $R_{Sx}$ . When the voltage across the current sense resistor equals the voltage on the  $V_{REFx}$  pin, the current sense comparator resets the PWM latch, which turns off the source driver.

The maximum value of current limiting is set by the selection of  $R_S$  and the voltage at the  $V_{REF}$  input with a transconductance function approximated by:

$$I_{TripMax} = V_{REF} / (3 \times R_S)$$

Each current step is a percentage of the maximum current,  $I_{TripMax}$ . The actual current at each step  $I_{Trip}$  is approximated by:

$$I_{Trip} = (\% I_{TripMax} / 100) I_{TripMax}$$

where  $\% I_{TripMax}$  is given in the Step Sequencing table.

Note: It is critical to ensure that the maximum rating of  $\pm 500$  mV on each SENSEx pin is not exceeded.

**Fixed Off-Time** The internal PWM current control circuitry uses a one shot circuit to control the time the drivers remain off. The one shot off-time,  $t_{off}$ , is internally set to 30  $\mu$ s.

**Blanking** This function blanks the output of the current sense comparator when the outputs are switched by the internal current control circuitry. The comparator output is blanked to prevent false detections of over current conditions, due to reverse recovery currents of the clamp diodes, or to switching transients related to the capacitance of the load. The stepper blank time,  $t_{BLANK}$ , is approximately 1  $\mu$ s.

**Control Logic** Communication is implemented via the industry standard I1, I0, and PHASE interface. This communication logic allows for full, half, and quarter step modes. Each bridge also has an independent  $V_{REF}$  input so higher resolution step modes can be programmed by dynamically changing the voltage on the  $V_{REFx}$  pins.

**Charge Pump (CP1 and CP2)** The charge pump is used to generate a gate supply greater than the  $V_{BB}$  in order to drive the source-side DMOS gates. A 0.1 $\mu$ F ceramic capacitor should be connected between CP1 and CP2 for pumping purposes. A 0.1  $\mu$ F ceramic capacitor is required between VCP and  $V_{BBx}$  to act as a reservoir to operate the high-side DMOS devices.

**Shutdown** In the event of a fault (excessive junction temperature, or low voltage on VCP), the outputs of the device are disabled until the fault condition is removed. At power-up, the undervoltage lockout (UVLO) circuit disables the drivers.

**Synchronous Rectification** When a PWM-off cycle is triggered by an internal fixed off-time cycle, load current will recirculate. The HR3988 synchronous rectification feature will turn on the appropriate MOSFETs during the current decay, and effectively short out the body diodes with the low  $R_{DS(on)}$  driver. This significantly lowers power dissipation. When a zero current level is detected, synchronous rectification is turned off to prevent reversal of the load current.

**Mixed Decay Operation** The bridges operate in mixed decay mode. Referring to figure 2, as the trip point is reached, the device goes into fast decay mode for 30.1% of the fixed off-time period. After this fast decay portion,  $t_{FD}$ , the device switches to slow decay mode for the remainder of the off-time. During transitions from fast decay to slow decay, the drivers are forced off for approximately 600 ns. This feature is added to prevent shoot-through in the bridge. As shown in figure 2, during this “dead time” portion, synchronous rectification is not active, and the device operates in fast decay and slow decay only.

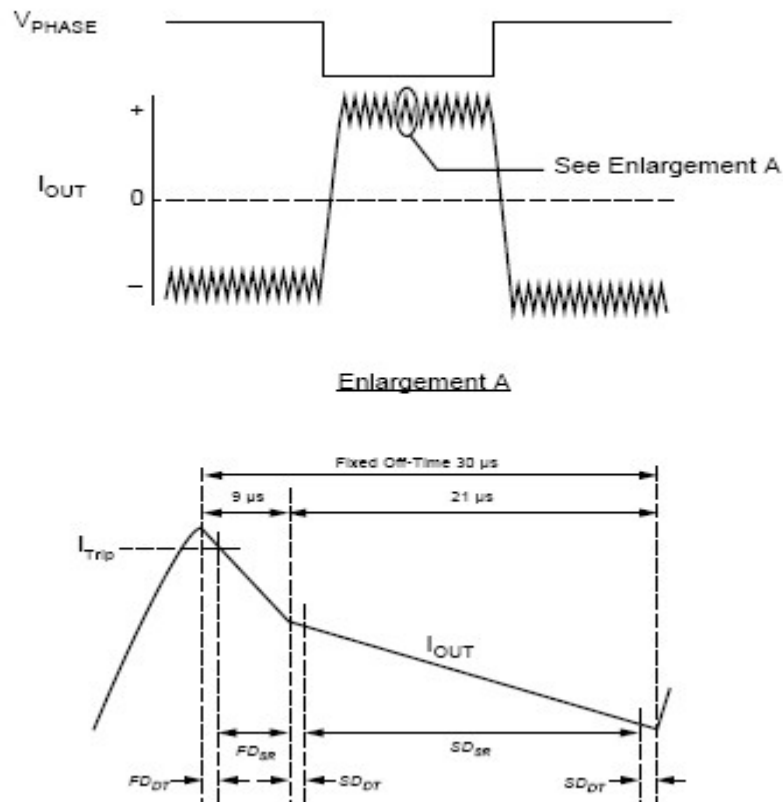


Figure 2. Mixed Decay Mode Operation

Step Sequencing Diagrams

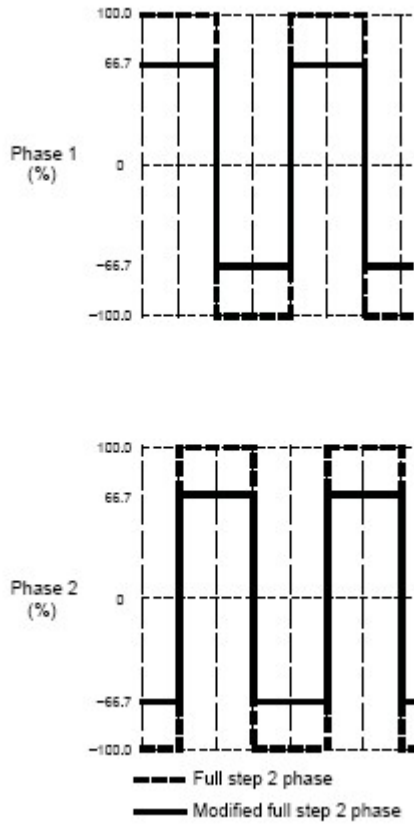


Figure 3. Step Sequencing for Full-Step Increments.

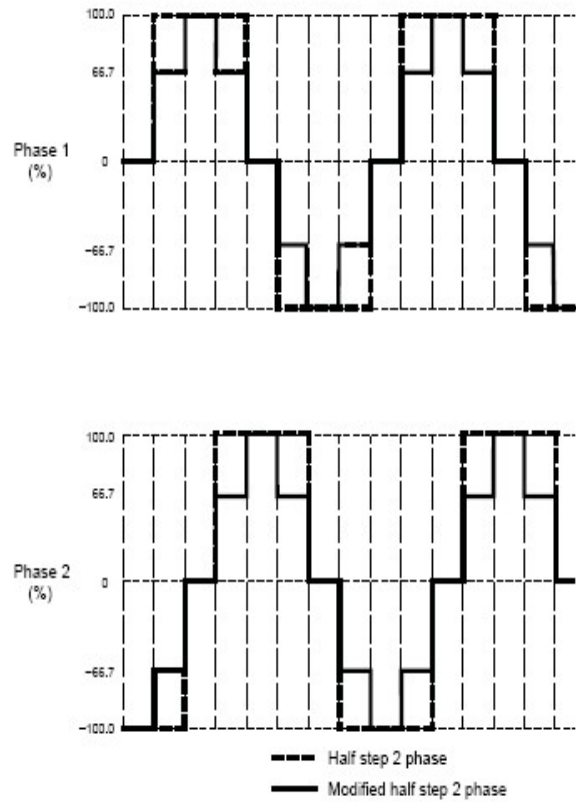


Figure 4. Step Sequencing for Half-Step Increments.

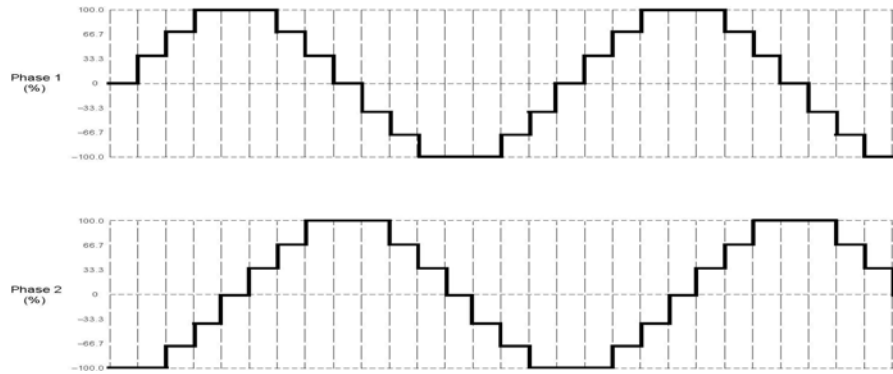


Figure 5. Step Sequence for Quarter-Step Increments

### Step Sequencing Settings

Full	1/2	1/4	Phase 1 (%I <sub>TrippMax</sub> )	I0x	I1x	PHASE	Phase 2 (%I <sub>TrippMax</sub> )	I0x	I1x	PHASE
	1	1	0	H	H	X	100	L	L	1
		2	33	L	H	1	100	L	L	1
1	2	3	100/66*	L/H*	L	1	100/66*	L/H	L	1
		4	100	L	L	1	33	L	H	1
	3	5	100	L	L	1	0	H	H	X
		6	100	L	L	1	33	L	H	0
2	4	7	100/66*	L/H*	L	1	100/66*	L/H	L	0
		8	33	L	H	1	100	L	L	0
	5	9	0	H	H	X	100	L	L	0
		10	33	L	H	0	100	L	L	0
3	6	11	100/66*	L/H*	L	0	100/66*	L/H	L	0
		12	100	L	L	0	33	L	H	0
	7	13	100	L	L	0	0	H	H	X
		14	100	L	L	0	33	L	H	1
4	8	15	100/66*	L/H*	L	0	100/66*	L/H	L	1
		16	33	LL/H*	H	0	100	L	L	1

\* Denotes modified step mode



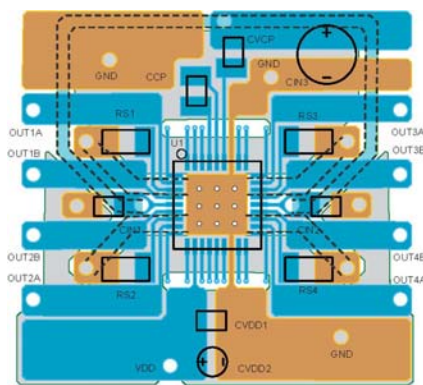
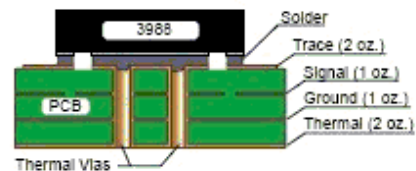
**Motor Configurations** For applications that require either a stepper/DC motor driver or dual DC motor driver, Heroic offers the A3989 and A3995. These devices are offered in the same 36 pin QFN package as the HR3988. The DC motor drivers are capable of supplying 2.4 A at 36 V. Commutation is done with a standard phase/enable logic interface. Please refer to the Heroic website for further information and datasheets about those devices.

**DC Motor Control** Each of the 4 full bridges has independent PWM current control circuitry that makes the HR3988 capable of driving up to four DC motors at currents up to 1.2 A. Control of the DC motors is accomplished by tying the I0, I1 pins together creating an equivalent ENABLE function with maximum current defined by the voltage on the corresponding VREF pin. The DC motors can be driven via a PWM signal on this enable signal, or on the corresponding PHASE pin. Motor control includes forward, reverse, and coast.

**Layout** The printed circuit board should use a heavy ground-plane. For optimum electrical and thermal performance, the HR3988 must be soldered directly onto the board. On the underside of the HR3988 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

**Grounding** In order to minimize the effects of ground bounce and offset issues, it is important to have a low impedance single-point ground, known as a star ground, located very close to the device. By making the connection between the exposed thermal pad and the ground plane directly under the HR3988, that area becomes an ideal location for a star ground point.

A low impedance ground will prevent ground bounce during high current operation and ensure that the supply voltage remains stable at the input terminal. The recommended PCB layout shown in the diagram below, illustrates how to create a star ground under the device, to serve both as low impedance ground point and thermal path.



TQFP48PP package layout shown

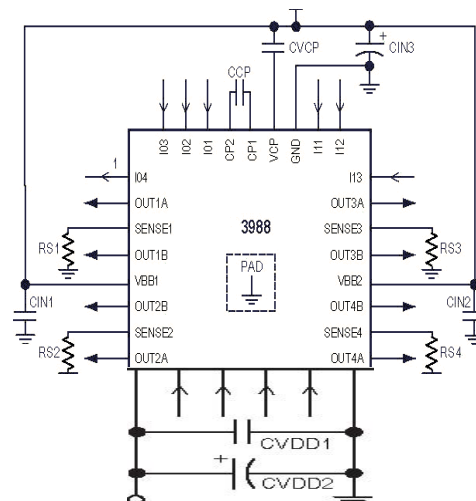


Figure 6. Printed circuit board layout with typical application circuit, shown at right. The copper area directly under the HR3988 (U1) is soldered to the exposed thermal pad on the underside of the device. The thermal vias serve also as electrical vias, connecting it to the ground plane on the other side of the PCB, so the two copper areas together form the star ground.

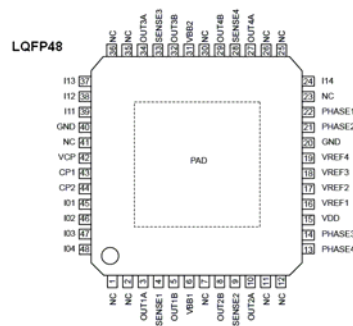
The two input capacitors should be placed in parallel, and as close to the device supply pins as possible. The ceramic capacitor should be closer to the pins than the bulk capacitor. This is necessary because the ceramic capacitor will be responsible for delivering the high frequency current components.

**Sense Pins** The sense resistors,  $RS_x$ , should have a very low impedance path to ground, because they must carry a large current while supporting very accurate voltage measurements by the current sense comparators. Long ground traces will cause

additional voltage drops, adversely affecting the ability of the comparators to accurately measure the current in the windings. As shown in the layout below, the  $SENSE_x$  pins have very short traces to the  $RS_x$  resistors and very thick, low impedance traces directly to the star ground underneath the device. If possible, there should be no other components on the sense circuits.

Note: When selecting a value for the sense resistors, be sure not to exceed the maximum voltage on the  $SENSE_x$  pins of  $\pm 500$  mV.

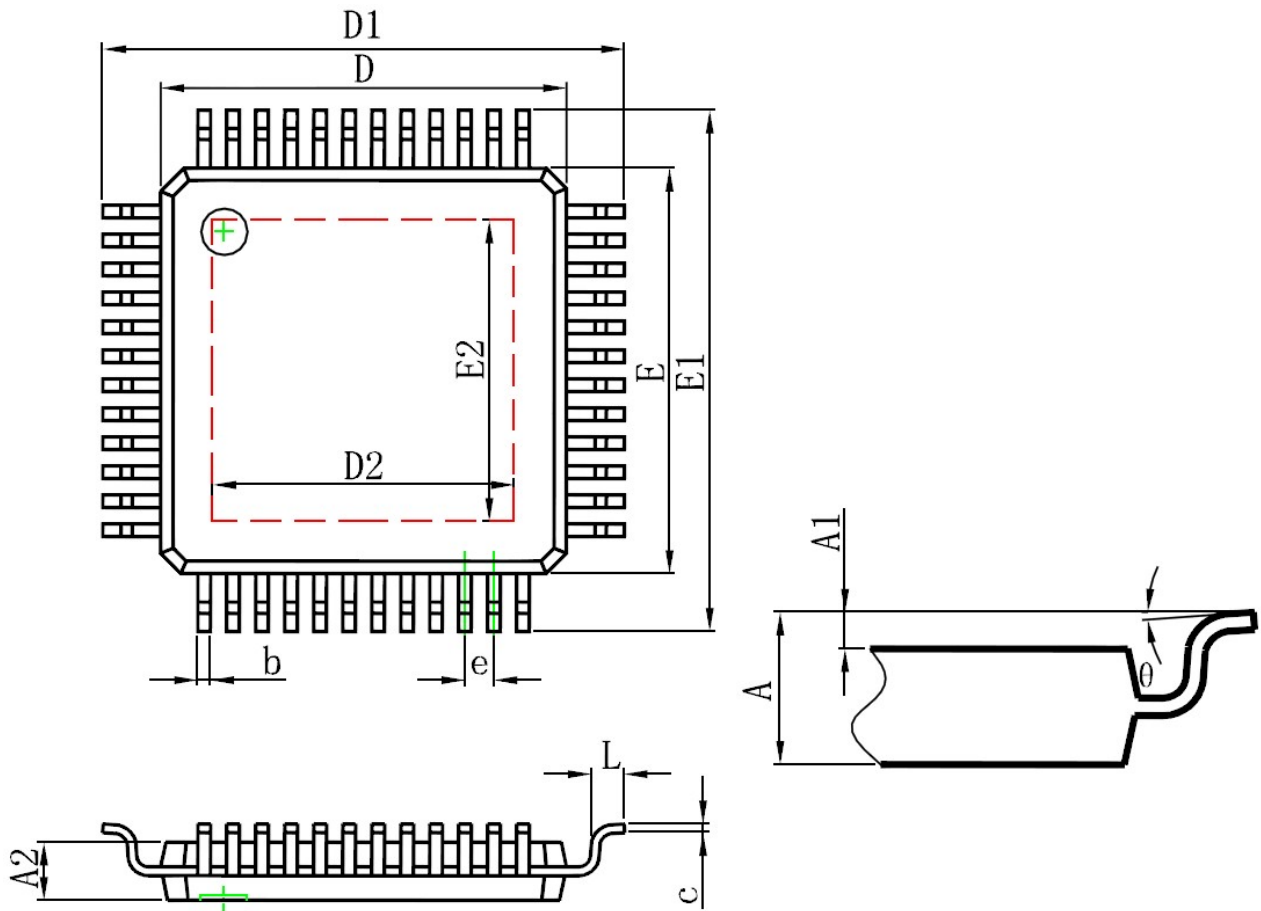
### Pin-out Diagrams



Terminal List Table

Number (LQFP48)	Pin Name	Pin Description
3	OUT1A	DMOS Full-Bridge 1 Output A
4	SENSE1	Sense Resistor Terminal for Bridge 1
5	OUT1B	DMOS Full-Bridge 1 Output B
6	VBB1	Load Supply Voltage
8	OUT2B	DMOS Full-Bridge 2 Output B
9	SENSE2	Sense Resistor Terminal for Bridge 2
10	OUT2A	DMOS Full-Bridge 2 Output A
13	PHASE4	Control Input
14	PHASE3	Control Input
15	VDD	Logic Supply Voltage
16	VREF1	Analog Input
17	VREF2	Analog Input
18	VREF3	Analog Input
19	VREF4	Analog Input
20	GND	Ground
21	PHASE2	Control Input
22	PHASE1	Control Input
24	I14	Control Input
27	OUT4A	DMOS Full-Bridge 4 Output A
28	SENSE4	Sense Resistor Terminal for Bridge 4
29	OUT4B	DMOS Full-Bridge 4 Output B
31	VBB2	Load Supply Voltage
32	OUT3B	DMOS Full-Bridge 3 Output B
33	SENSE3	Sense Resistor Terminal for Bridge 3
34	OUT3A	DMOS Full-Bridge 3 Output A
37	I13	Control Input
38	I12	Control Input
39	I11	Control Input
40	GND	Ground
42	VCP	Reservoir Capacitor Terminal
43	CP1	Charge Pump Capacitor Terminal
44	CP2	Charge Pump Capacitor Terminal
45	I01	Control Input
46	I02	Control Input
47	I03	Control Input
48	I04	Control Input
1, 2, 7, 11, 12, 23, 25, 26, 30, 35, 36, 41	NC	No Connect
-	PAD	Exposed pad for enhanced thermal performance. Should be soldered to the PCB.

**48 Pin TQFP with Exposed Thermal Pad**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.950	1.050	0.037	0.041
b	0.190	0.260	0.007	0.010
c	0.090	0.200	0.004	0.008
D	6.900	7.100	0.272	0.280
D1	8.850	9.150	0.348	0.360
D2	5.100	5.300	0.201	0.209
E	6.900	7.100	0.272	0.280
E1	8.850	9.150	0.348	0.360
E2	5.100	5.300	0.201	0.209
e	0.500 (BSC)		0.020 (BSC)	
L	0.450	0.750	0.018	0.030
θ	1°	7°	1°	7°

## Revision History

Revision	Revision Date	Description of Revision
Rev. 0.1	Aug. 26, 2013	First version
Rev. 0.2	Nov.11, 2013	Pre-release Trial version

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