8-bit MCU
HR7P171

Datasheet

☐ **Brief**

☑ **Datasheet**

☐ **Specifications**

SHANGHAI EASTSOFT MICROELECTRONICS CO., LTD.

2017.12.08

Application Notes

Power On/Off Sequence

Eastsoft MCUs are designed with separate power pins. If a MCU is applied in a system which has multiple power supplies, the MCU should be powered on first or at the same time together with other devices involved in the system. Conversely, the MCU should be powered off after all other devices are powered off. Reversed steps may cause excessive voltage or current on the MCU internal components, which is very likely to cause malfunction and weaken components performances. For details, please refer to the datasheet.

Reset

Eastsoft MCUs provide an internal power-on reset circuit, which could possibly be invalid in different fast/slow power on/off systems. To ensure a proper reset function, the following resets are recommended: external reset, brown-out reset, watchdog reset, etc. The triode reset or the RC reset is recommended when the external reset circuit is used; otherwise, it is suggested to connect the reset pin to power supply with a resistor or to use other protection circuits if necessary. For details, please refer to the datasheet.

Clock

Eastsoft MCUs offer internal and external clock sources. The internal clock frequency may experience a variation due to unstable temperature or voltage, which may affect the accuracy of the clock source. When a ceramic or crystal oscillator circuit is used as an external clock source, it is suggested to enable the oscillator start-up timer. When a RC oscillator circuit is used, it is suggested to take account of the capacitor matching and resistor matching. When an external active oscillator or external clock input is used, consider to input a high-voltage or low-voltage. For details, please refer to the datasheet

Initialization

For different application systems, it is necessary to initialize registers, memories and function modules, especially the multiplexed I/O pins, in order to avoid the unknown status of I/O pins when MCU is powered on.

Pins

Eastsoft MCUs are designed with wide-range input voltage. It is suggested that the input high-level voltage should be higher than V_{IHMIN}, the input low-level voltage should be lower than V_{ILMAX}. To avoid the noise entering into MCU, the input voltage should not be set between V_{IHMIN} and V_{ILMAX}. The unused I/O pins are suggested to be set to input mode, and should be connected to VDD via pull-up resistors or to GND via pull-down resistors. Alternatively, set unused pins to output mode with fixed voltage and leave them floating. How to handle unused pins varies from application to application and it is important to follow the specific application specification and instructions.

ESD Protection

Eastsoft MCUs have industrial ESD standard protection circuit. It is suggested to take proper protection measures depending on application/storage environment to prevent MCUs from static electricity. Special attention should be paid to the humidity of application environment. Do not use the insulators which could cause static electricity. Use anti-static-electricity container/shields or conductive materials to store and transport the MCUs. Ground all the testing tools, measuring tools, including the workbench. Use anti-static-electricity belts or gloves, and do not touch the MCU with fingers directly.

EFT Protection

Eastsoft MCUs have industrial EFT standard protection circuit.. When MCUs are used in PCB systems, the related design requests should be satisfied, including wiring of VDD or GND (i.e. separation of digital/analog power supply,

single-point/multi-point grounding and so on), protection circuits for reset pins, decoupling capacitors between VDD and GND, separate processing of high/low frequency circuits, selection of single-layer/multi-layer board and so on.

Development Environment

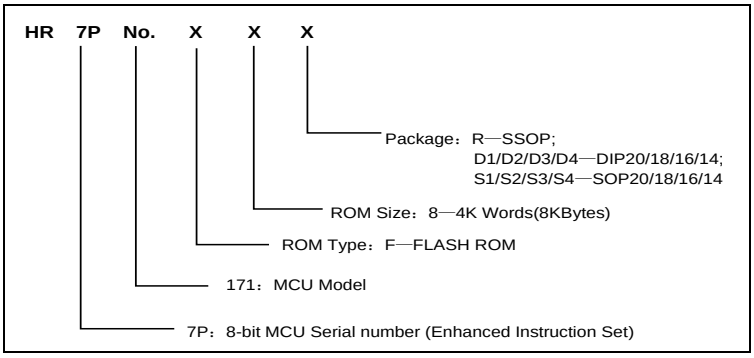
Eastsoft MCUs have a complete software/hardware development environment with protected intellectual property.. When using the development tools, such as assembler, compiler, burner and firmware emulator of Shanghai Eastsoft IC Co, Ltd. or by the appointed third party, please follow the related specifications and instructions..

Note: For any questions arising from product development, please contact us through the sales department or other ways.

Ordering Information

Part Number	Program Memory	Data Memory	Package
HR7P171F8D1*	FLASH：4K Words	SRAM：256 Bytes	DIP20
HR7P171F8D2*			DIP18
HR7P171F8D3*			DIP16
HR7P171F8D4*			DIP14
HR7P171F8S1			SOP20
HR7P171F8S2			SOP18
HR7P171F8S3			SOP16
HR7P171F8S4			SOP14
HR7P171F8R1			SSOP20

Note*: These products are no longer available.



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Revision History

Date	Summary
2017-12-8	Initial version, based on the HR7P171_Datasheet_C_V2.6

Note: Should you have any questions, please refer to the corresponding version of the HR7P171_Datasheet_C.

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  - High performance Harvard-architecture RISC CPU
  - 66 RISC instructions
  - Maximum Operating Frequency up to 16MHz
  - 8-level PC Hardware Stack
  - Reset Vector located at 000_H, Default Interrupt Vector located at 004_H, Interrupt Priority and Interrupt Vector Table supported.
  - Supports Interrupt Handler
- Memory
  - 4K Words FLASH Program Memory
  - 256 Bytes SRAM Data Memory
  - Program memory supports direct addressing
  - Data memory supports direct addressing and indirect addressing
- I/O Ports
  - Port A (PA0~PA4,PA6~PA7)
  - Port B (PB0~PB7)
  - Port C (PC0~PC1)
  - Up to 17 ports are large current configurable
- Peripherals
  - 8-bit Timer T8N
    - Timer mode (Fosc) / counter mode (external counter clock input)
    - Configurable prescaler
    - Interrupt capability
  - 8-bit PWM Timer T8P1/T8P2
    - Timer mode (Fosc)
    - Configurable prescaler and post-scaler
    - Interrupt capability
    - One standard PWM output extension mode supported
    - One enhanced PWM output extension mode supported
  - 16-bit Gate Timer T16G
    - Timer mode (Fosc) / counter mode (external counter clock input)
    - Configurable prescaler
    - Interrupt capability
    - Capture mode (TE1CI)
    - Compare mode (TE1CO)
  - Analog to Digital Convertor (ADC)

- 10-bit resolution
- 8 analog input channels
- Interrupt capability

◇ Analog Comparator ACP and Reference Voltage Module

- 2 analog comparators
- 1 programmable reference voltage module

◆ Special Functions

◇ High precision 16MHz internal oscillator

- Frequeny can be divided down to 125KHz
- Factory-calibrated accuracy within ±2% (25℃, VDD=3.3V ~5V) ,

◇ Low power mode

◇ Power On Reset POR

◇ Brown-out Reset BOR

◇ External reset N_MRST

◇ Integrated hardware watchdog timer

◇ In System Programming ISP interface

◇ Encrypted programming code

◇ In Circuit Debugger ICD

◆ Design and Process

◇ Low power consumption, high speed Flash CMOS Process

◇ DIP /SOP/ SSOP-20pin

◇ DIP/SOP-18pin, DIP/SOP-16pin, DIP/SOP-14pin

◇ SSOP-10pin

◆ Operation Condition

◇ Operating Voltage: 3.0V ~ 5.5V

◇ Operating Temperature: -40 ~ 85℃

1. 2 Applications

The HR7P171 is ideal for small home appliances, inverters and other applications.

1. 3 Block Diagram

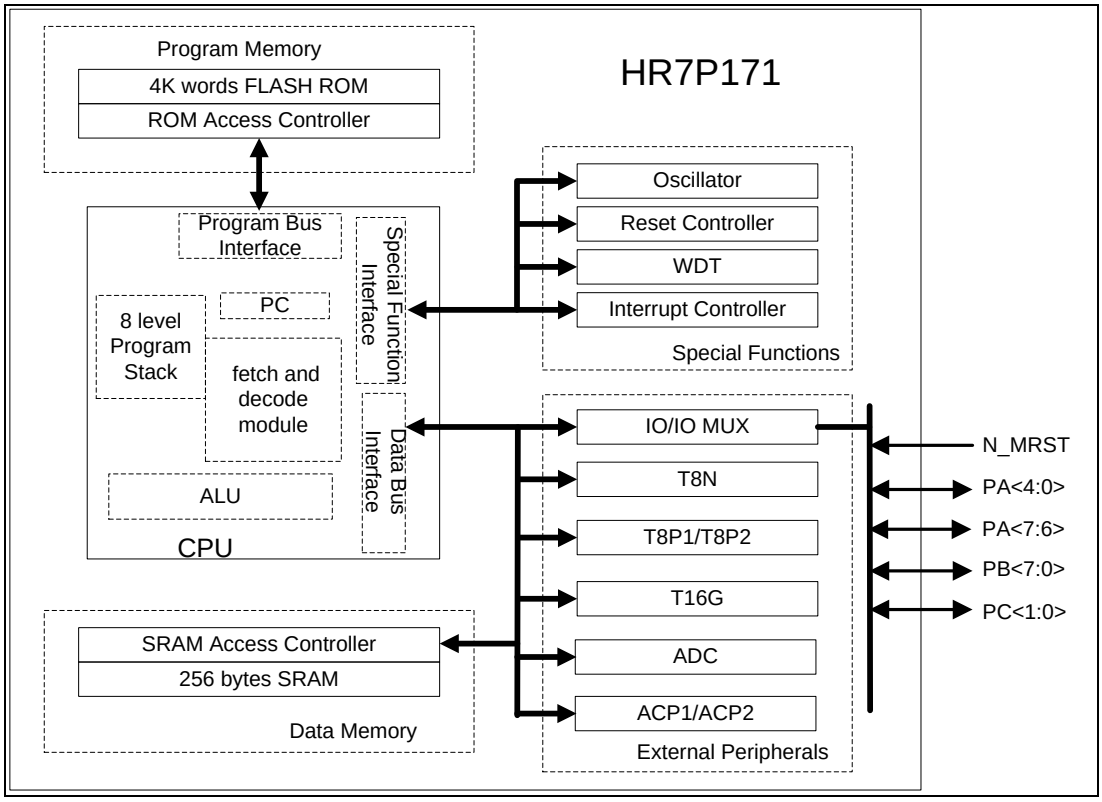


Figure 1-1 HR7P171 Block Diagram

Note: N_MRST is active-low

1. 4 Pin Diagrams

1. 4. 1 20-Pin

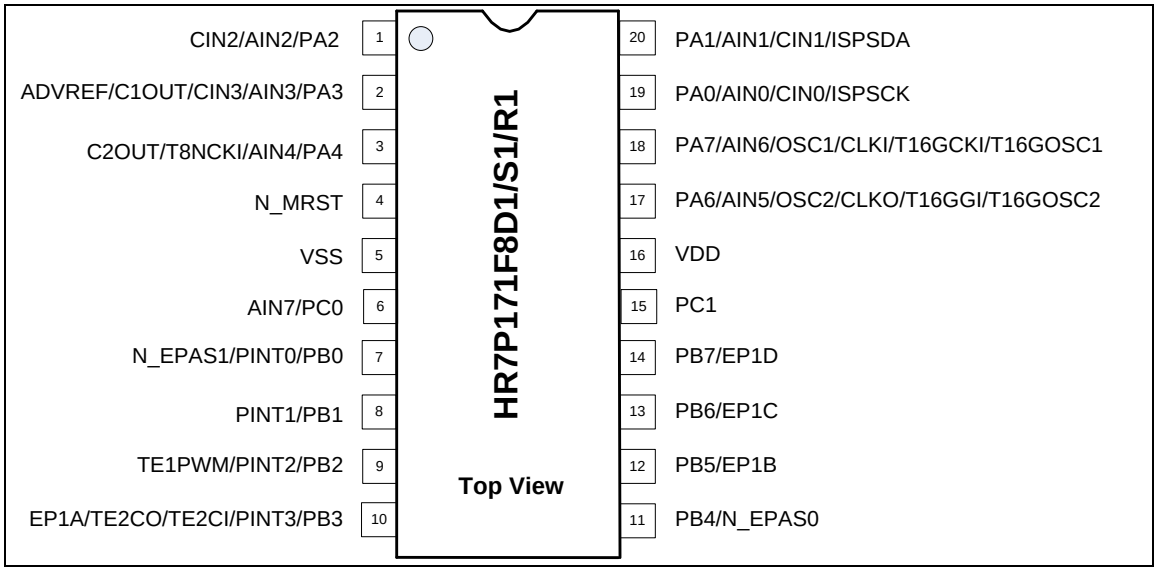


Figure 1-2 HR7P171 (DIP20/SOP20/SSOP20)Top view

1. 4. 2 18-Pin

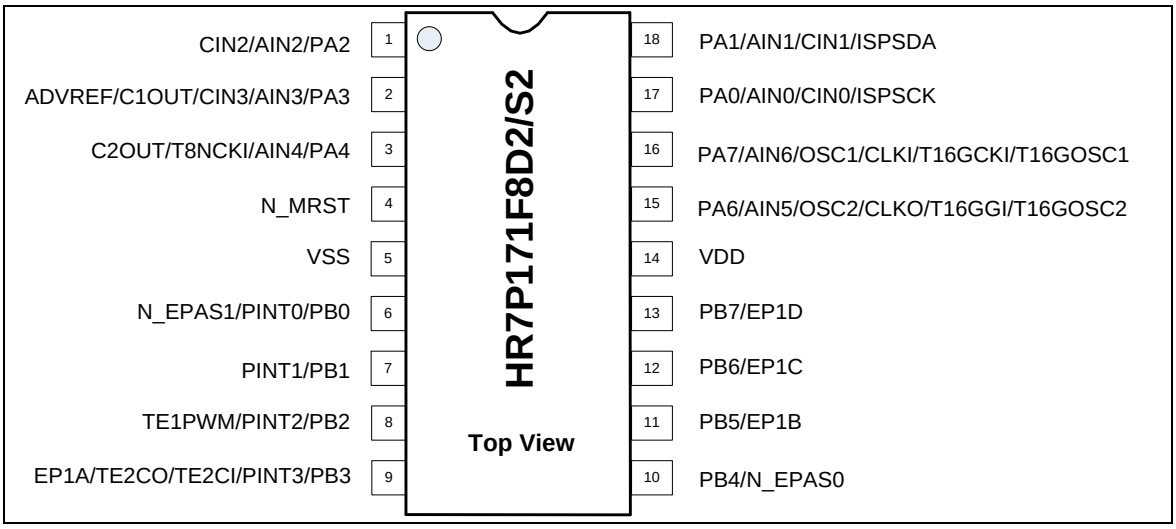


Figure 1-3 HR7P171 (DIP18/SOP18)Top view

1. 4. 3 16-Pin

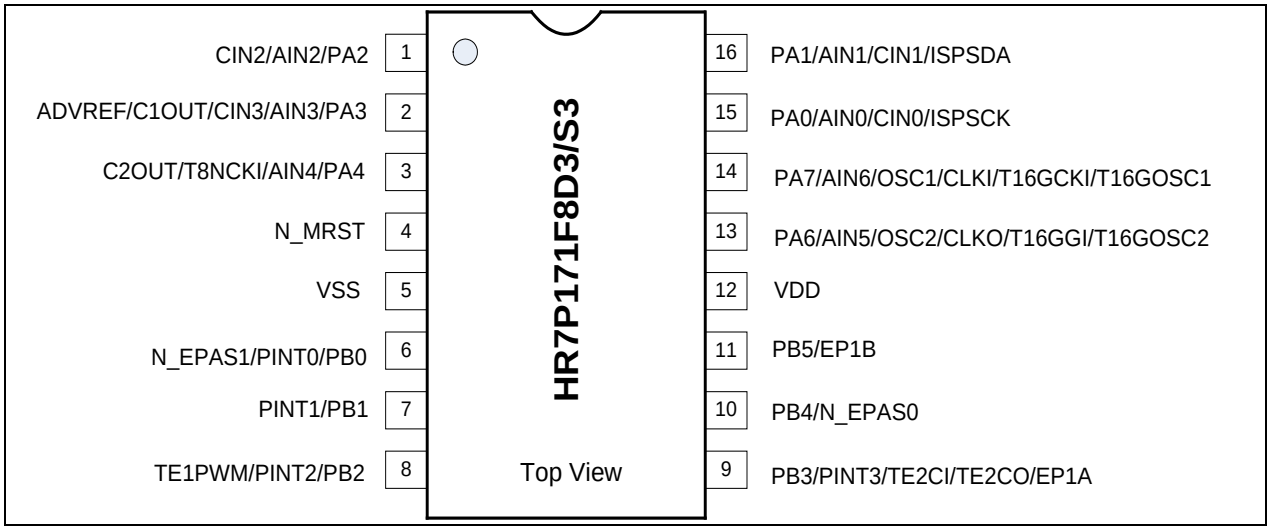


Figure 1-4 HR7P171 (DIP16/SOP16) Top view

1. 4. 4 14-Pin

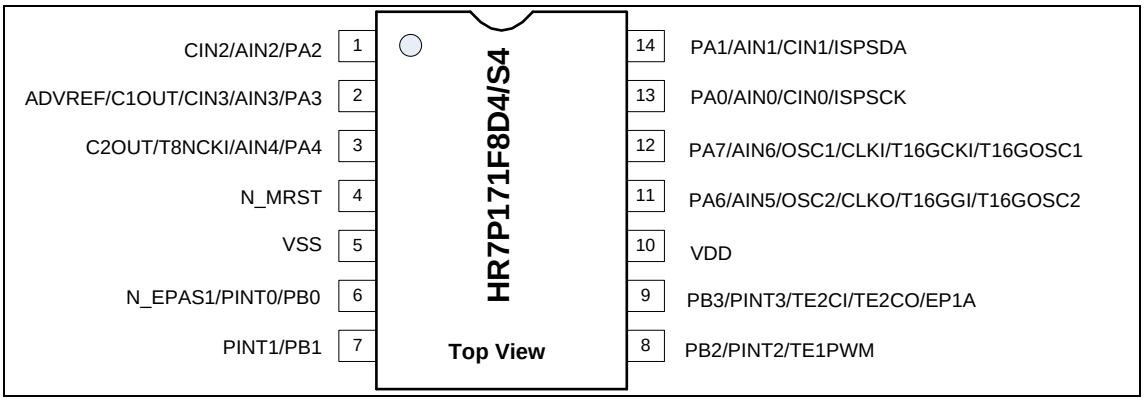


Figure 1-5 HR7P171 (DIP14/SOP14) Top view

Note：N_MRST, , N_EPAS0 and , N_EPAS1 are active-low.

1. 5 Pin Descriptions

1. 5. 1 Pin Allocation

Pin Name	HR7P171			
	20-pin	18-pin	16-pin	14-pin
PA0/AIN0/CIN0/ISPSCK	19	17	15	13
PA1/AIN1/CIN1/ISPSDA	20	18	16	14
PA2/AIN2/CIN2	1	1	1	1
PA3/AIN3/CIN3/C1OUT/ADVREF	2	2	2	2
PA4/AIN4/T8NCKI/C2OUT	3	3	3	3
PA6/AIN5/OSC2/CLKO/T16GGI/ T16GOSC2	17	15	13	11
PA7/AIN6/OSC1/CLKI/T16GCKI/ T16GOSC1	18	16	14	12
PB0/PINT0/N_EPAS1	7	6	6	6
PB1/PINT1	8	7	7	7
PB2/PINT2/TE1PWM	9	8	8	8
PB3/PINT3/TE2CI/TE2CO/EP1A	10	9	9	9
PB4/N_EPAS0	11	10	10	-
PB5/EP1B	12	11	11	-
PB6/EP1C	13	12	-	-
PB7/EP1D	14	13	-	-
PC0/AIN7	6	-	-	-
PC1	15	-	-	-
N_MRST	4	4	4	4
VDD	16	14	12	10
VSS	5	5	5	5

Table 1-1 Pin Allocation

1. 5. 2 Pin Multiplexing

Pin Name	Multiplexing	A/D	Port Description	Notes
PA0/AIN0/CIN0/ ISPSCK	PA0	D	General Purpose I/O	Weak Pull-up can be enabled
	AIN0	A	ADC Analog Channel 0 Input	
	CIN0	A	Comparator 0 Input	
	ISPSCK	D	ISP Clock Input	
PA1/AIN1/CIN1/ ISPDA	PA1	D	General Purpose I/O	Weak Pull-up can be enabled
	AIN1	A	ADC Analog Channel 1 Input	
	CIN1	A	Comparator 1 Input	
	ISPDA	D	ISP Data Input/Output	
PA2/AIN2/CIN2	PA2	D	General Purpose I/O	Weak Pull-up can be enabled
	AIN2	A	ADC Analog Channel 2 Input	
	CIN2	A	Comparator 2 Input	
PA3/AIN3/CIN3/ C1OUT/ADVRE F	PA3	D	General Purpose I/O	Weak Pull-up can be enabled
	AIN3	A	ADC Analog Channel 3 Input	
	CIN3	A	Comparator 3 Input	
	C1OUT	D	Comparator 1 Output	
	ADVREF	A	External A/D Reference Voltage Input	
PA4/AIN4/ T8NCKI/C2OUT	PA4	D	General Purpose I/O	Weak Pull-up can be enabled
	AIN4	A	ADC Analog Channel 4 Input	
	T8NCKI	D	T8N Clock Input	
	C2OUT	D	Comparator 2output	
PA6/AIN5/OSC2/ CLKO/ T16GGI/T16GO SC2	PA6	D	General Purpose I/O	Weak Pull-up can be enabled
	AIN5	A	ADC Analog Channel 5 Input	
	OSC2	A	Crystal/Oscillator Pin 2	
	CLKO	D	Fosc/4 Reference Clock Output	
	T16GGI	D	T16G Gate Control Input	
	T16GOSC2	A	T16G Oscillator Pin 2	
PA7/AIN6/OSC1/ CLKI/ T16GCKI/ T16GOSC1	PA7	D	General Purpose I/O	Weak Pull-up can be enabled
	AIN6	A	ADC Analog Channel 6 Input	
	OSC1	A	Crystal/Oscillator Pin 1	
	CLKI	A/D	System Clock Input	
	T16GCKI	D	T16G Clock Input	
	T16GOSC1	A	T16G Oscillator Pin 1	
PB0/PINT0 /N_EPAS1	PB0	D	General Purpose I/O	Weak Pull-up can be enabled
	PINT0	D	External Port Interrupt 0 Input	

[Contiune 1]

Pin Name	Multiplexing	A/D	Port Description	Notes
	N_EPAS1	D	EPWM Automatic Shutdown Input 1	
PB1/PINT1	PB1	D	General Purpose I/O	Weak Pull-up can be enabled
	PINT1	D	External Port Interrupt 1 Input	
PB2/PINT2/ TE1PWM	PB2	D	General Purpose I/O	Weak Pull-up can be enabled
	PINT2	D	External Port Interrupt 2 Input	
	TE1PWM	D	TE1 Standard PWM Output	
PB3/PINT3/ TE2CI/TE2CO/ EP1A	PB3	D	General Purpose I/O	Weak Pull-up can be enabled
	PINT3	D	External Port Interrupt 3 Input	
	TE2CI	D	TE2 Capturer Input	
	TE2CO	D	TE2 Comparator Output	
	EP1A	D	TE2 EPWM Output	
PB4/N_EPAS0	PB4	D	General Purpose I/O	Weak Pull-up can be enabled
	N_EPAS0	D	EPWM Automatic Shutdown Input 0	
PB5/EP1B	PB5	D	General Purpose I/O	Weak Pull-up can be enabled
	EP1B	D	EPWM Output	
PB6/EP1C	PB6	D	General Purpose I/O	Weak Pull-up can be enabled
	EP1C	D	EPWM Output	
PB7/EP1D	PB7	D	General Purpose I/O	Weak Pull-up can be enabled
	EP1D	D	EPWM Output	
PC0/AIN7	PC0	D	General Purpose I/O	-
	AIN7	A	ADC Analog Channel 7 Input	-
PC1	PC1	D	General Purpose I/O	-
N_MRST	N_MRST	-	Master Reset Input	-
VDD	VDD	-	Power	-
VSS	VSS	-	GND, , 0V Reference	-

Table 1-2 Pins Description

Note：

1. A = Analog, D = Digital;
2. N_MRST, N_EPAS0 and N_EPAS1 are active-Low;
3. All general purpose data I/O are TTL/SMT input and CMOS output.

Chapter 2 CPU Characteristics

2. 1 CPU Overview

- CPU Features
  - High performance Harvard-architecture RISC CPU
  - 66 RISC instructions, instruction length 15 bits
  - Maximum operating frequency up to 16MHz
  - Program memory supports direct addressing mode
  - Data memory supports direct and indirect addressing modes
  - Reset vector located at 000_H, default interrupt vector located at 004_H, interrupt priority and interrupt vector table supported
  - Supports Interrupt handler

2. 2 System Clock and Machine Cycle

The system clock of HR7P171 operates up to 16MHz. The on-chip clock generator divides the input clock into four non-overlapping orthogonal clocks termed as phase1 (p1), phase2 (p2), phase3 (p3) and phase4 (p4), which compose one machine cycle.

2. 3 Instruction Set Overview

HR7P171 supports 66 RISC instructions of HR7P series.

Most of the instructions can be executed within a single machine cycle, except the instructions of some conditional jumps and program control operations, whose executions take two machine cycles. Four system clock cycles compose one machine cycle, a single machine cycle is 1μs if the system clock frequency is 4 MHz.

For details, please refer to Appendix Instruction Set.

2. 4 PC and Hardware Stack

2. 4. 1 Program Counter (PC)

HR7P171 contains a 12-bit PC with addressing range from 000_H to FFF_H. Accessing a location beyond this range will cause an endless loop. The PC returns to 0000_H after reset. The interrupt vector start addresses are at 004_H, 008_H, $00C_H$, 010_H, 014_H, 018_H, $01C_H$, 020_H and 024_H.

For PC<11:0>, PC<7:0> could be read and written directly via PCRL, whereas PC<11:8>could only be indirectly assigned via PCRH<3:0>. On any reset, PCRL, PCRH and PC will be cleared. The value in PCRH register will not be changed when PC operates with hardware stack.

The content below shows how PC value changes by execuiting different instructions.

◇ When modifing the PC value through instructions directly, PC<7:0> can be modified directly by assigning value to PCRL or executing instructions with PCRL as target register, while the value of PCRH<3:0> will be assigned to PC<11:8>. That means PC<7:0> = PCRL<7:0> while PC<11:8>= PCRH<3:0>. Therefore, to modify the PC value, the value of PCRH<3:0> should be modified first, then PCRL<7:0>;

◇ When executing instructins of CALL and GOTO, the lower 11 bits of PC value will be provided by 11 bits of immediate (operand) in instruction, and PC<11> = PCRH<3>;

◇ When executing the other instructions, the PC value will be increased by one automatically.

Application example：Instructions application with PCRL as destination register.

```
……
MOVI    pageaddr
MOVA    PCRH        ; set table page address
MOVI    tableaddr   ; set offset to A
LCALL   TABLE       ; access Table by calling subroutine
……
TABLE:
ADD     PCRL          ; add offset to PC, pointing to accessed address
RETIA   0X01
RETIA   0X02
RETIA   0X03
……
```

2. 4. 2 Hardware Stack

HR7P171 is designed with an 8-level hardware stack, whose width is the same as PC, The stack is used for the PUSH and POP operations of PC. When the CALL or LCALL instruction is executed or an interrupt is responded, the PC will be pushed into stack automatically. When executing the RET, RETIA or RETIE, the stack will POP the latest PUSH value to PC.

The 8-level hardware stack only supports 8-level buffer. This means that the hardware stack only holds the 8 recent pushed values and the 9th push overwrites the 1st push. Likewise, the 9th pop may cause the program flow out of control..

2. 5 Special Function Register

Reg. Name	Base Select Register (BSET)		
Address	081_H 181_H		
Reset value	1111 1111		
PS<2:0>	bit2-0	R/W	T8N/WDT Prescaler ratio select bits 000: 1:2 001: 1:4 010: 1:8 011: 1:16 100: 1:32 101: 1:64 110: 1:128 111: 1:256
PSA	bit3	R/W	Prescaler assign bit 0：Prescaler assigned to T8N 1：Prescaler assigned to WDT
T8NSE	bit4	R/W	T8N Clock edge select bit 0：T8NCKI rising edge 1：T8NCKI falling edge
T8NCS	bit5	R/W	T8N clock source select bit 0:Internal clock frequency divided by 4 (Fosc/4) 1:T8NCKI(ext. clock source) input
PEG	bit6	R/W	PINT interrupt edge select bit 0：PINT falling edge 1：PINT rising edge
-	bit7	-	Not used

Reg. Name	Program Status Word Register(PSW)		
Address	003_H 083_H 103_H 183_H		
Reset value	0000 0xxx		
C	bit0	R/W	Full Carry /Borrow Bit 0:No carry bit or one borrow bit 1:One carry bit or no Borrow bit
DC	bit1	R/W	Half Carry /Half Borrow Bit, for addition/subtraction instruction 0:No carry bit or one borrow bit on lower 4 bits 1:One carry bit or no borrow bit on lower 4 bits
Z	bit2	R/W	Zero flag bit 0:The result of an arithmetical or logical operation is not zero 1:The result of an arithmetical or logical operation is zero
-	bit7-3	-	Not used

Reg. Name	Section Select Register(BKSR)		
Address	$00C_H$ $08C_H$ $10C_H$ $18C_H$		
Reset value	0000 0000		
RP<1:0>	bit1-0	R/W	Register space select bits(direct addressing) RP<1:0> | Section Selection 00 | Section0(000_H ~ $07F_H$) 01 | Section1(080_H ~ $0FF_H$) 10 | Section2(100_H ~ $17F_H$) 11 | Section3(180_H ~ $1FF_H$)
-	bit3-2	-	Unused
IRP	bit4	R/W	Register space select bits together with IAA<7> (indirect addressing) IRP :IAA<7> | Section selection 00 | Section0(000_H ~ $07F_H$) 01 | Section1(080_H ~ $0FF_H$) 10 | Section2(100_H ~ $17F_H$) 11 | Section2(180_H ~ $1FF_H$)
-	bit7-5	-	Not used

Chapter 3 Memory

3. 1 Program Memory

3. 1. 1 Overview

The program memory of this chip is 4K words Flash memory. The 12-bit PC has the address range from 000_H to FFF_H. Addressing beyond the address range will make PC return back to 000_H. The reset vector is at 000_H, and the interrupt vectors are at 004_H,008_H, $00C_H$,010_H,014_H,018_H,$01C_H$,020_H and 024_H.

3. 1. 2 Addressing Mode

The program memory supports direct addressing mode. The PC fetches the instructions from the program memory by direct addressing.

3. 1. 3 Program Memory Map and Stack

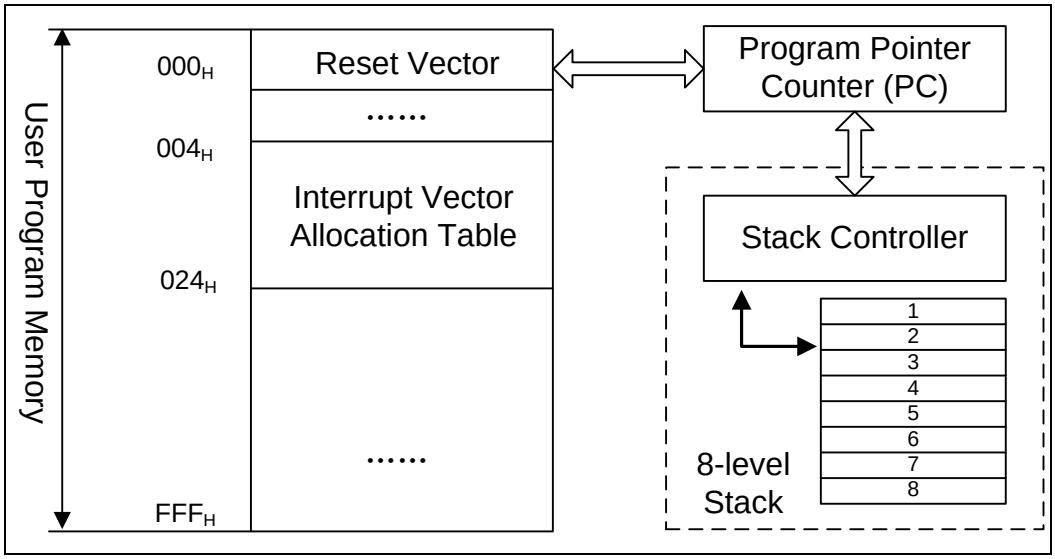


Figure 3-1 Program Memory Map and Stack

3. 2 Data Memory

3. 2. 1 Data memory address map

Data memory consists of the special function registers and the general purpose data registers, which can be divided into 4 sections (section0~3). Each data section consists of the corresponding special function register area and general purpose data register area. And among them ,$0F0_H$ ~ $0FF_H$, 170_H ~ $17F_H$ and $1F0_H$ ~ $1FF_H$ are mapped to the same physical space of 070_H ~ $07F_H$.

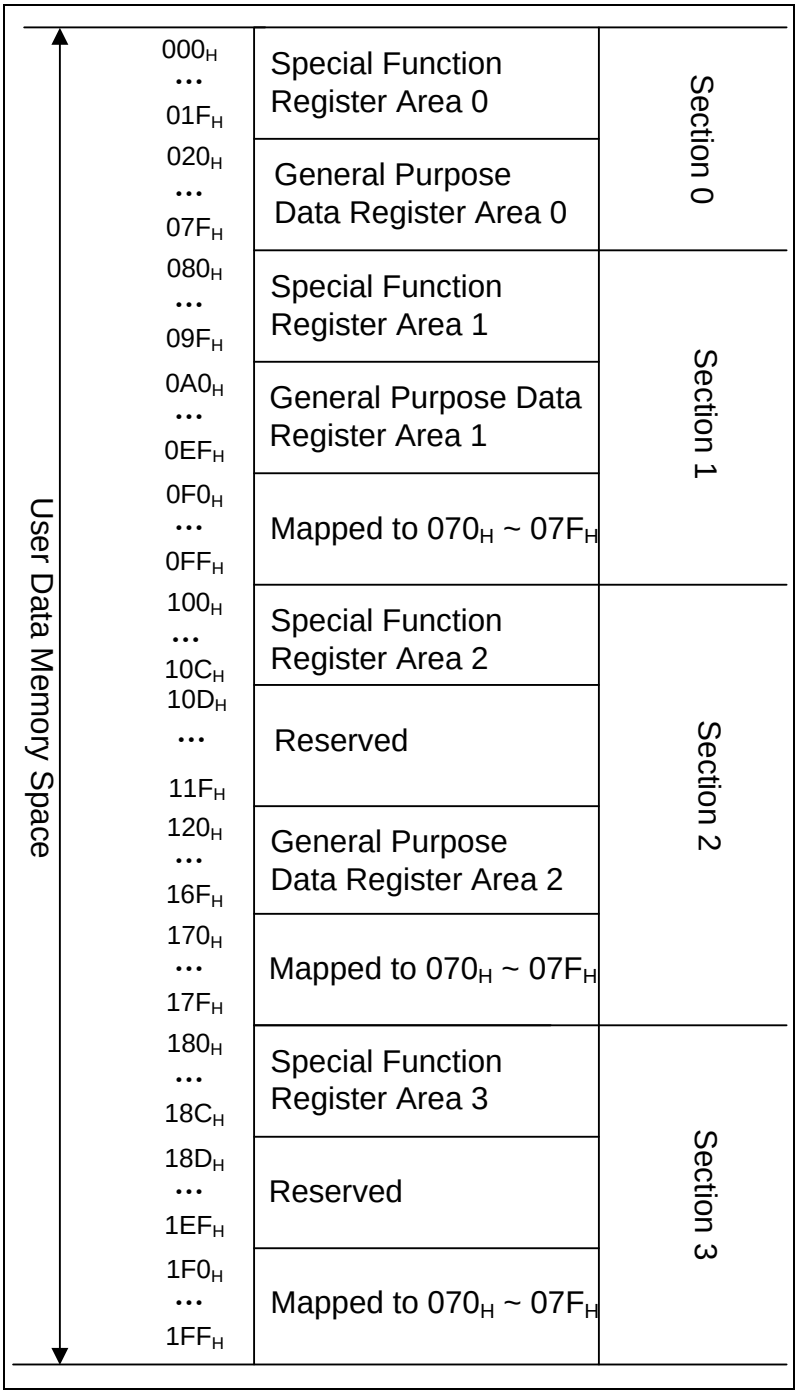


Figure 3-2 Data Memory Address Map

3. 2. 2 Addressing Mode

The addressing mode of data memory includes the direct addressing and indirect addressing:

Direct Addressing:

The RP<1:0> of BKSR are the higher address bits of direct addressing, which are used to select section 0~3. The operand in instruction indicates 7-bit address information for direct addressing in the selected section.

Indirect Addressing:

In indirect addressing mode, the higher address bits consist of the IRP bit of the BKSR and the highest bit of the IAA register (Indirect Accessing Address register), which are used for selection in section 0~3; The lower 7 bits of IAA hold the lower address bits for addressing in the selected section. The indirect addressing is done by read/write of IAD register.

IAD register is not a physical register. Reading from or writing to IAD is actually accessing the location specified by IAA. In other words, IAA is used as an address register and IAD is used as a data register in the indirect addressing mode. Reading IAD itself indirectly will return to 00_H, writing to IAD register indirectly is regarded as NULL operation (Status bits may be affected).

Application Example: Clear registers in Section 0 (020_H ~ $02F_H$) via Indirect addressing.

```
BCC   BKSR, IRP    ; Select Section
MOVI  0X20         ; Initialize pointer
MOVA  IAA          ; IAA points to RAM
NEXT1:
CLR   IAD          ; Clear IAD
INC   IAA          ; IAA increased by one
JBS   IAA, 4       ;
GOTO  NEXT1        ; not finished, loop back to location NEXT1
CONTINUE: ……       ; finished, continue to execute the following code
……
```

Application Example: Write $5A_H$ into registers in Section 1 ($0B0_H$ ~ $0B7_H$) via indirect addressing.

```
CONTINUE:
BCC   BKSR, IRP    ; Select section
MOVI  0XB0         ; Initialize pointer
MOVA  IAA          ; IAA points to RAM
NEXT1:
```

```
MOVI  0X5A        ; Assign 5A_H to register A
MOVA  IAD         ; Assign data to IAD using indirect addressing
INC   IAA         ; IAA increased by one
MOVI  0XB8        ; Assign B8_H to register A
XOR   IAA, 0      ; Perform XOR on IAA and B8_H
JBS   PSW, Z      ; Check if IAA =B8_H
GOTO  NEXT1       ; If IAA≠B8_H, continue looping
CONTINUE: ……      ; If IAA = B8_H, continue with following code
……
```

3. 2. 3 Special Function Register Area

Special function registers include special function register area 0 ~ 3. See the following tables for details.

Special Function Register Area 0/4:

Address	Reg. Name	Function Description	Notes
000_H	IAD	Indirect Addressing Data Register	-
001_H	T8N	T8N Register	-
002_H	PCRL	Program Counter Register Low Byte	-
003_H	PSW	Program Status Word Register	-
004_H	IAA	Indirect Addressing Address Register	-
005_H	PA	Port A Register	-
006_H	PB	Port B Register	-
007_H	PC	Port C Register	-
008_H	-	-	-
009_H	-	-	-
$00A_H$	PCRH	Program Counter Register High Byte	-
$00B_H$	INTC0	Interrupt Control Register 0	-
$00C_H$	BKSR	Section Select Register	-
$00D_H$	INTF0	Interrupt Flag Register 0	-
$00E_H$	T16GL	T16G Counter Register Low Byte	-
$00F_H$	T16GH	T16G Counter Register High Byte	-
010_H	T16GC	T16G Control Register	-
011_H	T8P1	T8P1 Register	-
012_H	T8P1C	T8P1 Control Register	-
013_H	CALR	Internal Clock Calibration Register	-
014_H	INTF1	Interrupt Flag Register 1	-
015_H	TE2L	TE2 Register Low Byte	-
016_H	TE2H	TE2 Register High Byte	-
017_H	TE2C	TE2 Control Register	-
018_H	TE2PWMC	EPWM Configuration Register	-
019_H	TE2AS	TE2 Auto Shutdown Register	-
$01A_H$	N_PAPU	Port A Pull-up Register	-
$01B_H$	N_PBPU	Port B Pull-up Register	-
$01C_H$	INTF2	Interrupt Flag Register 2	-
$01D_H$	T8P1P	T8P1 Period Register	-
$01E_H$	ADCRL	ADC Result Register Low Byte	-
$01F_H$	ADCC0	ADC Control Register 0	-

Special Function Register Area 1/4:

Address	Reg. Name	Function Description	Notes
080_H	IAD	Indirect Addressing Data Register	-
081_H	BSET	Select Register	-
082_H	PCRL	Program Counter Register Low Byte	-
083_H	PSW	Program Status Word Register	-
084_H	IAA	Indirect Addressing Address Register	-
085_H	PAT	Port A Tristate Register	-
086_H	PBT	Port B Tristate Register	-
087_H	PCT	Port C Tristate Register	-
088_H	-	-	-
089_H	-	-	-
$08A_H$	PCRH	Program Counter Register High Byte	-
$08B_H$	INTC0	Interrupt Control Register 0	-
$08C_H$	BKSR	Section Select Register	-
$08D_H$	INTE0	Interrupt Enable Register 0	-
$08E_H$	PWRC	Power Control Register	-
$08F_H$	INTC1	Interrupt Control Register 1	-
090_H	IPR	Interrupt Priority Register	-
091_H	T8P2	T8P2 Register	-
092_H	T8P2C	T8P2 Control Register	-
093_H	OSCC	Oscillator Control Register	-
094_H	INTE1	Interrupt Enable Register 1	-
095_H	ACPC	Analog Compare Control Register	-
096_H	VRC	Reference Voltage Control Register	-
097_H	TE1L	TE1 Register Low Byte	-
098_H	TE1H	TE1 Register High Byte	-
099_H	TE1C	TE1 Control Register	-
$09A_H$	ADSEL	Analog Digital Select Register	-
$09B_H$	WKDC	Weak-up Delay Control Register	-
$09C_H$	INTE2	Interrupt Enable Register 3	-
$09D_H$	T8P2P	T8P2 Period Register	-
$09E_H$	ADCRH	ADC Result Register High Byte	-
$09F_H$	ADCC1	ADC Control Register 1	-

Special Function Register space 2/4:

Address	Reg. Name	Function Description	Notes
100_H	IAD	Indirect Addressing Data Register	-
101_H	T8N	T8N Register	-
102_H	PCRL	Program Counter Register Low Byte	-
103_H	PSW	Program Status Word Register	-
104_H	IAA	Indirect Addressing Address Register	-
105_H	PA	Port A Register	-
106_H	PB	Port B Register	-
107_H	PC	Port C Register	-
108_H	-	-	-
109_H	-	-	-
$10A_H$	PCRH	Program Counter Register High Byte	-
$10B_H$	INTC0	Interrupt Control Register 0	-
$10C_H$	BKSR	Section Select Register	-
$10D_H$	-	-	-
$10E_H$	-	-	-
$10F_H$	-	-	-

Special Function Register Area 3/4:

Address	Reg. Name	Function Description	Notes
180_H	IAD	Indirect Addressing Aata Register	-
181_H	BSET	Base Select Register	-
182_H	PCRL	Program Counter Register Low Byte	-
183_H	PSW	Program Status Word Register	-
184_H	IAA	Indirect Addressing Address Register	-
185_H	PAT	Port A Tristate Register	-
186_H	PBT	Port B Tristate Register	-
187_H	PCT	Port C Tristate Register	-
188_H	-	-	-
189_H	-	-	-
$18A_H$	PCRH	Program Counter Register High Byte	-
$18B_H$	INTC0	Interrupt Control Register 0	-
$18C_H$	BKSR	Section Select Register	-
$18D_H$	-	-	-
$18E_H$	-	-	-
$18F_H$	-	-	-

3. 2. 4 General Purpose Data Memory

The general purpose data memory has the physical address range 020_H ~ $07F_H$ (section 0), $0A0_H$ ~ $0FF_H$ (section 1), 120_H ~ $17F_H$ (section 2) and $1F0_H$ ~ $1FF_H$ (section 3), among which $0F0_H$ ~ $0FF_H$, 170_H ~ $17F_H$ and $1F0_H$ ~ $1FF_H$ are mapped to 070_H ~ $07F_H$, used as common data storage. The general purpose data memory has a capacity of 256 bytes.

General purpose data memory is used to hold data and control information during the execution of instructions. Its value is unknown after a power-on reset.

The general purpose data memory may be directly addressed, or indirectly addressed through the IAA register.

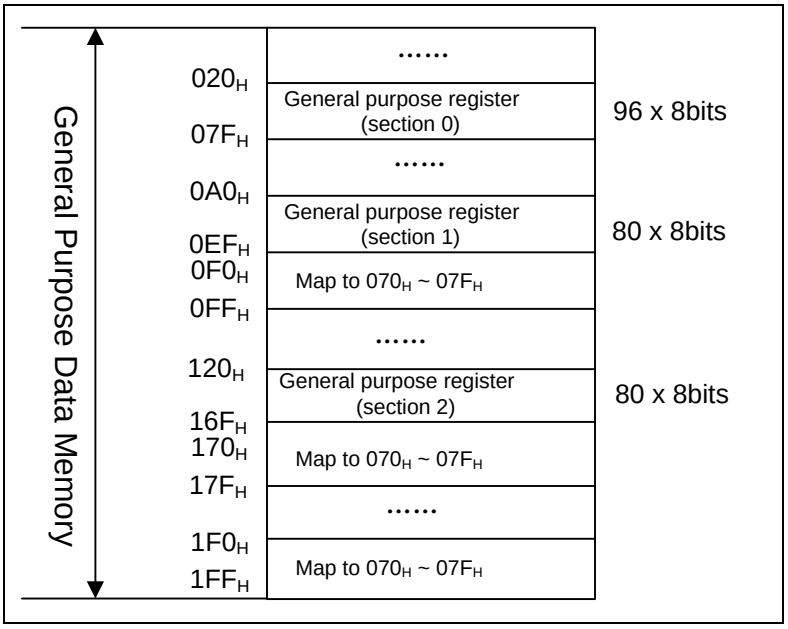


Figure 3-3 General Purpose Data Memory Address Map

Chapter 4 Input/Output Ports

4. 1 Overview

HR7P171 supports up to 17 I/O ports.

All I/O ports are TTL/SMT input and CMOS output. Each port is associated with a related control register PxT for input/output control. When PxT is set to “1”, the related I/O port will work in input mode; to the contrary, when PxT is set to “0”, the related I/O port will work in output mode.

When an I/O port is in output mode, the voltage level is determined by the related Px register, “1” is high level and “0” is low level.

When an IO port is in input mode, the status of the voltage level can be read from Px register.

All the IO ports have independent internal weak pull-up control registers except port C. Weak pull-up can be enabled or disabled by N_PxPU Register. Weak pull-up is disabled if N_PxPU is “1”, and is enabled if N_PxPU is “0”. Internal weak pull-up will be disabled automatically when a port is configured as output or analog input.

When executing read-modify-write operation on a Px register, the voltage level should be read first and then write the value back to Px register after modification. Because bitwise operation is also a read-modify-write operation, a bitwise operation on a Px register might also affect other bits of the Px register.

Pin multiplexing is supported and the port level is determined by the specific function. See Pin Descriptions and I/O MUX for details.

Pin	0	1	2	3	4	5	6	7	Remark
PA	B	B	B	B	B	-	B	B	-
PB	B	B	B	B	B	B	B	B	-
PC	A	A	-	-	-	-	-	-	-

Table 4-1 IO Port Block Diagram Information Table

Note: “A” represents port block diagram A, “B” represents port block diagram B. The two diagrams are as follows:

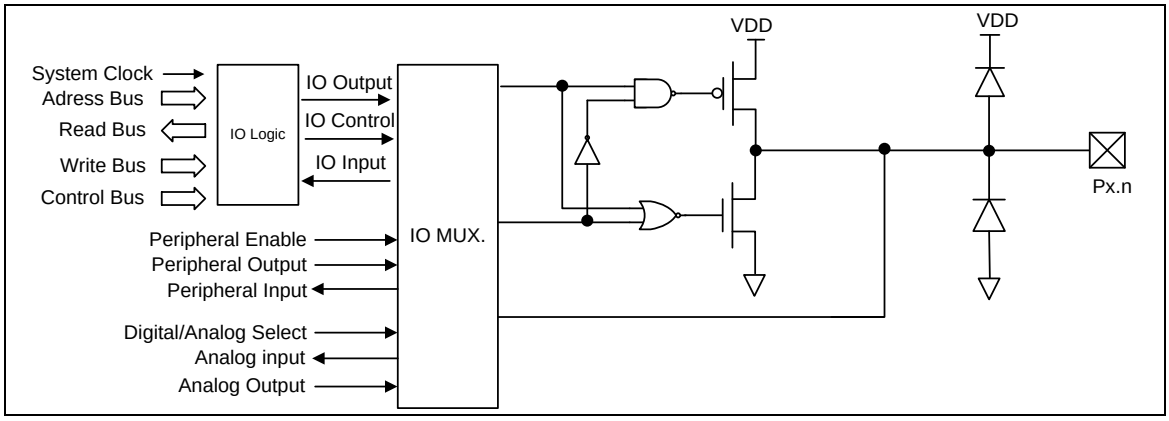


Figure 4-1 IO Port Block Diagram A

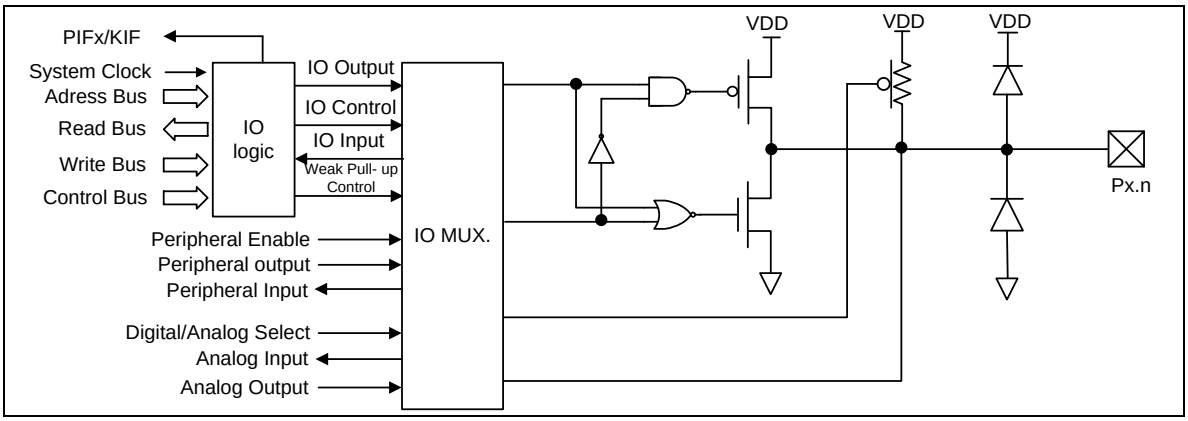


Figure 4-2 IO Port Block Diagram B

4. 2 I/O MUX

Pin	Pin MUX.	PAT	Peripheral Enable	Remarks
PA0	PA0	-	-	-
	AIN0	1	Set Analog Digital Select Register ADSEL	
	CIN0	1	Set ACP Control Register ACPM<2:0>	
	ISPSCK	1	-	-
PA1	PA1	-	-	-
	AIN1	1	Set Analog Digital Select Register ADSEL	
	CIN1	1	Set ACP Control Register ACPM<2:0>	
	ISPDA	-	-	-
PA2	PA2	-	-	-
	AIN2	1	Set Analog Digital Select Register ADSEL	
	CIN2	1	Set ACP Control Register ACPM<2:0>	
PA3	PA3	-	-	-
	AIN3	1	Set Analog Digital Select Register ADSEL	
	CIN3	1	Set ACP Control Register ACPM<2:0>	
	C1OUT	0	Set ACP Control Register ACPM<2:0>	
	ADVREF	1	Set ADC Control Register ADCC1<6>	
PA4	PA4	-	-	-
	AIN4	1	Set Analog Digital Select Register ADSEL	
	T8NCKI	1	Set T8N Control Register T8NCS	
	C2OUT	0	Set ACP Control Register ACPM<2:0>	
PA6	PA6	-	-	-
	AIN5	1	Set Analog Digital Select Register ADSEL	
	OSC2	1	Configure Configuration Word Bit OSCS<2:0>	
	CLKO	0	Configure Configuration Word Bit OSCS<2:0>	
	T16GGI	1	Set T16G Control Register T16GC<6>	
	T16GOSC2	-	Configure Configuration Word Bit OSCS<2:0> Set T16G Control Register T16GC<3>	
PA7	PA7	-	-	-
	AIN6	1	Set Analog Digital Select Register ADSEL	
	OSC1	1	Configure Configuration Word Bit OSCS<2:0>	
	CLKI	1	Configure Configuration Word Bit OSCS<2:0>	
	T16GCKI	1	Set T16Gcontrol Register T16GC<1:0>	
	T16GOSC1	-	Configure Configuration Word Bit OSCS<2:0> Set T16G Control Register T16GC<3>	
PB0	PB0	-	-	-
	PINT0	1	Set Interrupt Enable Control Register INTC0 <PIE0>	
	N_EPAS1	1	Set TE2 Auto Shutdown Register Bit EPWMAS1	
PB1	PB1	-	-	-
	PINT1	1	Set Interrupt Enable Control Register INTE1 <PIE1>	

Pin	Pin MUX.	PAT	Peripheral Enable	Remarks
PB2	PB2	-	-	-
	PINT2	1	Set Interrupt Enable Control Register INTE1 <PIE2>	
	TE1PWM	0	TE1C<3>=1	
PB3	PB3	-	-	-
	PINT3		Set Interrupt Enable Control Register INTE1 :PIE3=1	
	TE2CI		Set TE2C Control Register TE2M<3:0>	
	TE2CO		Set TE2C Control Register TE2M<3:0>	
	EP1A		Set TE2C Control Register TE2M<3:0> and P1M<1:0>	
PB4	PB4	-	-	-
	N_EPAS0		Set TE2 Auto Shutdown Register Bit EPWMAS0	
PB5	PB5	-	-	-
	EP1B		Set TE2C Control Register TE2M<3:0> and P1M<1:0>	
PB6	PB6	-	-	-
	EP1C		Set TE2C Control Register TE2M<3:0> and P1M<1:0>	
PB7	PB7	-	-	-
	EP1D		Set TE2C Control Register TE2M<3:0> and P1M<1:0>	
PC0	PC0	-	-	-
	AIN7		Set Analog Digital Select Register ADSEL	
PC1	PC1	-	-	-

4. 3 I/O Ports Weak Pull-Up

Pin	0	1	2	3	4	5	6	7
PA	Y	Y	Y	Y	Y	-	Y	Y
PB	Y	Y	Y	Y	Y	Y	Y	Y
PC	N	N	-	-	-	-	-	-

Table 4-2 IO Ports Weak Pull-up

Note: “Y” represents supported, “N” represents not supported.

4. 4 External Interrupt

4. 4. 1 External Port Interrupt (PINT)

4 I/O ports have interrupt capability. Each interrupt is enabled by the corresponding bit of the PIE<3:0>. PEG selects rising edge or falling edge as the triggering edge. Occurance of an interrupt will assert the corresponding interrupt flag PIF<3:0>.

Pin	Interrupt	Interrupt Enable	Port Input	Trigger Selection	Interrupt Flag
PB0	PINT0	PIE0	PINT0	PEG	PIF0
PB1	PINT1	PIE1	PINT1	PEG	PIF1
PB2	PINT2	PIE2	PINT2	PEG	PIF2
PB3	PINT3	PIE3	PINT3	PEG	PIF3

Table 4-3 External Port Interrupt

4. 4. 2 External Key Interrupt (KINT)

8 I/O ports have key interrupt capability. When the external key interrupt is enabled, if the current voltage is different from the voltage of last read/write operation, an interrupt will then occur.

KIEx is the external key interrupt enable bit and KIFx is the external key interrupt flag bit.

Prior to clearing a KIF, it is necessary to read/ write all enabled external key input ports to make sure that the unequal condition no longer exists; otherwise, the KIFx cannot be cleared.

Pin	Interrupt	Interrupt Enable	Input	Interrupt Flag
PA0	KINT0	KIE0	KIN0	KIF0
PA1	KINT1	KIE1	KIN1	KIF1
PA2	KINT2	KIE2	KIN2	KIF2
PA3	KINT3	KIE3	KIN3	KIF3
PB4	KINT4	KIE4	KIN4	KIF4
PB5	KINT5	KIE5	KIN5	KIF5
PB6	KINT6	KIE6	KIN6	KIF6
PB7	KINT7	KIE7	KIN7	KIF7

Table 4-4 External Key Interrupt

4. 5 Special Function Register

Reg. Name	Port A/ Port B Register(PA/PB)		
Address	PA：005_H 105_H PB：006_H 106_H		
Reset value	xxxx xxxx		
Px<7:0>	bit7-0	R/W	PA/ PB voltage level 0：Low- level 1：High-level

Reg. Name	Port C Register(PC)		
Address	PC：007_H 107_H		
Reset Value	xxxx xxxx		
Px<1:0>	bit1-0	R/W	Port C voltage level 0：Low-level 1：High-level

Reg. Name	Port A/ Port B Tristate Register(PAT/PBT)		
Address	PAT：085_H 185_H PBT：086_H 186_H		
Reset value	1111 1111		
PxT<7:0>	bit7-0	R/W	PA/ PB input/ output mode select bit 0：Output 1：Input

Reg. Name	Port C Tristate Register(PCT)		
Address	PCT：087_H 187_H		
Reset value	1111 1111		
PxT<1:0>	bit1-0	R/W	PC input/ output mode select bit 0：Output 1：Input

Reg. Name	Port A/ Port B Pull-up Register Register(N_PAPU/N_PBPU)		
Address	N_PAPU：$01A_H$ N_PBPU：$01B_H$		
Reset value	1111 1111		
N_PxPU<7:0>	bit7-0	R/W	PA/ PB weak pull-up enable bit 0：Enable 1：Disable

Chapter 5 Peripherals

5. 1 Timer/ Counter

The HR7P171 features 1 8-bit timer/ counter T8N, 2 8-bit PWM timers T8P1 and T8P2, and 1 16-bit gate timer T16G. Besides, two timers with extended functions TE1 and TE2 are also available.

5. 1. 1 8-bit Timer/ Counter (T8N)

5. 1. 1. 1 Overview

- Clock resource: Fosc/4 or external input clock T8NCKI
- Timer mode and counter mode
- One programmable pre-scaler
- Not available in idle mode
- Counter overflow interrupt

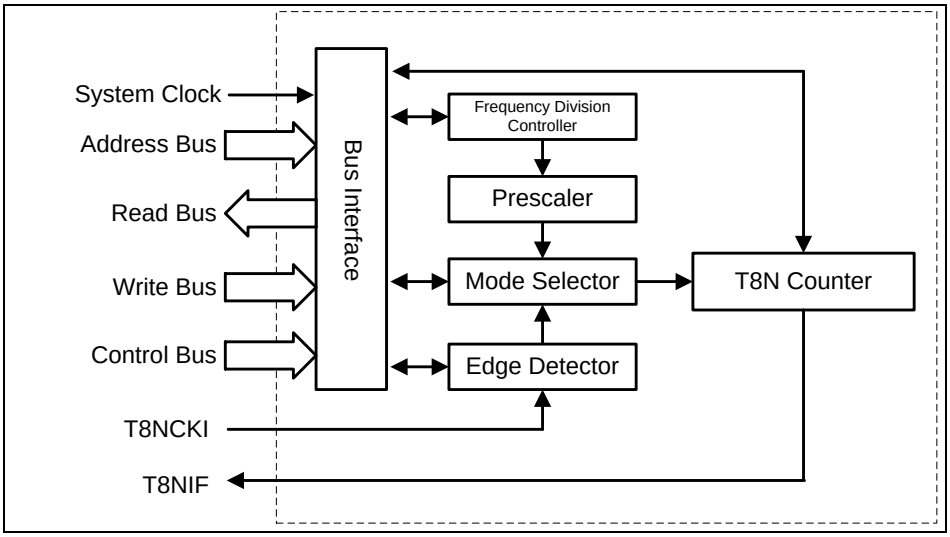


Figure 5-1 T8N Block diagram

5. 1. 1. 2 T8N Operating Mode

The T8NCS bit (BSET<5>) selects the operating mode of T8N.

T8N operates in timer mode by writing T8NCS = 0, clocked by the system clock divided by 4. Without the prescaler, the T8N increment period is one machine cycle. If the prescaler is used, the T8N increment period is the output clock period of the prescaler.

T8N operates in counter mode by setting T8NCS = 1, clocked by an external clock source T8NCKI. The T8NSE bit (BSET<4>) selects on which edge of T8NCKI to increment, rising edge or falling edge. When T8NSE = 0, rising edge is selected. When T8NSE =1, falling edge is selected. T8NCKI is synchronized with the internal phase clock by samling the phase clock p2 and p4, where T8NCKI must maintain high or low for a minimum of 4 system clock cycles.

5. 1. 1. 3 T8N Prescaler

The PSA bit (BSET<3>) can assign the prescaler to T8N. When the prescaler is used by T8N, a write to the T8N register will clear the prescaler counter without changing the prescaler ratio. The prescaler counter value is not readable or writable. The prescaler ratio is configured by the PS<2:0> (BSET<2:0>).

5. 1. 1. 4 T8N Interrupt Flag

An overflow occurs when the T8N counter values transitions from FF_H to 00_H. This asserts the interrupt flag T8NIF (INTF0<2>). If the T8NIE (INTE0<1>) and the global interrupt enable bit GIE are both set, a T8N overflow interrupt will occur; otherwise the interrupt will not be serviced. Prior to enabling this interrupt again, the T8NIF must be cleared to avoid any unexpected interrupt. T8N stops working in idle mode.

5. 1. 2 8-bit PWM Timers (T8P1/T8P2)

5. 1. 2. 1 Overview

- Clock source is system clock frenquency divided by 4(Fosc/4)
- Timer mode
- Configurable prescaler and post-scaler
- Period register supported to store the counter period
- A match signal will be generated if counter value matches period register value, and the counter will be cleared at the same time.
- Extended timer modules support PWM mode

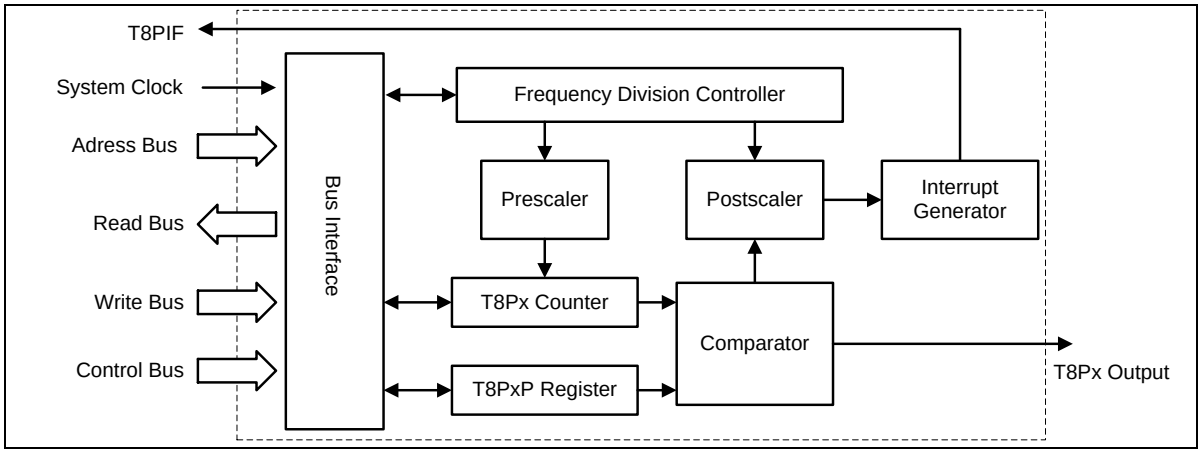


Figure 5-2 T8Px Block Diagram

Note:T8PxP is the period register of T8Px.

5. 1. 2. 2 Operating Mode

T8Px timer mode is clocked by the system clock divided by 4 (Fosc/4). The standard PWM mode and the enhanced timer mode can be implemented by the extended timer modes TE1 and TE2. See Chapter 5.1.4.2 TE1 PWM Mode and 5.1.4.5 TE2 PWM Mode.

5. 1. 2. 3 Prescaler and Postscaler

There are one configurable prescaler and one configurable postscaler supported by T8Px. The prescaler counter is not readable or writable and the prescaler ratio is configured by T8PxPRS<1:0> (T8PxC<1:0>). The postscaler counter is also not readable or writable and the postscaler ratio is configured by T8PxPOS<3:0> (T8PxC<6:3>). Any modification on T8Px control register or T8P control register will clear both prescaler and postscaler counter values.

5. 1. 2. 4 Interrupt Flag

T8Px support one period register and one counter register, and both of them are 8-bit readable/writable registers. A match signal will be generated when the value of T8Px counter reaches to the value of period register. The postscaler will count the match signals, and the T8PxIF will be set to “1” when the post-scaler value reaches the defined value. The T8Px interrupt will occur when T8PIE is enabled and peripheral interrupt (PEIE) and global interrupt (GIE) are also enabled. Otherwise, the interrupt will not be responded. To avoid triggering the interrupt by mistake, T8PxIF should be cleared in software before re-enabling the interrupt. T8Px will not work when CPU is in idle mode, therefore, no interrupt will be triggered in that situation.

Application Example: set T8P1 timer and select prescaler ratio 1:4, post-scaler ratio is 1:1

```
……
BCC     BKSR, RP1
BSS     BKSR, RP0       ; select section1
MOVI    0X30
MOVA    T8P1P           ; set T8P1 timer period
MOVI    0X05
MOVA    T8P1C           ; set prescaler and postscaler
……
```

5. 1. 3 16-bit Timer/Counter (T16G)

5. 1. 3. 1 Overview

- Clock source options: Fosc/4, external clock input T16GCKI or LP oscillator
- Timer mode and counter mode
- Synchronous counter mode and asynchronous counter mode clocked by an external clock source
- Two counters T16GL and T16GH, counting on Fosc divided by 4 or prescaled Fosc output, or external clock edge
- T16G controlled by gate input
- Configurable prescaler
- Overflow interrupt, able to wake up the MCU from idle mode in asynchronous counter mode
- Capture mode supported by TE1 and TE2
- Compare mode supported by TE1 and TE2

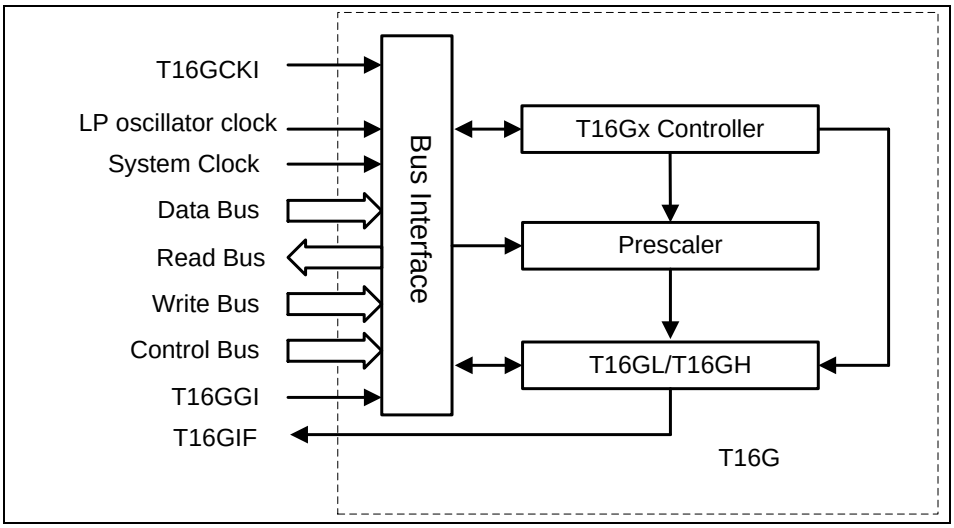


Figure 5-3 T16G Block Diagram

5. 1. 3. 2 T16G Operating Mode

The T16GCS (T16GC<1>) bit selects the operating mode of T16G. In counter mode, the T16GSYN (T16GC<2>) selects the synchronous counter mode or asynchronous counter mode.

1. T16G Timer Mode:

When T16GCS = 0, T16G will work in timer mode, and the clock source of T16G is system clock divided by 4 (Fosc/4).

2. T16G Synchronous Counter Mode

When T16GCS = 1 and T16GSYN = 0, T16G will work in synchronous counter mode. The external clock input T16GCKI needs to be synchronized with Fosc/4, which hence requires the T16GCKI maintain high level or low level for a minimum of 4x Tosc (one machine cycle)..

In synchronous counter mode, if the MCU enters idle mode, T16G will stop counting because the clock synchronous block also enters idle mode.

Note: In synchrounous counter mode, the external clock must maintain high level or low level for a minimum of 1 machine cycle, otherwise the pulse mighe be lost.

3. T16G Asynchronous Counter Mode

When T16GCS = 1 and T16GSYN=1, T16G will work in asynchronous counter mode. T16G asynchronous counter keeps working in idle mode and will generate the interrupt signal on overflow. MCU can wake up by this interrupt.

4. T16G Extended Functions

By working with TE1/TE2, T16G also supports capture mode and compare mode. See 5.1.4.3 T16G Capture Mode and 5.1.4.4 T16G Compare Mode.

5. 1. 3. 3 Oscillator

T16G supports an external LP oscillator. When the device is clocked from an internal clock source without CLKO outout, T16G can be clocked by the LP oscillator by asserting the T16GOSCEN bit. The T16G oscillator frequency is 32KHz.

Note: The clock and the gate input are shared by the same pin, Therefore, when T16G uses the external LP osciilator, gate control is not supported.

5. 1. 3. 4 Gate Control

In counter mode, T16G is controlled by the gate input T16GGI by enabling the T16GGEN (T16GC<6>) bit. The T16GGINV (T16GC<7>) controls the active level of the gate input T6GGI. When T16GGINV = 0, T16G counts on T16GGI low level. When T16GGINV = 1, T16G counts on T16GGI high level

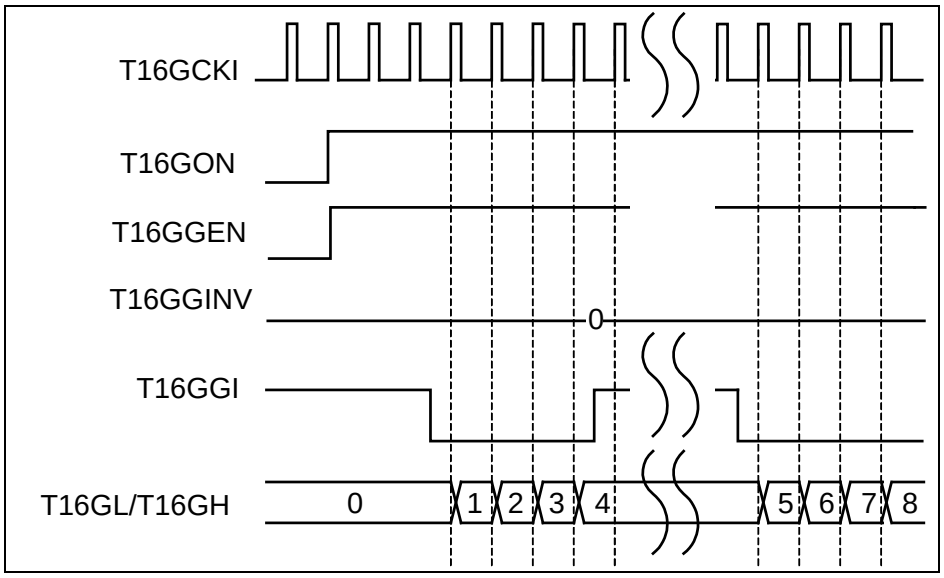


Figure 5-4 T16G Timer Gate Counter

5. 1. 4 Timer/Counter Extension Module (TE)

5. 1. 4. 1 Overview

HR7P171 includes two timer/counter extension modules: TE1 and TE2.

TE1 supports only normal PWM mode with T8Px only.

TE2 supports three extended modes: T16G capture mode, T16G compare mode and T8P1 enhanced PWM (EPWM) mode with T8P1, selected by the TE2M<3:0>.

5. 1. 4. 2 TE1 Standard PWM Mode

When TE1 is configured for PWM mode (TE1PWM and TE2PWM), TE1PWM ports are capable of outputting a 10-bit resolution PWM. On initializing TE1PWM ports, the associated pins must be set to output mode.

T8P1 or T8P2 can be used as the time base for TE1PWM output, selected by the PWMTBS bit of the TE1C register. The PWM period is provided by T8P1 or T8P2. When T8P1 or T8P2 is used as the PWM time base, only the presaler is active while the postscaler is inactive. T8Px counter increments from 0. When it reaches to the T8PxP value, a complete PWM cycle is finished. At this point, the TE1PWM output will be set to 1 (TE1PWM output will not be set if the PWM duty cycle is 0), the TE1L value will be latched to TE1H, and T8Px will be cleared and restart counting up.

The pulse width of TE1PWM is determined by values written to TE1L register and

TE1C<5:4> bits. TE1L and TE1C<5:4> can be written at any time, but the new values written will not be latched into TE1H and resbuf<1:0> until T8PxP=T8Px (i.e., the count cycle is completed). If the TE1PWM pulse width is no less than PWM period, TExPWM port will not be cleared. In PWM mode, TE1H is a read-only register.

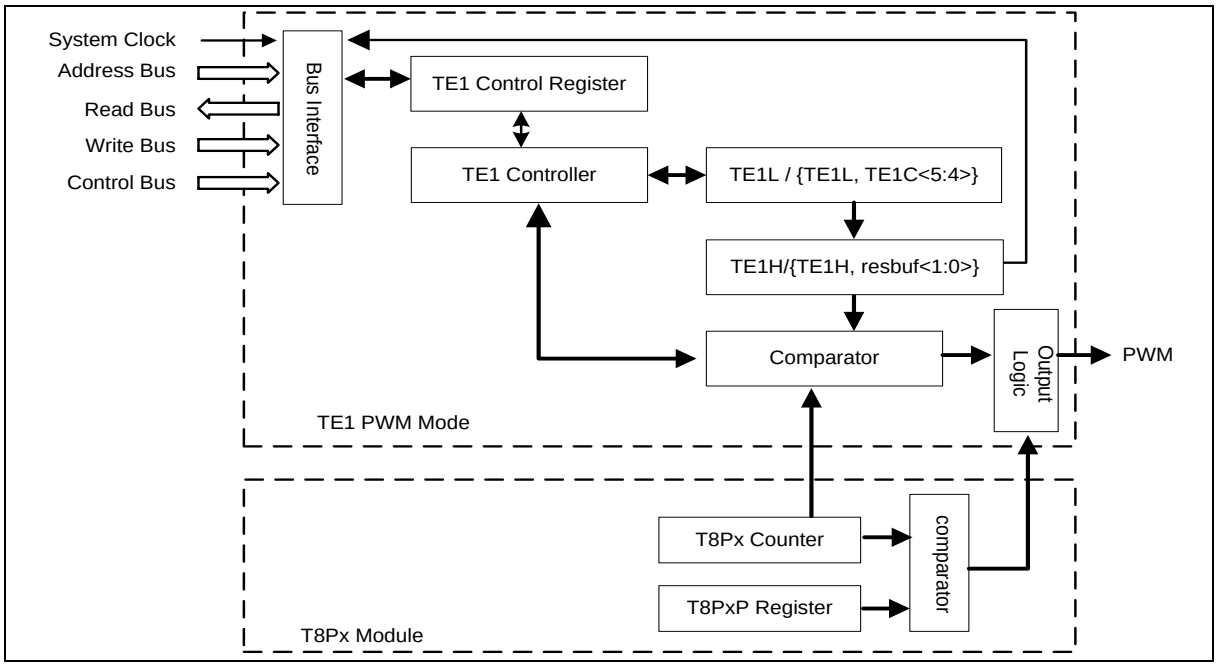


Figure 5-5 TE1 PWM Mode Diagram

PWM output waveform:

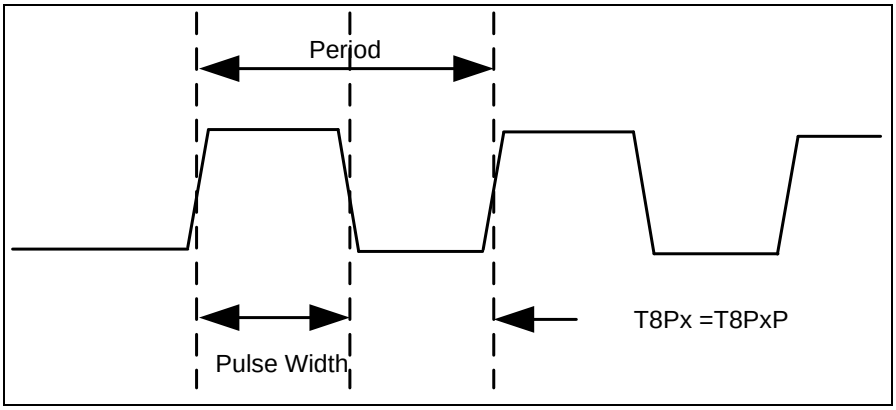


Figure 5-6 PWM Output

When the PWM mode is disabled, the TE1PWM ports will then become GPIOs.

PWM formulas are as follows:

PWM Period = [(T8PxP)+1]×4×Tosc×(T8PxPrescaler Value)

PWM Frequency = 1 / [PWM Period]

PWM Pulse Width =(TE1L:TE1C<5:4>)×Tosc×(T8Px Prescaler Value)

PWM Duty Ratio = (TE1L:TE1C<5:4>)/4[(T8PxP)+1]

The maximum PWM resolution for a given PWM frequency:

$$Resolutison = \frac{\log(\frac{Fosc}{Fpwm * F_{T8PxPRS}})}{\log 2}$$

Where $F_{T8PxPRS}$ is the T8Px prescaler value.

Application Example: to obtain a PWM output with a period of 256us and duty cycle of 50% (system operates at 4MHz)

```
BCC     BKSR,RP1
BCC     BKSR,RP0        ; Select section0
MOVI    0XFF            ; Move 0XFF to A
MOVA    T8P1P           ; Set PWM period
BSS     BKSR, RP0       ; Select section 1
MOVI    0X80            ; Set PWM pulse width
MOVA    TE1L
MOVI    0X0C
MOVA    T8P1C
MOVI    0X08            ; Set T8P1 as PWM time base
MOVA    TE1C
MOVI    0XF7            ;Set PB3 to output
MOVA    PBT
……
```

5. 1. 4. 3 TE2 Capturer Mode

When TE2M<3:0> = 0100 ~ 0111, TE2 is configured for capture mode where TE2 monitors the TE2CI input and T16G operates as a counter. On initializing T16G, it must be configured for timer mode or synchronous counter mode. The pin associated with TE2CI must be set to input mode.

When the capture condition of TE2CI input is true, TE1 will capture the T16G counter value to TE2 register (TE2H: TE2L), and a TE2 interrupt will occur. The interrupt flag must be cleared by software. When the next capture event occurs, if the TE2H: TE2L have not been read, the old captured values will be overwritten by the new ones.

TE2 supports one prescaler, and it is used only when TE2 operates in capture mode. When TE2 is disabled or configured for other modes, the prescaler will be cleared and not be available. However, when the capture condition is changed, the prescaler will not be cleared. Therefore, the prescaler counter value might not be 0 for the first capture after the capture condition has been changed.

Switching between operating modes might trigger a false TE1 interrupt. Thus, the TE2IE must be 0 during switching, and the TE2IF must also be cleared.

TE2 supports 4 capture conditions:

- Capture at every falling edge
- Capture at every rising edge
- Capture at every 4th rising edge
- Capture at every 16th rising edge

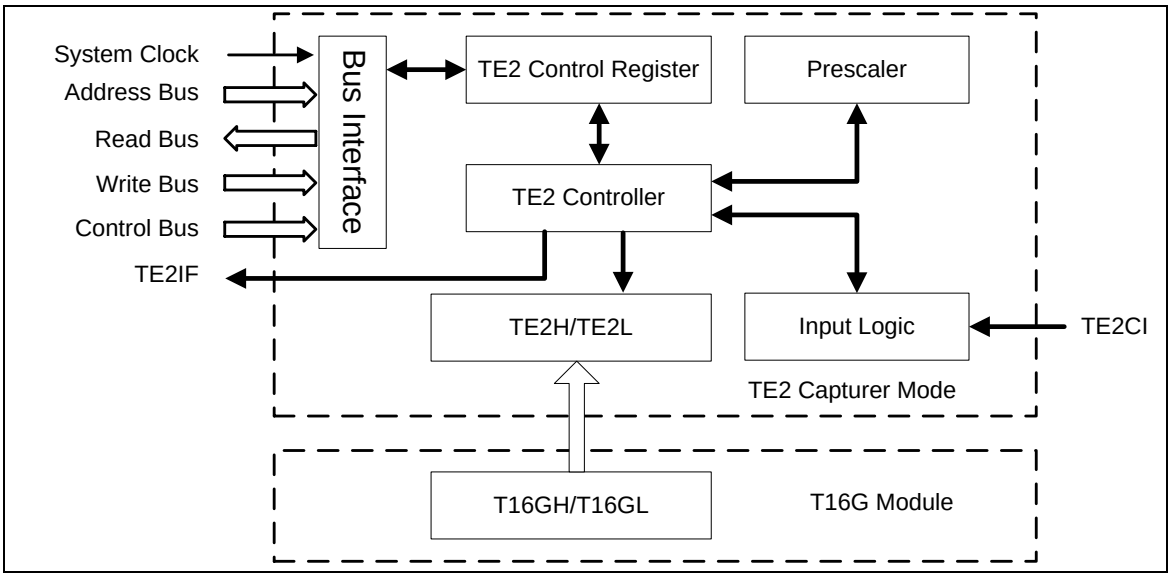


Figure 5-7 TE2 Capture Mode Diagram

5. 1. 4. 4 TE2 Compare Mode

When TE2M<1:0> = 1000 ~ 1011, TE2 is configured for compare mode by working together with T16G. When the T16G counter value reaches TE2 (TE2H:TE2L) value, TE2 will generate a match signal, one of the four match event will occur, and the interrupt flag TE2IF will be set which needs to be cleared by software.

One of the following four events will occur after a match

- Toggle the TE2CO output
- Set the TE2CO output
- Clear the TE2CO output
- TE2CO output no change
- Generate a special event trigger: clear T16G counter

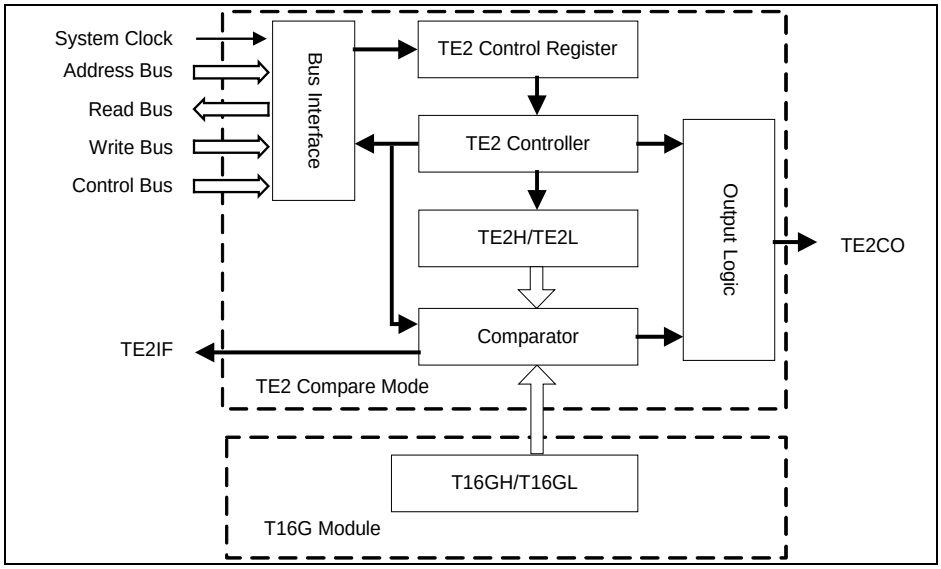


Figure 5-8 TE2 Compare Mode Diagram

5. 1. 4. 5 TE2 Enhanced PWM Mode

When TE2 is configured for the enhanced PWM mode, T8P1 is used as its time base and the output port is selected by the P1M<1:0> bits of the TE2C register.

Single Bridge Output

Single bridge output is standard PWM output, which is the same as the TE1 standard PWM mode described in previous section 5.1.4.2.

Half Bridge Output

In half bridge mode, two ports are used as outputs to drive push-pull load. The PWM output signal is output to EP1A pin, while the complementary PWM output signal is output to the EP2A pin. A programmable dead zone delay can be used to prevent shoot-through current in half bridge power devices. The delay zone delay is determined by the system clock and the TE2PWMC value, expressed by Tdelay = 4 * Tosc * TE2PWMC<6:0>.

In half bridge output mode, PBT<3> and PBT<5> must be cleared to set the corresponding pins to output mode.

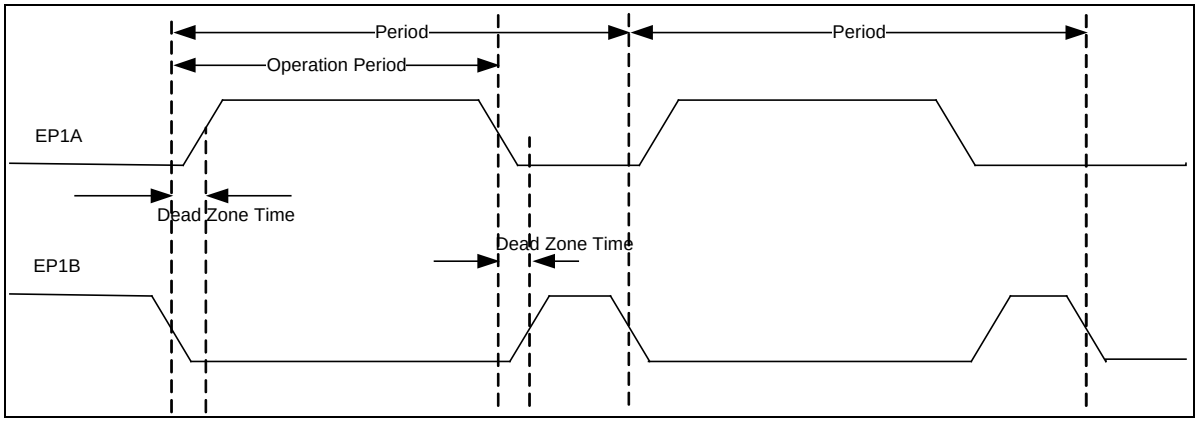


Figure 5-9 Half Bridge Output Diagram

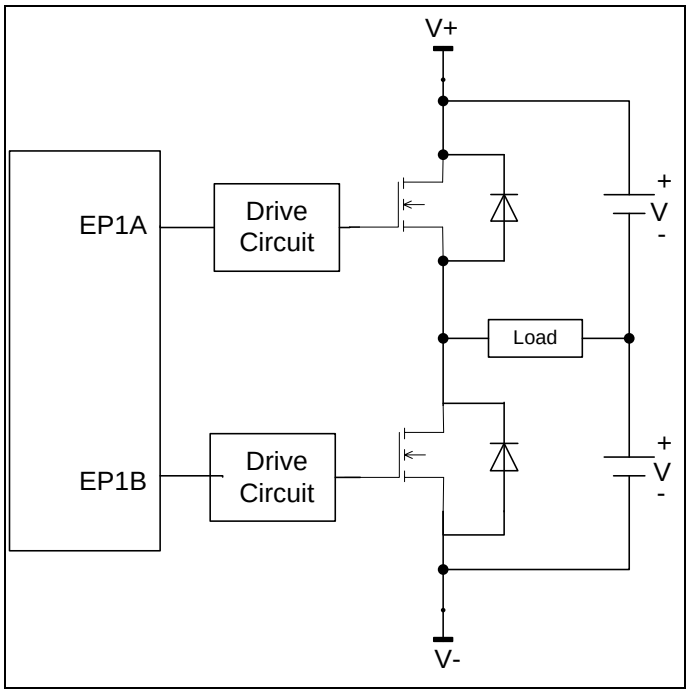


Figure 5-10 Standard Half Bridge Mode Circuit

In half bridge applications, all power devices are turned-on and turned-off by EPWM output. If the two switch transistors are switching simultaneously, they might be both turned on in a very short time, causing a shoot-through current to flow through the transtors. To prevent this from happening, a dead zone delay is used to ensure that one transistor is turned on after the other is completely turned off.

Full Bridge Output

In full bridge mode, four pins are used as outputs. In the forward mode, pin EP1A is driven to its active state and pin EP1D is modulated. In reverse mode, pin EP1C is driven to its active state and pin EP1B is modulated. EP1A/ EP1B/ EP1C/ EP1D are respectively multiplexed with PB<3> and PB<7:5>. PBT<3> and PBT<7:5> must be cleared to set EP1A/ EP1B/ EP1C/ EP1D to output mode..

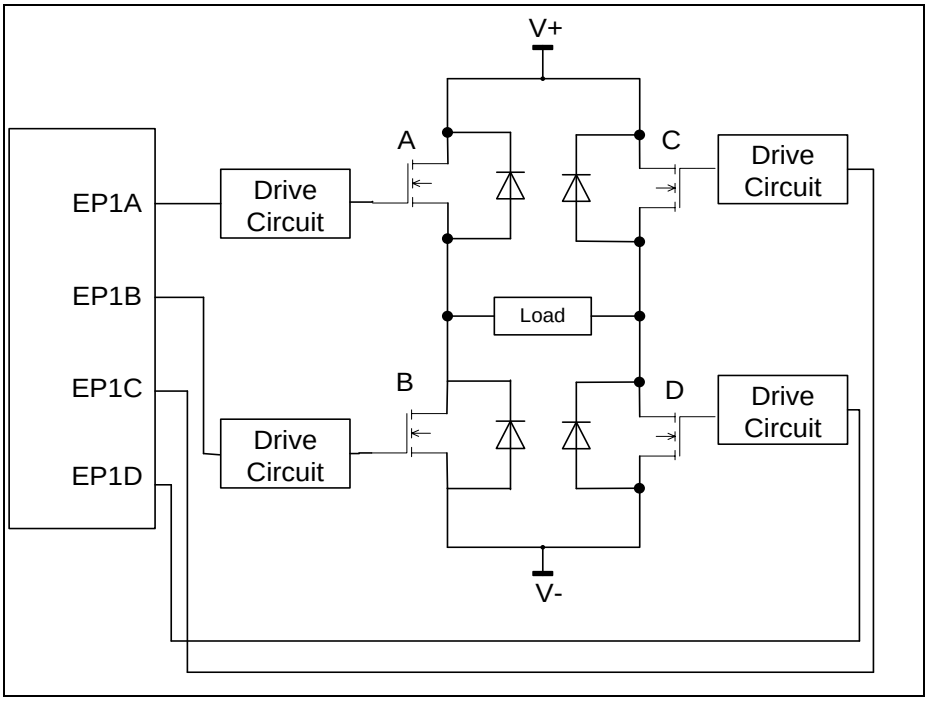


Figure 5-11 Full-Bridge Application Circuit

In full bridge mode, the P1M<1> bit of the TE2C register selects the forward mode or reverse mode. When the software changes this direction control bit, the module will change to the new direction on the next PWM cycle. When the current PWM cycle is complete, the modulated outputs EP1B and EP1D are placed in their inactive state while the unmodulated outputs EP1A and EP1C are switched to drive in the opposite direction. A certain delay must be used between the current cycle and the next new cycle and the delay is determined by 4 * Tosc * (T8P1 Frequency Division Ratio).

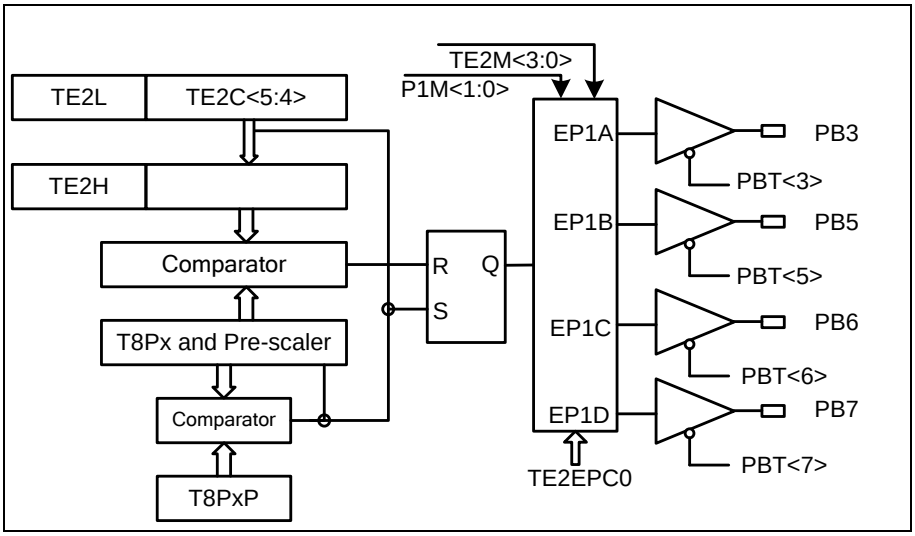


Figure 5-12 EPWM Simplified Block Diagram

EPWM Single-Bridge Output Diagram

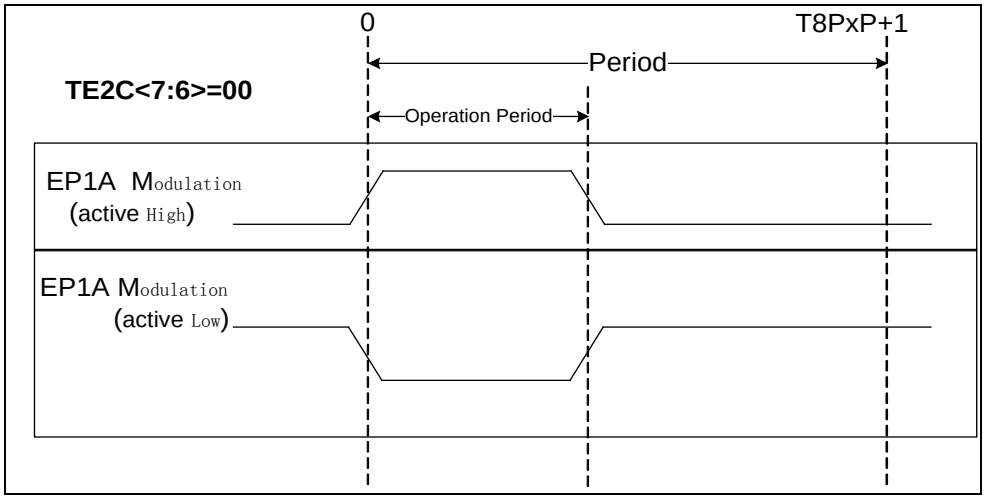


Figure 5-13 EPWM Single-Bridge Output Diagram

EPWM Half-Bridge Output Diagram

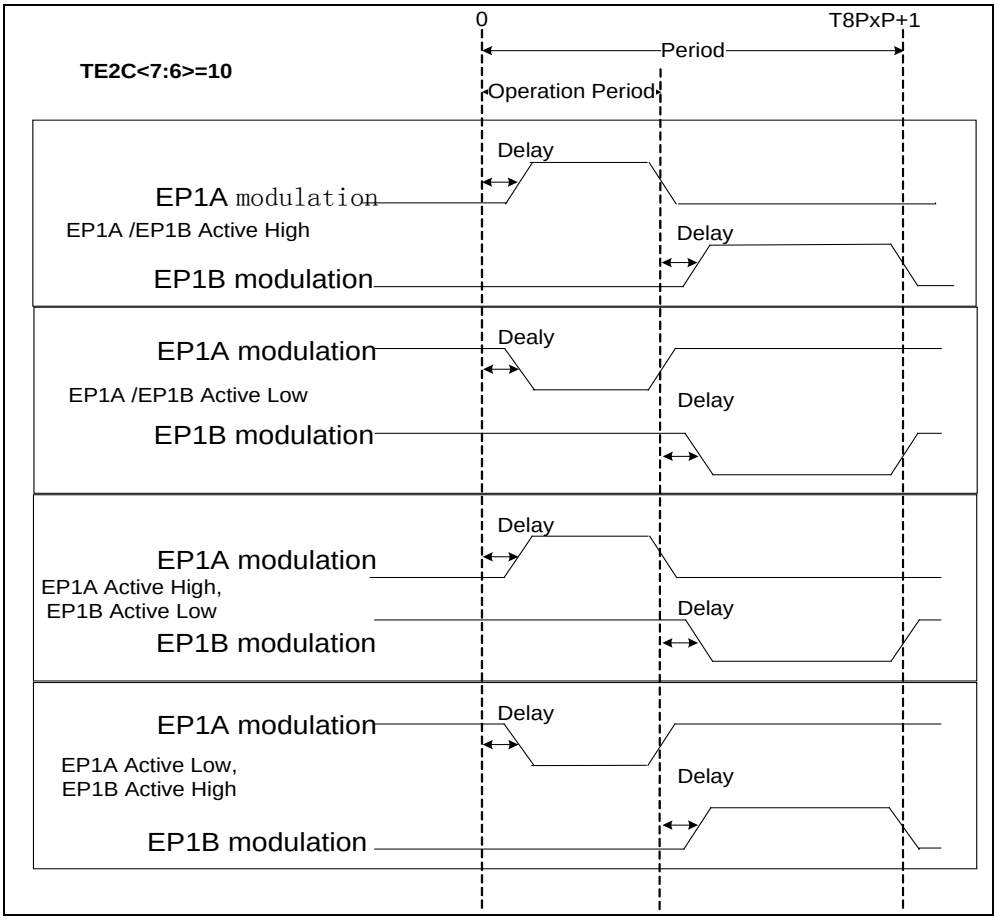


Figure 5-14 EPWM Half-Bridge Output Diagram

Note: The above "Delay" means dead zone delay time determined by 4*Tosc*(PWMC0<6:0>).

EPWM Forward Full-Bridge Output Diagram

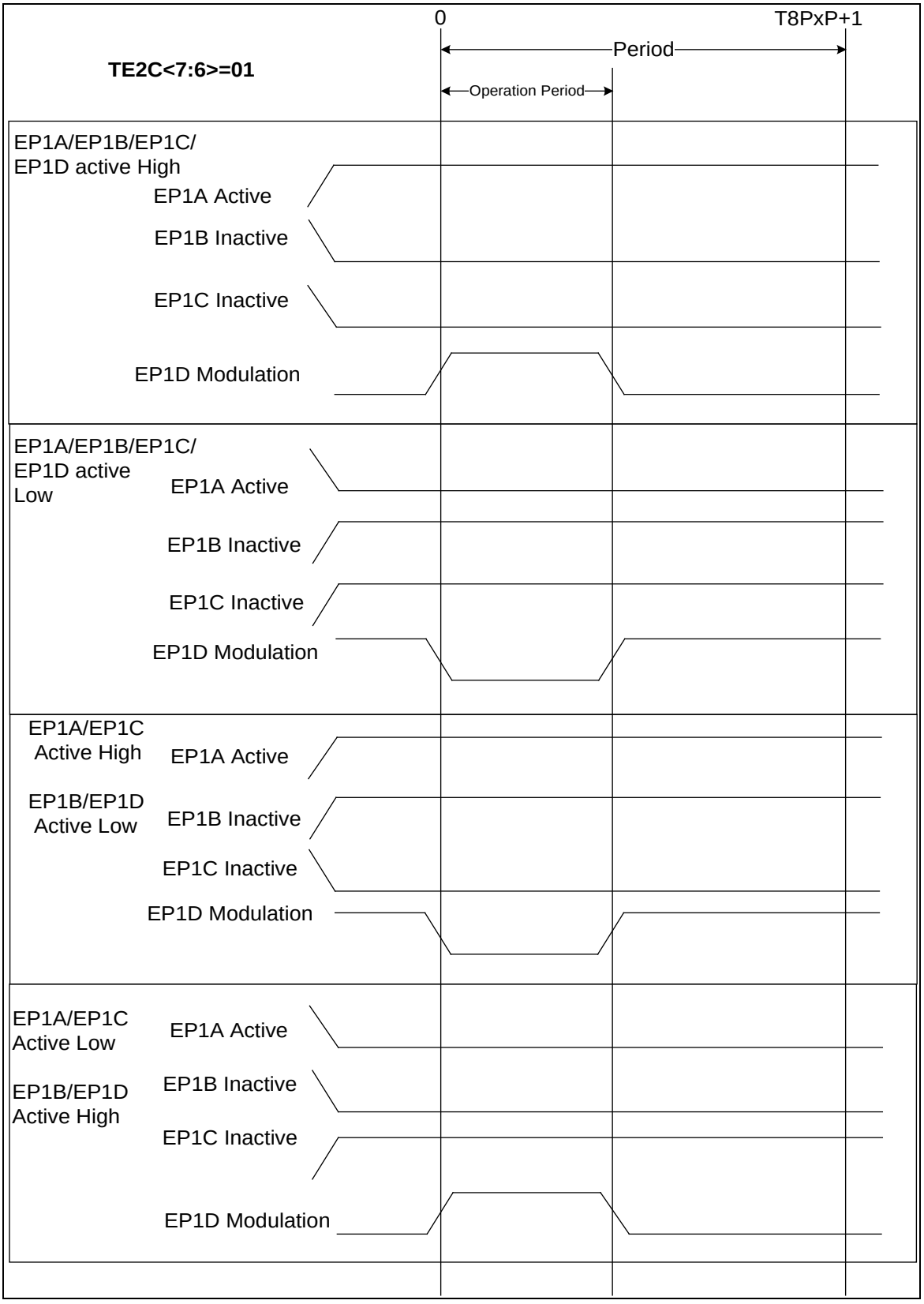


Figure 5-15 EPWM Forward Full-Bridge Output Diagram

EPWM Reserved Full-Bridge Output Diagram

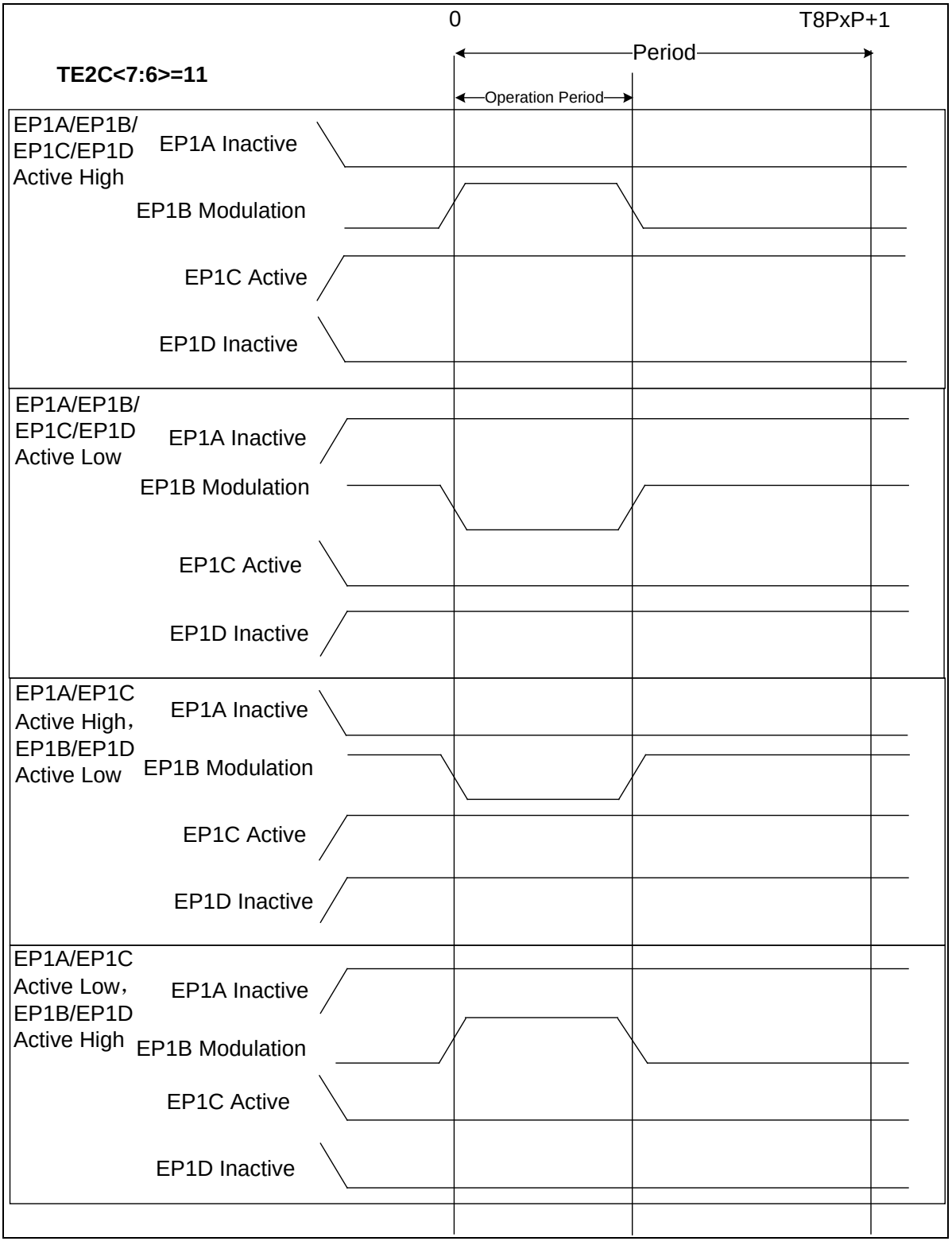


Figure 5-16 EPWM Reverse Full-Bridge Output Diagram

EPWM Auto Shutdown and Restart

An auto shutdown event occurs if the EPWMAS0/ EPWMAS1 is enabled and pin PB0/N_EPAS1 or PB4/N_EPAS0 inputs 0.

When a shutdown event has occurred, the EPWM output pins are placed in shutdown state. The shutdown state of the EPWM output pin can be configured to output 1, 0 or high impedence (tristate). Meanwhile, the shutdown flag bit EPWMASS (TE2AS<7>) is set to 1. If the shutdown event remains, the shutdown flag bit will not be cleared. See the TE2AS register for more detailed decription.

The PRESEN bit (TE2PWMC<7>) can restart EPWM. If the PRSEN = 1, the EPWM function will automatically restart by hardware when the shutdown event ceases. If the PRSEN = 0, for EPWM to restart when the shutdown event ceases, the shutdown flag bit must be cleared by software. After the EPWM restart, it will output normally from the next PWM cycle.

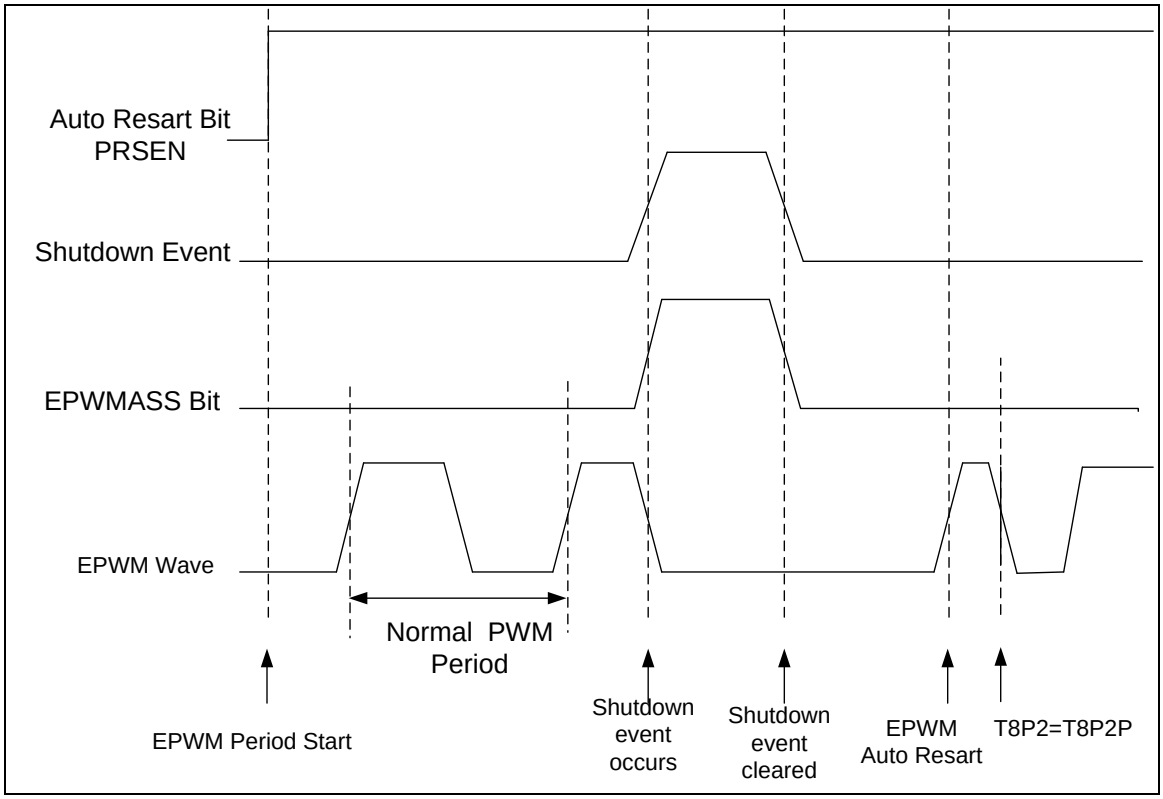


Figure 5-17 EPWM Shutdown and Restart when PRSEN=1

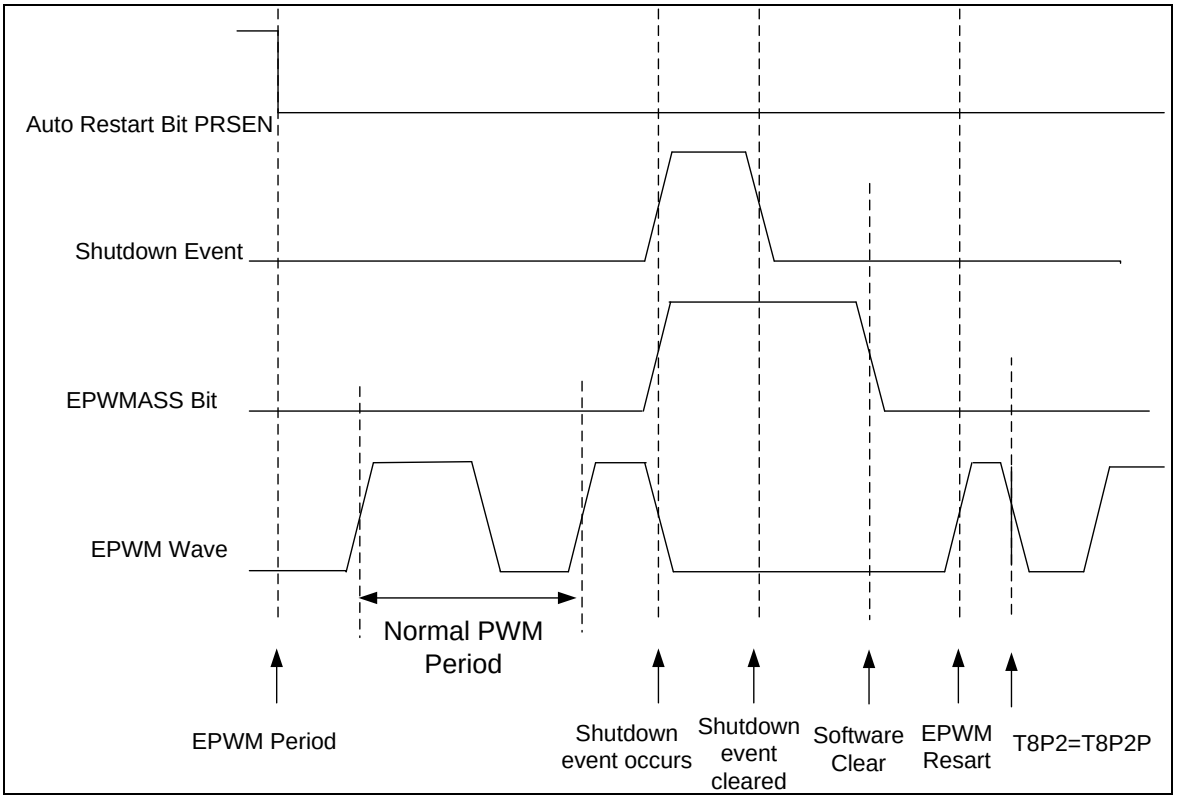


Figure 5-18 EPWM Shutdown and Restart when PRSEN=0

Initialization Considerations

On initializing the EPWM module, set pin EP1A, EP1B, EP1C and EP1D to output mode after initialization is done.

Application Example: to configure TE2 for the EPWM half bridge mode.

```
……
BCC     BKSR,RP0
BCC     BKSR,RP1
MOVI    0XC8
MOVA    T8P1P           ; Set period of EPWM
MOVI    0X32
MOVA    TE2L            ; Configure pluse width of EPWM
MOVI    0X8C
MOVA    TE2C            ; Half-bridge output mode
MOVI    0X8F
MOVA    TE2PWMC         ;Set dead zone delay time,enable automatic restart bit
MOVI    0X40
MOVA    TE2AS           ; Enable auto shutdown on PB0
MOVI    0X05
MOVA    T8P1C           ; Configure prescaler of T8P1, start T8P1
BSS     BKSR, RP0       ; Select section 1
BSS     PBT, 3          ; Set the corresponding PBT to output
BSS     PBT, 5
```

……

5. 1. 5 Special Function Registers

Reg. Name	T8N Register(T8N)		
Address	001_H 101_H		
Reset Value	xxxx xxxx		
T8N<7:0>	bit7-0	R/W	T8N counter 00_H ~ FF_H

Reg. Name	T8Px Register(T8P1, T8P2)		
Address	T8P1=011_H, T8P2=091_H		
Reset Value	xxxx xxxx		
T8Px<7:0>	bit7-0	R/W	T8Px counter 00_H ~ FF_H

Reg. Name	T8Px Period Register(T8P1P, T8P2P)		
Address	T8P1P: $01D_H$ T8P2P: $09D_H$		
Reset Value	1111 1111		
T8PxP<7:0>	bit7-0	R/W	T8Px Period Register 00_H ~ FF_H

Reg.Name	T8P1 Control Register(T8P1C)		
Address	012_H		
Reset Value	0000 0000		
T8P1PRS	bit1-0	R/W	T8P1 prescaler ratio select bits 00: 1:1 01: 1:4 1x: 1:16
T8P1E	bit2	R/W	T8P1 enable bit 0: Disable T8P1 1: Enable T8P1
T8P1POS<3:0>	bit6-3	R/W	T8P1 postscaler ratio select bitS 0000: 1:1 0001: 1:2 0010: 1:3 … 1111: 1:16
EPWMC	bit7	R/W	EPWM output control bit 0：Output EPWM when a first T8P1 match event occurs 1：Always output EPWM

Reg.Name	T8P2 Control Register(T8P2C)		
Address	092_H		
Reset Value	0000 0000		
T8P2PRS <1:0>	bit1-0	R/W	T8P2 prescaler ratio select bits 00: 1:1 01: 1:4 1x: 1:16
T8P2E	bit2	R/W	T8P2 enable bit 0: Disable T8P2 1: Enable T8P2
T8P2POS <3:0>	bit6-3	R/W	T8P2 postscaler ratio select bits 0000: 1:1 0001: 1:2 0010: 1:3 … 1111: 1:16
-	bit7	-	Unused

Reg.Name	T16G Counter Register Low Byte (T16GL)		
Address	$00E_H$		
Reset Value	xxxx xxxx		
T16GL<7:0>	bit7-0	R/W	T16G counter lower 8 bits 00_H ~ FF_H

Reg.Name	T16G Counter Register High Byte(T16GH)		
Address	$00F_H$		
Reset Value	xxxx xxxx		
T16GH<7:0>	bit7-0	R/W	T16G counter higher 8 bits 00_H ~ FF_H

Reg.Name	T16G Control Register(T16GC)		
Address	010_H		
Reset Value	0000 0000		
T16GON	bit0	R/W	T16G enable bit 0:Disable T16G 1:Enable T16G
T16GCS	bit1	R/W	T16G clock source select bit 0: Fosc/4, used in timer mode 1: External clock input T16GCKI (rising edge)
T16GSYN	bit2	R/W	T16G external clock input synchronize bit 0: T16GCS = 1:synchronize with external clock input T16GCS = 0: not used in timer mode 1: T16GCS = 1: do not synchronize with with external clock input T16GCS = 0: not used in timer mode
T16GOSCEN	bit3	R/W	T16G oscillator enable bit 0:Disable T16G Oscillator 1:Enable T16G oscillator (recommded to use only when system clock is in INTOSCIO mode)
T16GPRS <1:0>	bit5-4	R/W	T16G input prescaler ratio select bits 00 = 1:1 01 = 1:2 10 = 1:4 11 = 1:8
T16GGEN	bit6	R/W	T16G gate control enable bit 0: T16GON = 0: don't care T16GON = 1: disable T16G gate control, T16G always counts 1: T16GON = 0: don't care T16GON = 1:enable T16G gate control, T16G counts when gate input T16GGI is active.
T16GGINV	bit7	R/W	T16G gate input level select bit 0: T16G counts on T16GGI input low 1:T16G counts on T16GGI input high

Reg. Name	TE1 Register Low Byte (TE1L)		
Address	097_H		
Reset Value	xxxx xxxx		
TE1L<7:0>	bit7-0	R/W	TE1 register low byte 00_H ~ FF_H

Reg. Name	TE1 Register High Byte(TE1H)		
Address	098_H		
Reset Value	xxxx xxxx		
TE1H<7:0>	bit7-0	R/W	TE1 register high byte 00_H ~ FF_H

Reg. Name	TE1 Control Register(TE1C)		
Address	099_H		
Reset Value	0000 0000		
-	bit2-0	-	Not used
PWMEN	bit3	R/W	TE1 PWM enable bit 0:Disabled 1:Enabled
PWMLSB<1:0>	bit5-4	R/W	10-bit PWM period LSB 2 bits 10 bit resolution: Data LSB<1:0> 8 bit resolution: 00
-	bit6	-	Not used
PWMTBS	bit7	R/W	TE1 PWM time base select bit 0:Select T8P1 as standard PWM time base 1:Select T8P2 as standard PWM time base

Reg. Name	TE2 RegisterLow Byte (TE2L)		
Address	015_H		
Reset Value	xxxx xxxx		
TE2L<7:0>	bit7-0	R/W	TE2 register low byte 00_H ~ FF_H

Reg. Name	TE2 Register High Byte(TE2H)		
Address	016_H		
Reset Value	xxxx xxxx		
TE2H<7:0>	bit7-0	R/W	TE2 register high byte 00_H ~ FF_H

Reg. Name	TE2 Control Register(TE2C)		
Address	017_H		
Reset Value	0000 0000		
TE2M<3:0>	bit3-0	R/W	TE2 operating mode select bits 0000 = Disable TE2 module (to reset TE2) 0010 = Toggle TE2CO output on a match(TE2IF = 1) 0100 = Capture every falling edge (capturer mode) 0101 = Capture every rising edge (capturer mode) 0110 = Capture every 4th rising edge (capturer mode) 0111 = Capture every 16th rising edge (capturer mode) 1000 = Set TE2CO output 1 on a match (TE2IF = 1) 1001 = TE2CO output 0 on a match (TE2IF = 1) 1010 = Software interrupt occurs on a match (TE2IF =1, TE2CO unaffected) 1011 = Trigger a special event when a match is made (reset T16G counter, TE2IF = 1 and TE2CO not affected; or start ADC conversion if ADC conversion is enabled) 1100 = EPWM,EP1A,EP1C active high,EP1B,EP1D active high 1101 = EPWM,EP1A,EP1C active high, EP1B,EP1D active low 1110 = EPWM,EP1A,EP1C active low, EP1B,EP1D active high 1111 = EPWM,EP1A,EP1C active low, EP1B,EP1D active low
EPWMY - EPWMX	bit5-4	R/W	10-bit EPWM period lower 2 bits Capturer mode: not used Comparator mode: not used EPWM mode: 10 bit resolution: Data LSB<1:0>, 8 bit resolution: 00
P1M<1:0>	bit7-6	R/W	EPWM output port select bits When TE2M<3:2> = 00,01,10: xx = EP1A is used as capture input/ compare output, and EP1B/EP1C/EP1D are GPIOs When TE2M<3:2> = 11: 00 = In single bridge mode, EPIA is used as an EPWM output and EP1B/EP1C/EP1D are GPIOs 01 = In full bridge forward mode, EP1D is used as an EPWM output; EP1A is in active state while EP1B/EP1C are in inactive state. 10 = In half bridge mode, EP1A/EP1B are EPWM outputs with dead zone delay and EP1C/EP1D are GPIOs. 11 = In full bridge reverse mode, EP1B is used as an EPWM output; EP1C is in active state while EP1A/EP1D are in inactive state.

Reg. Name	TE2 PWM Control Register(TE2PWMC)		
Address	018_H		
Reset Value	0000 0000		
PDDC<6:0>	bit6-0	R/W	EPWM dead zone delay counter 00_H ~ $3F_H$
PRSEN	bit7	R/W	EPWM restart enable bit 0: Clear the shutdown flag bit in order to restart EPWM after the auto shutdown event ceases. 1: EPWM automatically restart after the auto shutdown event ceases.

Reg. Name	TE2 Auto Shutdown Register(TE2AS)		
Address	019_H		
Reset Value	0000 0000		
PSSBD<1:0>	bit1-0	R/W	Pin EP1B and EP1D shutdown status control bits 00: EP1B and EP1D output '0' 01: EP1B and EP1D output'1' 1X: EP1B and EP1D output tri-state
PSSAC<1:0>	bit3-2	R/W	Pin EP1A and EP1C shutdown status control bits 00: EP1A and EP1C output '0' 01: EP1A and EP1C output '1' 1X: EP1A and EP1C output tri-state
EPWMAS0	bit4	R/W	EPWM auto shutdown bit 0 1: Shutdown when N_EPAS0 inputs 0 0: N_EPAS0 port dose not affect EPWM
-	bit5	-	-
EPWMAS1	bit6	R/W	EPWM auto shutdown bit 1 1: Shutdown when N_EPAS1 inputs 0 0: N_EPAS1 port dose not affect EPWM
EPWMASS	bit7	R/W	EPWM shutdown event flag bit 1: Shutdown event occurred 0: No shut-off event

5. 2 Analog-to-Digital Converter (ADC)

5. 2. 1 Overview

The HR7P171 features a 10-bit AD converter with 8 analog input channels, which converts an analog signal to a corresponding 10-bit signal.

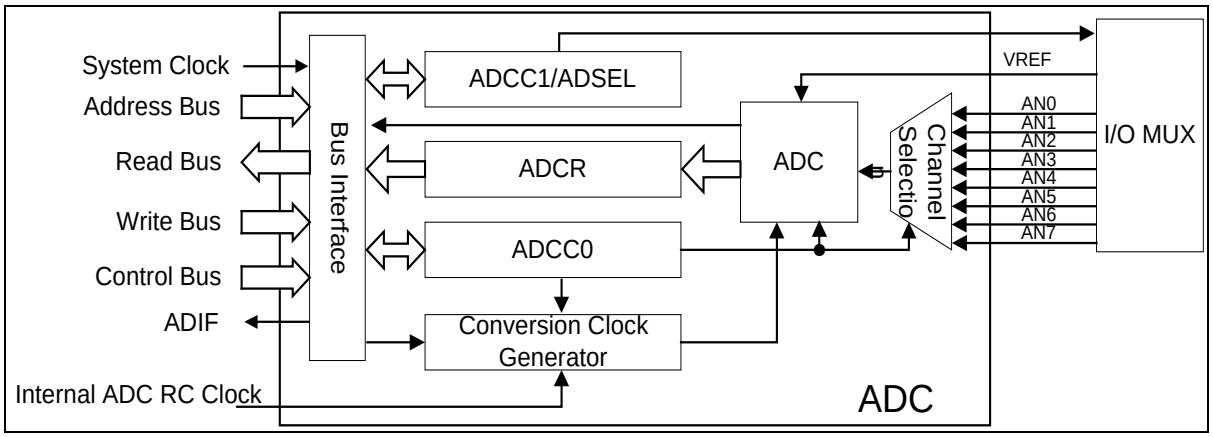


Figure 5-19 ADC Block Diagram

5. 2. 2 Operation Description

The ADC operation procedure is described below using a application example and timing diagrams.

Application Example: A/D conversion program

```
……
BCC   BKSR, RP1
BSS   BKSR, RP0          ; Select section 1
MOVI  0XFE
MOVA ADSEL               ; Set A/D analog input channel
BSS   INTE0, ADIE        ; Enable A/D interrupt
BCC   BKSR, RP0          ; Select section 0
MOVI  0X81               ; Start A/D conversion, select channel 0
MOVA ADCC0               ; PA0 is used as A/D input
BCC   INTF0, ADIF        ; Clear A/D interrupt flag
BSS   INTC0, PEIE_GIEL   ; Enable peripheral interrupt
BSS   INTC0, GIE_GIEH    ; Enable global interrupt
BSS   ADCC0, ADTRG       ; Start A/D conversion
……
```

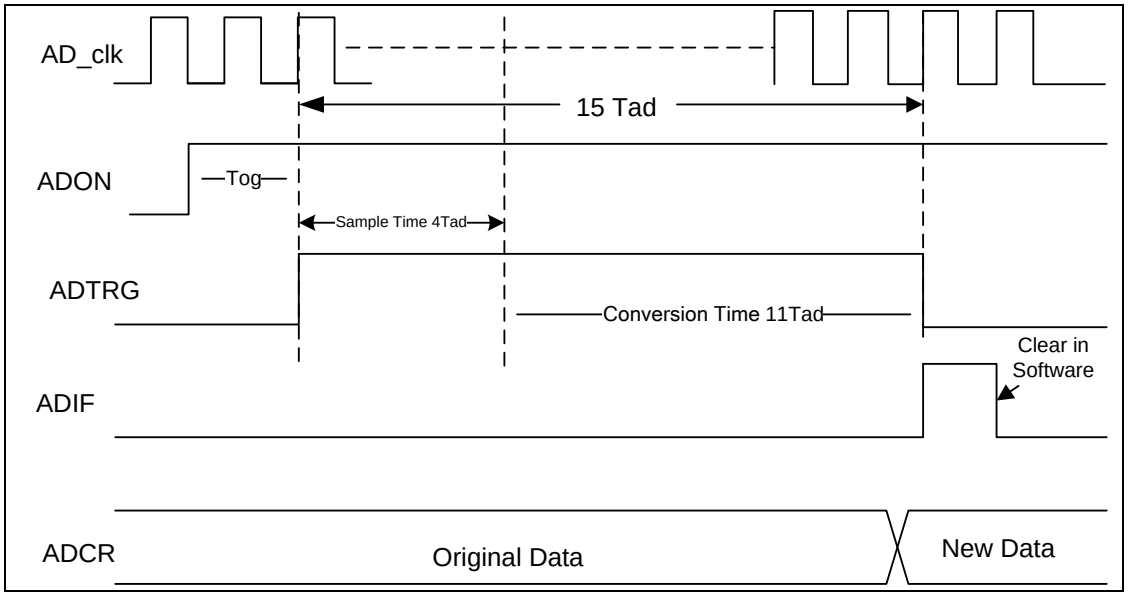


Figure 5-20 ADC Timing Diagram

Note：

1. Tad is clock period of ADC;
2. Tog is the delay time from the ADC enable to ADC start, and it must be greater than 0.

5. 2. 3 Special Function Registers

Reg. Name	ADC Control Register 0(ADCC0)		
Address	$01F_H$		
Reset Value	0000 0000		
ADON	bit0	R/W	A/D conversion enable bit 0: Disable A/D converter 1: Enable A/D converter
-	bit1	-	-
ADTRG	bit2	R/W	A/D conversion status bit 0:A/D conversion completed/not in progress 1:A/D conversion in progress, set this bit to start A/D conversion cycle
ADCHS<2:0>	bit5-3	R/W	A/D analog channel select bits 000 = Channel 0(AIN0) 001 = Channel 1(AIN1) 010 = Channel 2(AIN2) 011 = Channel 3(AIN3) 100 = Channel 4(AIN4) 101 = Channel 5(AIN5) 110 = Channel 6(AIN6) 111 = Channel 7(AIN7)
ADCS	bit7-6	R/W	ADC clock select bits 00 = Fosc/2 01 = Fosc/8 10 = Fosc/32 11 = Internal RC clock(250KHz)

Reg. Name	ADC Control Register 1(ADCC1)		
Address	$09F_H$		
Reset Value	0000 0000		
-	bit5-0	Unused	-
ADVREF	Bit6	R/W	Reference voltage select bit 0: Internal reference voltage VDD 1:External reference voltage VREF
ADFM	Bit7	R/W	10-bit ADC conversion result format select bit 0:ADCRH<7:0>,ADCRL<7:6> 1:ADCRH<1:0>, ADCRL<7:0>

Reg. Name	Analog Digital Select Register(ADSEL)		
Address	$09A_H$		
Reset Value	0000 0000		
ADSEL0	bit0	R/W	AIN0 digital/analog mode select bit 0:Analog mode 1:Digital mode
ADSEL1	bit1	R/W	AIN1 digital/analog mode select bit 0: Analog mode 1: Digital mode
ADSEL2	bit2	R/W	AIN2 digital/analog mode select bit 0: Analog mode 1: Digital mode
ADSEL3	bit3	R/W	AIN3 digital/analog mode select bit 0: Analog mode 1: Digital mode
ADSEL4	bit4	R/W	AIN4 digital/analog mode select bit 0: Analog mode 1: Digital mode
ADSEL5	bit5	R/W	AIN5 digital/analog mode select bit 0: Analog mode 1: Digital mode
ADSEL6	bit6	R/W	AIN6 digital/analog mode select bit 0: Analog mode 1: Digital mode
ADSEL7	bit7	R/W	AIN7 digital/analog mode select bit 0: Analog mode 1: Digital mode

Reg. Name	ADC Result Register Low Byte		
Address	$01E_H$		
Reset Value	xxxx xxxx		
ADCRL<7:0>	bit7-0	R/W	ADC result low byte 00_H ~ FF_H

Reg. Name	ADC Result Register High Byte		
Address	$09E_H$		
Reset Value	xxxx xxxx		
ADCRH<7:0>	bit7-0	R/W	ADC result high byte 00_H ~ FF_H

5. 3 Analog Comparator (ACP)

5. 3. 1 Overview

The HR7P171 features two analog comparators. All compare inputs are multiplexed with I/Os. In addition, the internal reference voltage output can also be a compare input.

5. 3. 2 Operation Description

The analog comparator is used by comparing two analog voltages CxIN+ and CxIN- and providing a digital output CxOUT. When the negative input CxIN- is greater than the positive input CxIN+, logic 0 will be output. When the negative input CxIN- is less than the positive input CxIN+, logic 1 will be output.

The input signal CxIN- and CINP, and output signal COUT can be configured by ACPM<2:0> (ACPC<2:0>) and ACPIS (ACPC<3>). When ACPM<2:0> = 110, C1OUT is output on PA3 and C2OUT is output on PA4.

An interrupt can be generated upon a change in the output value of the comparator. When a change in the output value is detected, and the comparator interrupt enable bits ACPIE (INTE0<3>) and PEIE (INTG<6>) are both set, an interrupt will occur and the interrupt flag bit ACPIF (INTF0<3>) will be set. If the global interrupt enable bit GIE (INTC0<7>) is also enabled, the system will execute the corresponding interrupt service subroutine to handle the interrupt. In idle mode, if the comparator is still active, the interrupt is capable of waking up.

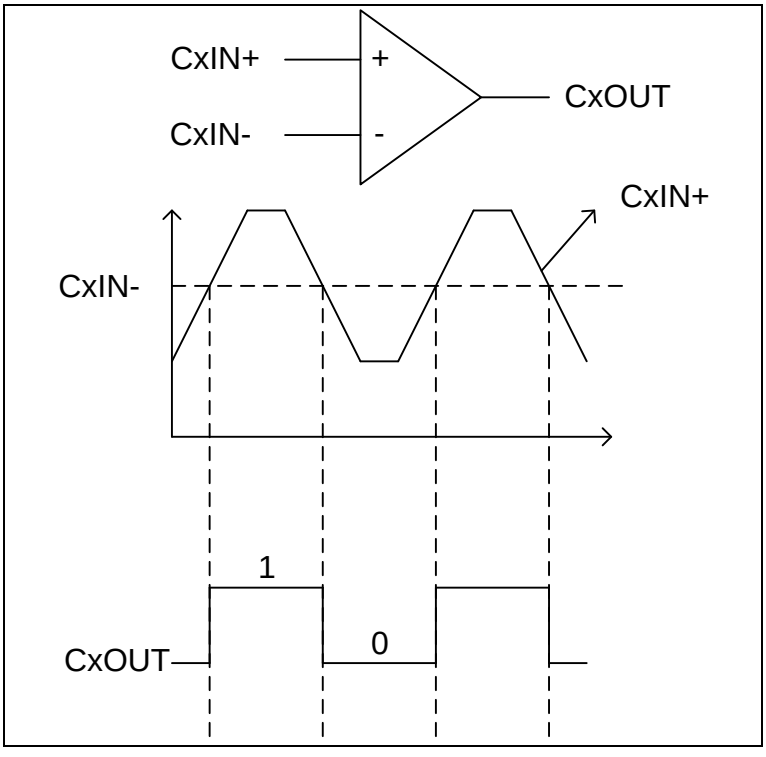


Figure 5-21 Analog Comparator Diagram

5. 3. 3 Special Function Registers

Reg.Name	Analog Compare Control Register (ACPC)		
Address	095_H		
Reset Value	0000 0111		
ACPM <2:0>	bit2-0	R/W	Comparator mode select bits, see following table for details
ACPIS	Bit3	R/W	Comparator input select bit, see following table for details
ACP1INV	Bit4	R/W	Comparator 1 output invert bit 0: Non-inverted C1OUT 1: Inverted C1OUT
ACP2INV	Bit5	R/W	Comparator 2 output invert bit 0: Non-inverted C2OUT 1: Inverted C2OUT
ACP1O	Bit6	R/W	Comparator 1 output bit When ACP1INV=0, 1=C1IN+>C1IN-, 0=C1IN+<C1IN- When ACP1INV=1, 1=C1IN+<C1IN-, 0=C1IN+>C1IN-
ACP2O	Bit7	R/W	Comparator 2 output bit When ACP2INV=0, 1=C2IN+>C2IN-, 0=C2IN+<C2IN- When ACP2INV=1, 1=C2IN+<C2IN-, 0=C2IN+>C2IN-

ACPM<2:0>	ACP1			ACP2		
	C1IN+	C1IN-	C1OUT	C2IN+	C2IN-	C2OUT
000	CIN3	CIN0	OFF	CIN2	CIN1	OFF
001	CIN2	ACPIS = 0(CIN0) ACPIS = 1(CIN3)	ACP1O	CIN2	CIN1	ACP2O
010	VREFACP	ACPIS = 0(CIN0) ACPIS = 1(CIN3)	ACP1O	VREFACP	ACPIS = 0(CIN1) ACPIS = 1(CIN2)	ACP2O
011	CIN2	CIN0	ACP1O	CIN2	CIN1	ACP2O
100	CIN3	CIN0	ACP1O	CIN2	CIN1	ACP2O
101	VSS	VSS	OFF	CIN2	CIN1	ACP2O
110	CIN2	CIN0	PA3	CIN2	CIN1	PA4
111	VSS	VSS	OFF	VSS	VSS	OFF

Note：

1. VREFACP is the output of internal reference voltage module.
2. CxOUT can be read via the ACPxO bit and configured to output to the I/O.

5. 4 Reference Voltage Module

5. 4. 1 Overview

The reference voltage module is a resistance ladder network that provides two selectable reference voltages. The VRC register controls the operation of the reference voltage module.

5. 4. 2 Operation Description

This module can provide 16 levels of reference voltage output.

Application Example: At VDD = 5.0V, set reference voltage to 1.25V.

```
……
BCC     BKSR, RP1
BCC     BKSR, RP0          ; Select section 1
MOVI    0X02
MOVA    ACPC          ; Use reference voltage output VREFACP as analog
                      ; comparator input
MOVI    0XA6          ;
MOVA    VRC           ; Enable reference voltage module, set voltage to 1.25V
……
```

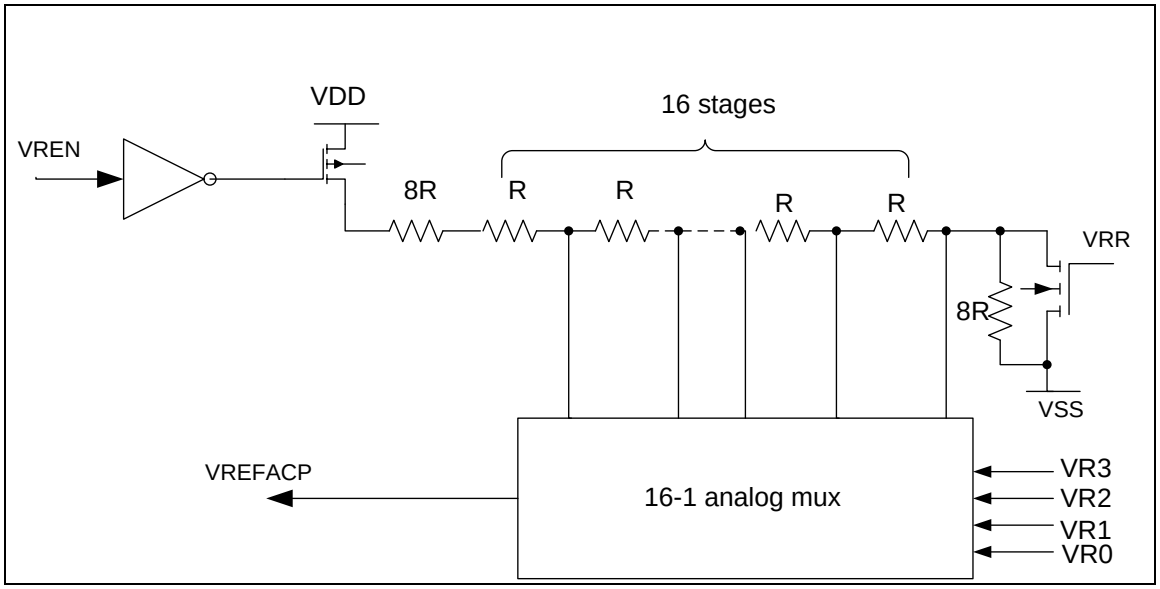


Figure 5-22 Reference Voltage Block Diagram

5. 4. 3 Special Function Register

Reg.Name	Internal Reference Voltage Control Register (VRC)		
Address	096_H		
Reset Value	0000 0000		
VR<3:0>	bit3-0	R/W	VREFACP value select bit VRR = 1: VREFACP =(VR<3:0>/24)×VDD VRR = 0: VREFACP = 1/4×VDD +(VR<3:0>/32)×VDD
-	bit4	-	-
VRR	bit5	R/W	VREFACP range select bit 0:High voltage range 1:Low voltage range
-	bit6	-	-
VREN	bit7	R/W	Internal reference voltage module enable bit 0:Disabled 1:Enabled

Chapter 6 Special Functions and Operations

6. 1 System Clock and Oscillator

6. 1. 1 Overview

The HR7P171 supports two system clock sources: an external clock source (HS, XT, LP, RC, RCIO and EXTCLK mode) and an internal clock source (INTOSC and INTOSCIO mode).

The specific clock source and the corresponding mode can be selected via OSCS <2:0> of the configuration word.

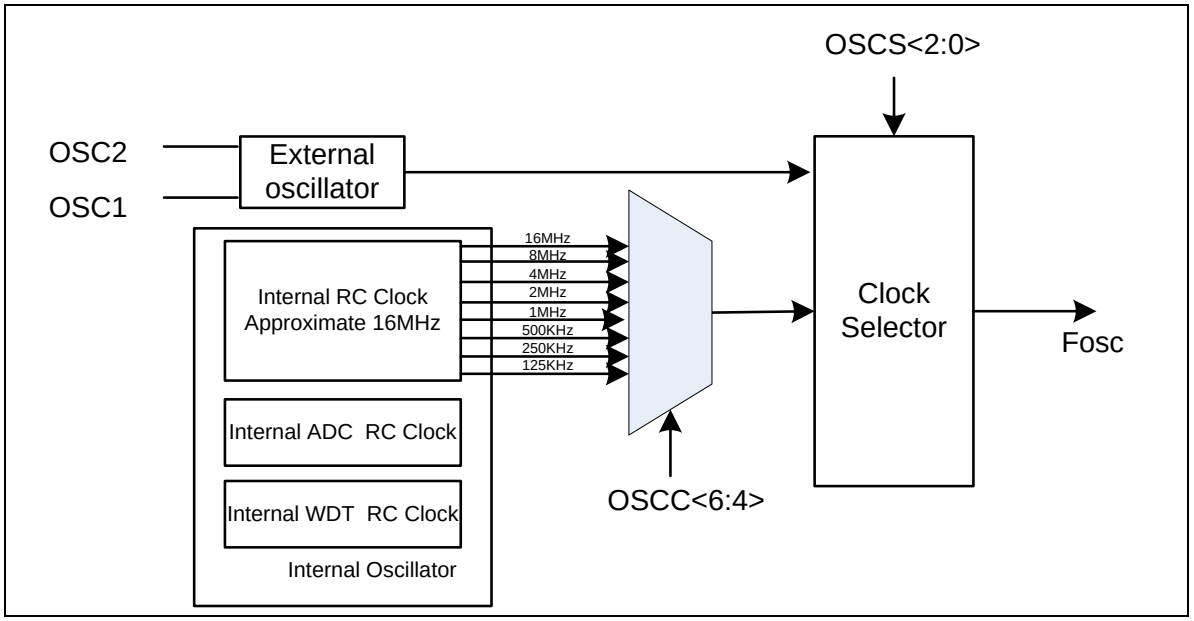


Figure 6-1 System Clock Block Diagram

6. 1. 2 External Oscillator

The external clocks include quartz crystal / ceramic oscillator mode (HS/XT/LP), RC and EXCLK mode. They are described as follows.

6. 1. 2. 1 Crystal/ Ceramic Oscillator (HS/ XT/ LP)

When OSCS<2:0> = 000, the LP mode is selected. When OSCS<2:0> = 010, the HS mode is selected. When OSCS<2:0> = 111, the XT mode is selected.

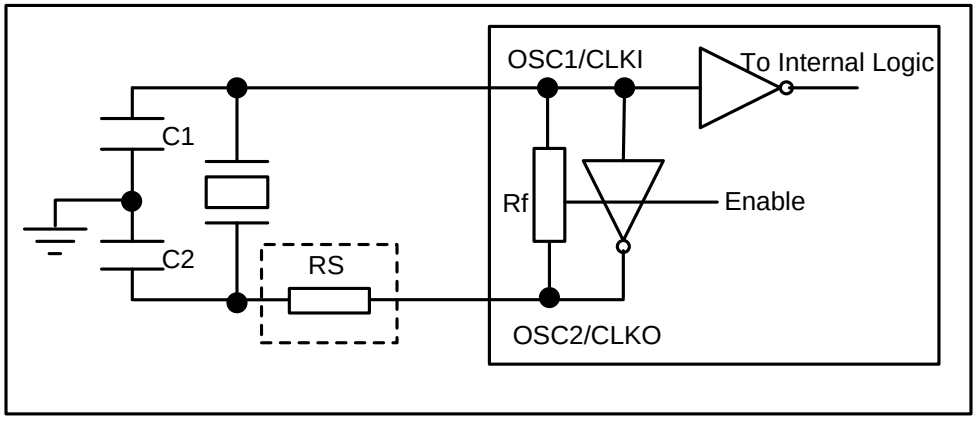


Figure 6-2 Crystal / Ceramic Oscillator (HS/ XT/ LP)

Note：R_S is optional.

Osc Type	OSC frequency	C1*	C2*
LP	32KHz	33pF	33pF
XT	1MHz	15 ~ 33pF	15 ~ 33pF
	4MHz		
HS	8MHz		
	16MHz	15pF	15pF

Table 6-1 Oscillator Capacitor Parameter

Note*: These values can be slightly adjusted depending on the OSC frequency and peripheral circuit.

6. 1. 2. 2 RC Oscillator (RC/RCIO)

The RC mode is selected by setting OSCS<2:0> = 001. The RCIO mode is selected by setting OSCS<2:0> = 110.

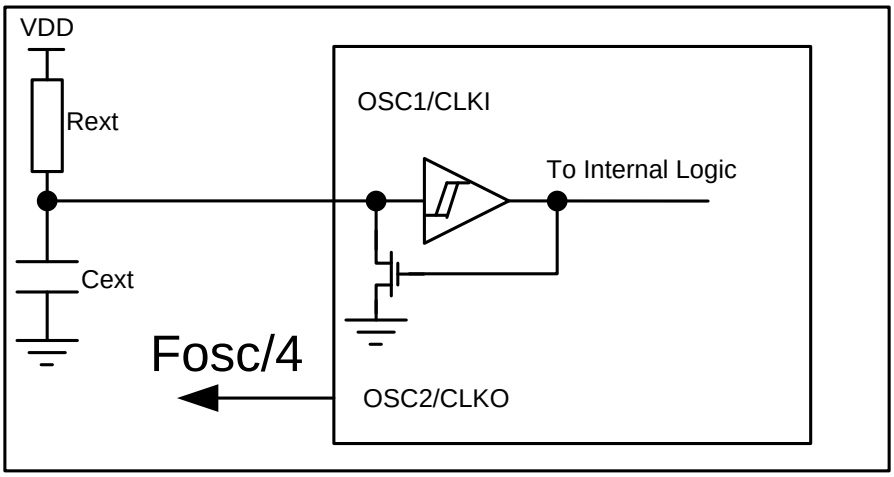


Figure 6-3 Oscillator RC Mode Equivalent Circuit and Peripheral Circuit

	Condition:-40~85℃ 3.0~5.5v
Recommended external resistance	15k≤Rext≤100k
Recommended external capacitance	20pf≤Cext≤300pf
Recommended oscillator frequency	10kHz≤f≤4MHz

Table 6-2 Recommeded Parameters in External RC Mode

6. 1. 2. 3 External Clock

When OSCS<2:0> = 011, the EXCLK mode is selected and the system clock is input on pin PA7/OSC1/CLKI.

6. 1. 3 Internal Clock (INTOS/ INTOSIO)

When OSCS<2:0> = 101, pin OSC1/CLKI and OSC2/CLKO are used as GPIOs.

When OSCS<2:0> = 100, pin CLKO outputs Fosc/4 and pin OSC1/CLKI is used as a GPIO.

If the internal clock source is used, the IRCPRS (OSCC<6:4>) can be used to select a system clock frequency.

The device has already been factory calibrated ±2% under 25℃, VDD = 3.0V~5.5V.

6. 1. 4 Special Function Register

Reg. Name	Internal Clock Calibration Register (CALR)		
Address	013_H		
Reset Value	1111 1111		
CALR<7:0>	bit7-0	R/W	8-bit clock frenquency calibration

Notes: The CALR register is used to tune the internal 16MHz clock. The internal clock has already been factory calibrated to 16MHz under room temperature. Unless there is a special requirement, users do not need to set the register,

Reg. Name	Oscillator Contrl Register (OSCC)		
Address	093_H		
Reset Value	0110 0000		
-	bit3-0	-	-
IRCPRS<2:0>	bit6-4	R/W	Internal clock frequency select bits 111 = 16MHz 110 = 8MHz 101 = 4MHz 100 = 2MHz 011 = 1MHz 010 = 500KHz 001 = 250KHz 000 = 125KHz
-	bit7	-	-

6. 2 Reset Module

6. 2. 1 Overview

There are four reset types:

- ◇ Power-on Reset (POR)
- ◇ Brown-out Reset (BOR)
- ◇ External reset (active low)
- ◇ WDT overflow reset

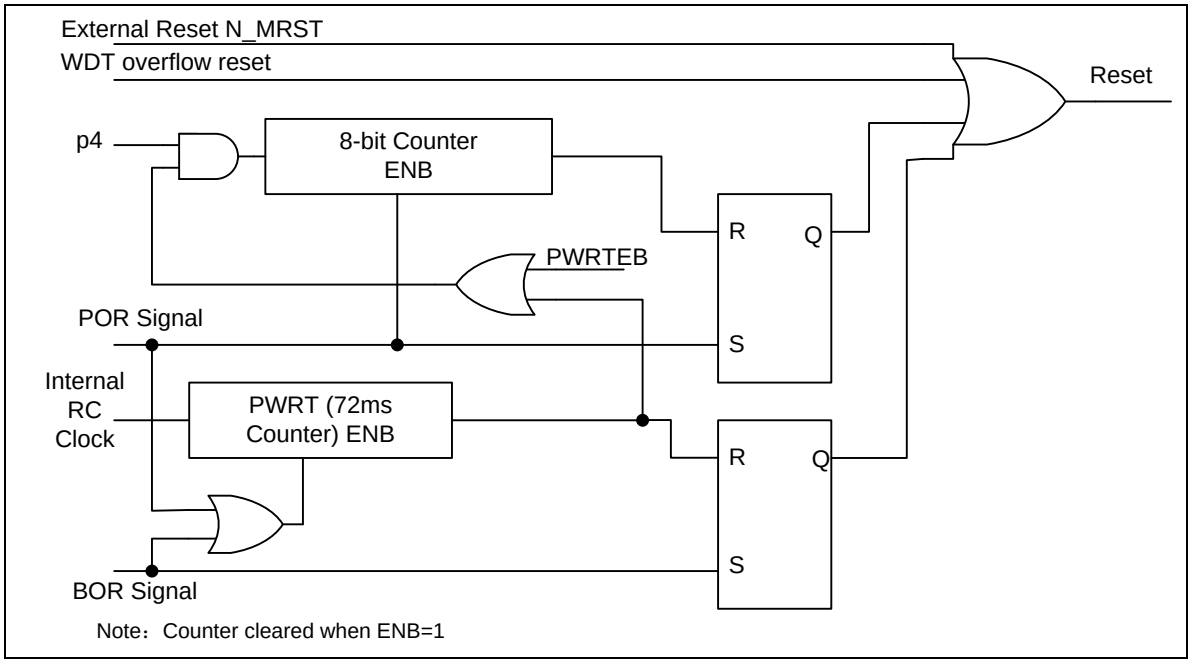


Figure 6-4 Chip Reset Diagram

6. 2. 2 Application Examples

◇ Example 1

In RC reset circuit, 47KΩ≤R1≤100KΩ, capacitor C1 is 0.1μF, R2 is current-limit resistor, 0.1KΩ≤R2≤1KΩ.

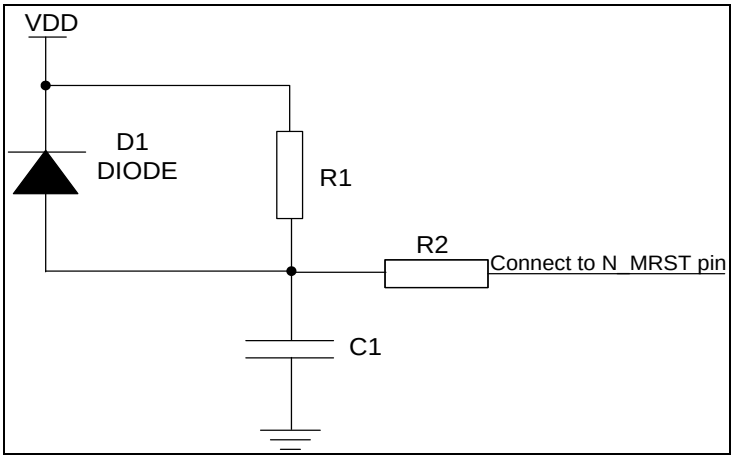


Figure 6-5 RC Reset Circuit

◇ Example 2

In PNP transistor reset, the voltage divided by R1 (2KΩ) and R2 (10KΩ) is used as base input, the emitter is connected to VDD. One route of the collector end is connected to ground through R3 (20KΩ), another is connected to ground through R4 (1KΩ) and C1 (0.1μF). The ungrounded end of C1 is used as input to N_MRST pin.

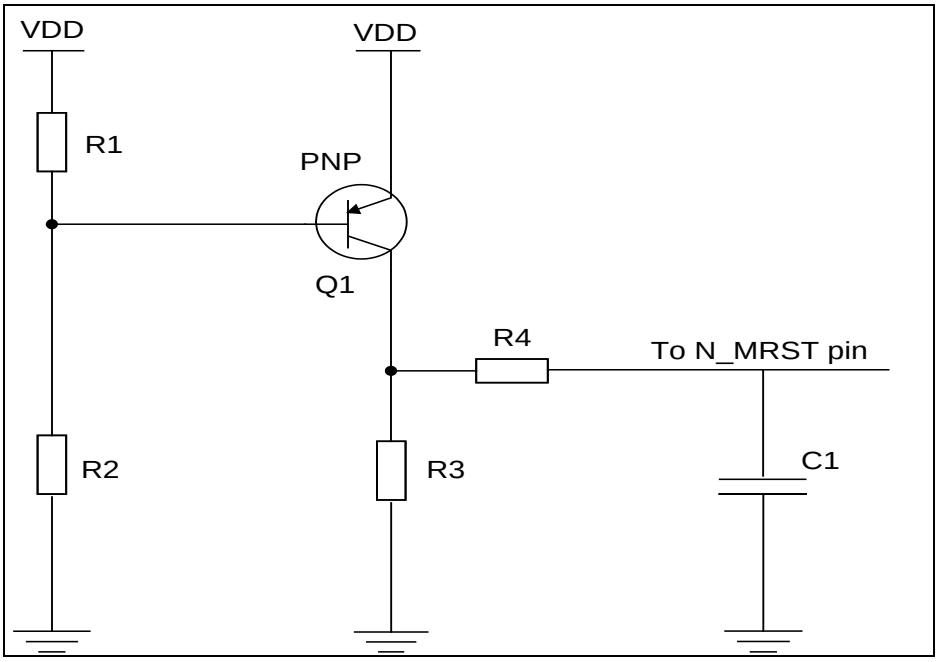


Figure 6-6 PNP Reset Circuit

6. 2. 3 Special Function Register

Reg. Name	Power Control Register (PWRC)		
Address	$08E_H$		
Reset Value	0100 110x		
N_BOR	bit0	R/W	BOR status bit 0: BOR reset occurred (Must be set in software) 1: No BOR reset occurred
N_POR	bit1	R/W	POR status bit 0: POR reset occurred (Must be set to 1 in software) 1: No POR reset occurred
N_PD	bit2	R/W	Power down flag bit 0:Cleared after executing IDLE instruction 1:Set to 1 after POR or executing CWDT instruction
N_TO	bit3	R/W	WDT overflow flag bit 0:Cleared on watchdog overflow 1:Set to 1 after POR or executing CWDT, IDLE instruction
LPMS	bit4	R/W	Low power mode enable bit 0:Idle1 mode 1:Idle0 mode
-	bit7-5	-	-

6. 3 Interrupt Handler

6. 3. 1 Overview

The HR7P171 supports all 20 interrupt sources and 2 interrupt modes: default interrupt mode and vectored interrupt mode, selected by INTVEN0 and INTVEN1.

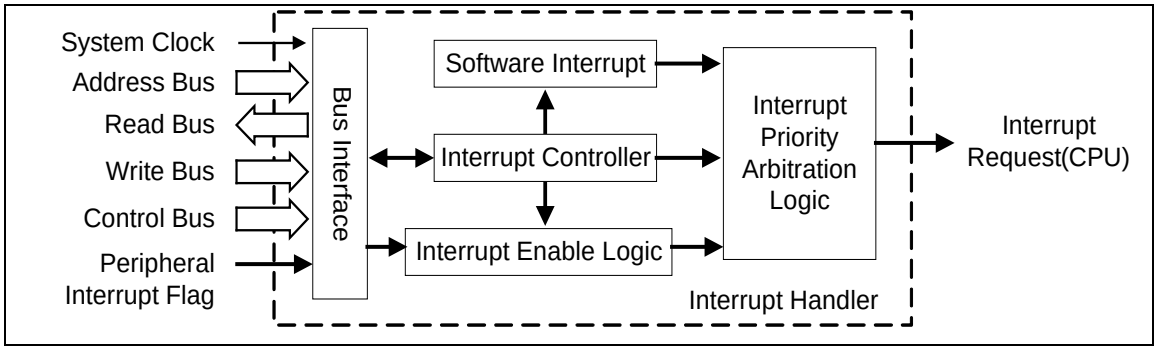


Figure 6-7 Interrupt Control Logic

6. 3. 2 Interrupt Logic Table

No.	Interrupt name	Interrupt flag	Interrupt Enable	Peripheral Enable	Global interrupt enable	Note
1	Software interrupt	SOFTIF	-	-	GIE	-
2	KINT0	KIF0	KIE0	-	GIE	-
3	KINT1	KIF1	KIE1	-	GIE	-
4	KINT2	KIF2	KIE2	-	GIE	-
5	KINT3	KIF3	KIE3	-	GIE	-
6	KINT4	KIF4	KIE4	-	GIE	-
7	KINT5	KIF5	KIE5	-	GIE	-
8	KINT6	KIF6	KIE6	-	GIE	-
9	KINT7	KIF7	KIE7	-	GIE	-
10	PINT0	PIF0	PIE0	-	GIE	-
11	PINT1	PIF1	PIE1	-	GIE	-
12	PINT2	PIF2	PIE2	-	GIE	-
13	PINT3	PIF3	PIE3	-	GIE	-
14	TE2INT	TE2IF	TE2IE	PEIE	GIE	-
15	T8NINT	T8NIF	T8NIE	-	GIE	-
16	T8P1INT	T8P1IF	T8P1IE	PEIE	GIE	-
17	T8P2INT	T8P2IF	T8P2IE	PEIE	GIE	-
18	T16GINT	T16GIF	T16GIE	PEIE	GIE	-
19	ACPINT	ACPIF	ACPIE	PEIE	GIE	-
20	ADINT	ADIF	ADIE	PEIE	GIE	-

Table 6-3 Interrupt Logic Table (Default Interrupt Mode)

No.	Interrupt name	Interrupt flag	Interrupt Enable	Global interrupt enable		Note
1	Software Interrupt	SOFTIF	-			-
2	KINT0	KIF0	KIE0	GIEL	GIEH	IGPx select GIEH/L
3	KINT1	KIF1	KIE1	GIEL	GIEH	IGPx select GIEH/L
4	KINT2	KIF2	KIE2	GIEL	GIEH	IGPx select GIEH/L
5	KINT3	KIF3	KIE3	GIEL	GIEH	IGPx select GIEH/L
6	KINT4	KIF4	KIE4	GIEL	GIEH	IGPx select GIEH/L
7	KINT5	KIF5	KIE5	GIEL	GIEH	IGPx select GIEH/L
8	KINT6	KIF16	KIE6	GIEL	GIEH	IGPx select GIEH/L
9	KINT7	KIF7	KIE7	GIEL	GIEH	IGPx select GIEH/L
10	PINT0	PIF0	PIE0	GIEL	GIEH	IGPx select GIEH/L
11	PINT1	PIF1	PIE1	GIEL	GIEH	IGPx select GIEH/L
12	PINT2	PIF2	PIE2	GIEL	GIEH	IGPx select GIEH/L
13	PINT3	PIF3	PIE3	GIEL	GIEH	IGPx select GIEH/L
14	TE2INT	TE2IF	TE2IE	GIEL	GIEH	IGPx select GIEH/L
15	T8NINT	T8NIF	T8NIE	GIEL	GIEH	IGPx select GIEH/L
16	T8P1INT	T8P1IF	T8P1IE	GIEL	GIEH	IGPx select GIEH/L
17	T8P2INT	T8P2IF	T8P2IE	GIEL	GIEH	IGPx select GIEH/L
18	T16GINT	T16GIF	T16GIE	GIEL	GIEH	IGPx select GIEH/L
19	ACPINT	ACPIF	ACPIE	GIEL	GIEH	IGPx select GIEH/L
20	ADINT	ADIF	ADIE	GIEL	GIEH	IGPx select GIEH/L

Table 6-4 Interrupt Logic Table (Vectored Interrupt Mode)

Note*: In order to avoid the interrupts being triggered by mistake, the interrupt flags should be cleared before enabling corresponding interrupts. All the flags must be cleared in software except read-only interrupt flags. To avoid unsuccessful clearing, it is suggested to check in software whether the clearing is successful. If not, keep clearing until it succeeds.

Application example: to clear a interrupt flag

```
……
BCC     INTC0, T8NIF    ; Clear interrupt flag
JBC     INTC0, T8NIF    ; Check whether the flag has been cleared
GOTO    $-2             ; Clear again if not successful
……
```

6. 3. 3 Default Interrupt Mode

Default interrupt mode is configured for by writing INTVEN = 0. In default interrupt mode, all interrupt vector start addresses are located at 0004_H. Users should check the interrupt flag and interrupt enable bit in interrupt service routine to determine the interrupt source in order to execute the corresponding interrupt service subroutine. Priority configuration is not supported in the default interrupt mode.

6. 3. 4 Vectored Interrupt Mode

Vectored interrupt mode is configured for by setting INTVEN0 and INTVEN1 to 1. In vectored interrupt mode, the software interrupt has the highest priority level and its start addressing is 004_H. Other interrupt sources are divided into 8 groups with their corresponding interrupt start address. The INTP register configures the priority level for each group.

6. 3. 4. 1 Interrupt Vector Groups

There are 19 hardware interrupt sources divided into 8 groups (IG0~IG7). The software interrupt is not in any group.

Interrupt No.	High/Low Priority Select	Interrupt Name	Note
IG0	IGP0	KINT0 ~ KINT7	-
		PINT0	-
IG1	IGP1	T8NINT	-
IG2	IGP2	PINT1 ~ PINT3	-
IG3	IGP3	T8P1INT	-
		T8P2INT	
		T16GINT	-
IG4	IGP4	TE2INT	-
IG5	IGP5	-	-
IG6	IGP6	ADINT	-
		ACPINT	-
IG7	IGP7	-	-

Table 6-5 Interrupt Vector Group Table

6. 3. 4. 2 Interrupt vector allocation table

Priority		0(high)	1	2	3	4	5	6	7	8(low)
Start address		004_H	008_H	$00C_H$	010_H	014_H	018_H	$01C_H$	020_H	024_H
INTV	00	Software interrupt	IG0	IG1	IG2	IG3	IG4	IG5	IG6	IG7
	01		IG0	IG1	IG6	IG7	IG4	IG5	IG2	IG3
	10		IG4	IG5	IG2	IG3	IG0	IG1	IG6	IG7
	11		IG7	IG6	IG5	IG4	IG3	IG2	IG1	IG0

Table 6-6 Interrupt Vector Allocation Table

6. 3. 4. 3 Interrupt Priority Arbitration

First of all, the software interrupt has the highest priority level.

Each group of hardware interrupts can be configured to have high/low priority in order to respond the interrupt nesting. All hardware interrupts can be separated into high or low priority arbitration area by IGPx bit, where each group in its corresponding region are ranked based on the setting of INTV<1:0> and the group with the highest priority is first serviced. The high and low priority arbitration regions are respectively enabled by the high priority interrupt enable bit GIE and low priority interrupt enable bit GIEL. During the execution of the low priority interrupt service routine, the nested interrupt with high priority will be serviced first.

6. 3. 5 Context Saving

Context saving during interrupts is a very important part of interrupt program.

The PUSH and POP instructions in instruction set could save and restore the current operation status very easily. The register A, B, PSW, PCRH and BKSR have their own two level shadow registers: AS1, BS1, PSWS1, PCRHS1, BKSR1 and AS0, BS0, PSWS0, PCRHS0, BKSR0, which are used to save and restore the corresponding registers. Shadow registers have no physical addresses, and they can only save and restore with PUSH and POP instructions.

6. 3. 6 Special Function Registers

Reg. Name	Interrupt Control Register 0(INTC0)		
Address	$00B_H$ $08B_H$ $10B_H$ $18B_H$		
Reset Value	0000 0000		
-	bit0	-	-
PIF0	bit1	R/W	External port interrupt 0 flag bit 0: No interrupt signal on external port PINT0 1: Interrupt signal on external port PINT0(must be cleared in software)
T8NIF	bit2	R/W	T8N overflow interrupt flag bit 0: T8N did not overflow 1:T8N overflew (must be cleared in software)
-	bit3	-	-
PIE0	bit4	R/W	External port interrupt 0 enable bit 0: Disable external port interrupt 0 1: Enable external port interrupt 0
T8NIE	bit5	R/W	T8N overflow interrupt enable bit 0: Disable T8N interrupt 1: Enable T8N interrupt
PEIE_GIEL	bit6	R/W	Peripheral interrupt enable bit/low priority interrupt enable bit 0: Disable peripheral interrupt/disable low priority interrupt 1: Enable unmasked peripheral interrupt/enable low priority interrupt
GIE_GIEH	bit7	R/W	Global interrupt enable bit/high priority interrupt enable bit 0: Disable all interrupts/disable high priority interrupt 1: Enable all unmasked interrupts/enable high priority interrupt

Reg. Name	Interrupt Control Register 1(INTC1)		
Address	$08F_H$		
Reset value	0000 0000		
INTV<1:0>	bit1-0	R/W	Interrupt vector table select bits, please refer to interrupt vector allocation table below for details
-	bit2	-	-
SOFTIF	bit3	R/W	Software interrupt flag bit 0: No software interrupt occurred 1: Software interrupt occurred
INTVEN0	bit4	R/W	Interrupt vector table and software interrupt enable bit 0: Disable interrupt vector table and software interrupt, interrupt start address at 0004_H 1: Enable interrupt vector table and software interrupt
-	bit7-5	-	-

Reg. Name	Interrupt Enable Register 0(INTE0)		
Address	$08D_H$		
Reset Value	0000 0000		
T16GIE	bit0	R/W	T16G interrupt enable bit 0: Disable T16G interrupt 1: Enable T16G interrupt
T8P1IE	bit1	R/W	T8P1 interrupt enable bit 0: Disable T8P1 interrupt 1: Enable T8P1 interrupt
TE2IE	bit2	R/W	TE2 interrupt enable bit 0: Disable TE2 interrupt 1: Enable TE2 interrupt
ACPIE	bit3	R/W	Analog comparator interrupt enable bit 0: Disable comparator interrupt 1: Enable comparator interrupt
-	bit5-4	-	-
ADIE	bit6	R/W	ADC interrupt enable bit 0: Disable ADC interrupt 1: Enable ADC interrupt
-	bit7	-	-

Reg. Name	Interrupt Enable Regsiter 1(INTE1)		
Address	094_H		
Reset value	0000 0000		
-	bit0	R/W	-
PIE1	bit1	R/W	External port interrupt 1 enable bit 0: Disable external port interrupt 1 1: Enable external port interrupt 1
PIE2	bit2	R/W	External port interrupt 2 enable bit 0: Disable external port interrupt 2 1: Enable external port interrupt 2
PIE3	bit3	R/W	External port interrupt 3 enable bit 0: Disable external port interrupt 3 1: Enable external port interrupt 3
-	bit4	-	-
T8P2IE	bit5	R/W	T8P2 interrupt enable bit 0: Disable T8P2 interrupt 1: Enable T8P2 interrupt
-	bit7-6	-	-

Reg. Name	Interrupt Enable Register 2(INTE2)		
Address	$09C_H$		
Reset value	0000 0000		
KIE0	bit0	R/W	PA0 external key interrupt enable bit 0: Disable external key interrupt 0 1: Enable external key interrupt 0
KIE1	bit1	R/W	PA1 external key interrupt enable bit 0: Disable external key interrupt 1 1: Enable external key interrupt 1
KIE2	bit2	R/W	PA2 external key interrupt enable bit 0: Disable external key interrupt 2 1: Enable external key interrupt 2
KIE3	bit3	R/W	PA3 external key interrupt enable bit 0: Disable external key interrupt 3 1: Enable external key interrupt 3
KIE4	bit4	R/W	PB4 external key interrupt enable bit 0: Disable external key interrupt 4 1: Enable external key interrupt 4
KIE5	bit5	R/W	PB5 external key interrupt enable bit 0: Disable external key interrupt 5 1: Enable external key interrupt 5
KIE6	bit6	R/W	PB6 external key interrupt enable bit 0: Disable external key interrupt 6 1: Enable external key interrupt 6
KIE7	bit7	R/W	PB7 external key interrupt enable bit 0: Disable external interrupt 7 1: Enable external key interrupt 7

Reg. Name	Interrupt Flag Register 0(INTF0)		
Address	$00D_H$		
Reset value	0000 0000		
T16GIF	bit0	R/W	T16G interrupt flag bit 0: No T16G counter overflow 1: T16G counter overflow (must be cleared in software)
T8P1IF	bit1	R/W	T8P1 interrupt flag bit 0: T8P1 did not overflow 1: T8P1 overflew (must be cleared in software)
TE2IF	bit2	R/W	TE2 interrupt flag bit 0: Capture mode: No capture interrupt occurred. Compare mode: No match interrupt occurred. PWM mode: not used 1: Capture mode: capture interrupt occurred (must be cleared in software) Comparator mode: match interrupt occurred (must be cleared in software) PWM mode:not used
ACPIF	bit3	R/W	Analog comparator interrupt flag bit 0: Analog comparator output did not change 1:Comparator output changed(must be cleared in software)
-	bit5-4	-	-
ADIF	bit6	R/W	ADC interrupt flag bit 0: A/D conversion in progress 1: A/D conversion completed(must be cleared in software)
-	bit7	-	-

Reg. Name	Interrupt Flag Register 1(INTF1)		
Address	014_H		
Reset value	0000 0000		
-	bit0	-	-
PIF1	bit1	R/W	External port interrupt 1 flag bit 0: No interrupt signal on external port PINT1 1: Interrupt signal on external port PINT1(must be cleared in software)
PIF2	bit2	R/W	External port interrupt 2 flag bit 0: No interrupt signal on external port PINT2 1: Interrupt signal on external port PINT2(must be cleared in software)
PIF3	bit3	R/W	External port interrupt 3 flag bit 0: No interrupt signal on external port PINT3 1: Interrupt signal on external port PINT3(must be cleared in software)
-	bit4	-	-
T8P2IF	bit5	R/W	T8P2 interrupt flag bit 0: T8P2 didi not overflow 1:T8P2 overflew (must be cleared in software)
-	bit7-6	-	-

Reg. Name	Interrupt Flag Register 2(INTF2)		
Address	$01C_H$		
Reset value	xxxx xxxx		
KIF0	bit0	R/W	PA0 external key interrupt flag bit 0: No level change on external key port PA0 1: Level change on external key port PA0(must be cleared in software)
KIF1	bit1	R/W	PA1 external key interrupt flag bit 0: No level change on external key port PA1 1: Level change on external key port PA1(must be cleared in software)
KIF2	bit2	R/W	PA2 external key interrupt flag bit 0: No level change on external key port PA2 1: Level change on external key port PA2(must be cleared in software)
KIF3	bit3	R/W	PA3 external key interrupt flag bit 0: No level change on external key port PA3 1: Level change on external key port PA3(must be cleared in software)
KIF4	bit4	R/W	PB4 external key interrupt flag bit 0: No level change on external key port PB4 1: Level change on external key port PB4(must be cleared in software)
KIF5	bit5	R/W	PB5 external key interrupt flag bit 0: No level change on external key port PB5 1: Level change on external key port PB5(must be cleared in software)
KIF6	bit6	R/W	PB6 external key interrupt flag bit 0: No level change on external key port PB6 1: Level change on external key port PB6(must be cleared in software)
KIF7	bit7	R/W	PB7 external key interrupt flag bit 0: No level change on external key port PB7 1: Level change on external key port PB7(must be cleared in software)

Reg. Name	Interrupt Priority Register(INTP)		
Address	090_H		
Reset value	0000 0000		
IGP0	bit0	R/W	IG0 interrupt priority 0: Low priority 1: High priority
IGP1	bit1	R/W	IG1 interrupt priority 0: Low priority 1: High priority
IGP2	bit2	R/W	IG2 interrupt priority 0: Low priority 1: High priority
IGP3	bit3	R/W	IG3 interrupt priority 0: Low priority 1: High priority
IGP4	bit4	R/W	IG4 interrupt priority 0: Low priority 1: High priority
IGP5	bit5	R/W	IG5 interrupt priority 0: Low priority 1: High priority
IGP6	bit6	R/W	IG6 interrupt priority 0: Low priority 1: High priority
IGP7	bit7	R/W	IG7 interrupt priority 0: Low priority 1: High priority

Interrupt Vector Allocation Table

Default priority		0(high)	1	2	3	4	5	6	7	8(low)
Entry address		004_H	008_H	$00C_H$	010_H	014_H	018_H	$01C_H$	020_H	024_H
INTV	00	Software interrupt	IG0	IG1	IG2	IG3	IG4	IG5	IG6	IG7
	01		IG0	IG1	IG6	IG7	IG4	IG5	IG2	IG3
	10		IG4	IG5	IG2	IG3	IG0	IG0	IG6	IG7
	11		IG7	IG6	IG5	IG4	IG3	IG2	IG1	IG0

6. 4 Watchdog Timer (WDT)

6. 4. 1 Overview

WDT starts counting when the WDTEN (configuration word CONFIG1<3>) is enabled. To avoid any unexpected WDT overflow reset, the WDT Counter should be cleared periodically in program using CWDT instruction. When WDTEN is disabled, the WDT will stop counting.

WDT supports one prescaler to divide the clock source of WDT. The divided clock will be used as the counter clock for WDT. The clock source of WDT is WDT internal RC clock divided by 2, the clock frenquency of WDT RC clock is about 32KHz.

The typical value of WDT counter overflow time at room temperature (25℃) is about 17ms with prescaler ratio 1:1. For WDT counter overflow time in other operation conditions, please refer to Appendix3.2 Characteristics Graphs.

6. 4. 2 Block Diagram

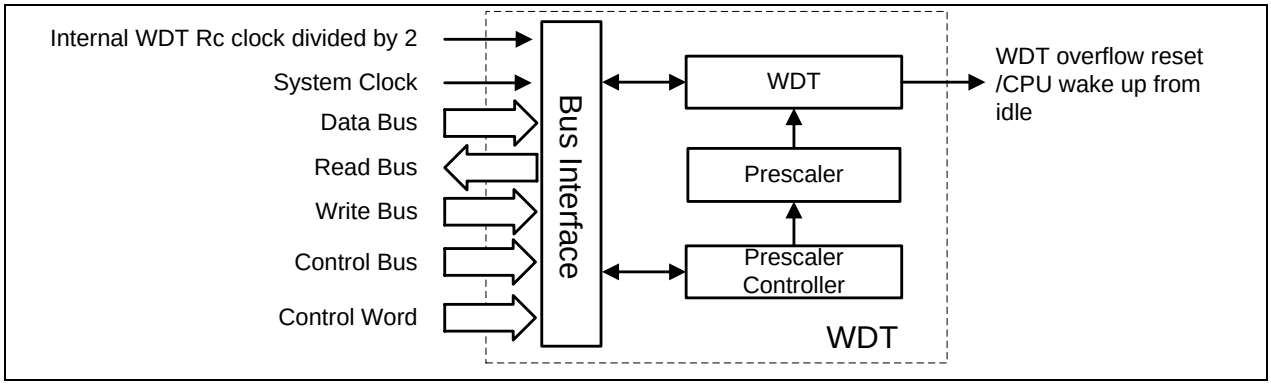


Figure 6-8 WDT Block Diagram

Note: See the BSET register for WDT configuration.

6. 5 Low Power Mode

6. 5. 1 Idle

Two low power modes are available, idle 0 mode or idle 1 mode, selected by LPM bit LPMS (PWRC<4>) .

The idle mode can be entered by executing an IDLE instruction.

- ◇ In idle 1 mode, the clock source stops and the system clock halts
- ◇ In idle 0 mode, the clock source continues to run and the system clock halts
- ◇ All I/Os maintain the status they had before entering idle mode
- ◇ If WDT is enabled, WDT will be cleared but keeps running
- ◇ N_PD bit is cleared and N_TO bit is set.

In idle mode, to avoid switching currents caused by floating inputs, the high-impedance input I/O pins should be pulled-up/down to high/low level. N_MRST pin should be at a logic high level.

6. 5. 2 Wake up

The following wake up sources are able to wake up the device from idle mode.

No.	Wake-up Source	Interrupt Enable	Peripheral interrupt Enable	Note
1	N_MRST	-	-	External reset
2	WDT	-	-	WDT overflow
3	KINT0	KIE0	-	-
4	KINT1	KIE1	-	-
5	KINT2	KIE2	-	-
6	KINT3	KIE3	-	-
7	KINT4	KIE4	-	-
8	KINT5	KIE5	-	-
9	KINT6	KIE6	-	-
10	KINT7	KIE7	-	-
11	PINT0	PIE0	-	-
12	PINT1	PIE1	-	-
13	PINT2	PIE2	-	-
14	PINT3	PIE3	-	-
15	T16GINT	T16GIE	PEIE	Asynchronous Counter mode
16	ACPINT	ACPIE	PEIE	-
17	ADINT	ADIE	PEIE	A/D clock source is internal RC oscillator

Table 6-7 Wake up from Idle Mode

Take note of the following two points when the MCU wakes up from idle mode

1. Wake-up from low power mode is regardless of the status of the global interrupt enable bit. If an interrupt is generated by peripherals, the system will still wake up from the low power mode even if GIE=0 in default interrupt mode. However, the interrupt service routine will not be executed.

2. When an event has occurred, the next instruction following the IDLE instruction is executed after the chip has been running for Twkdly time which is called wake up delay, calculated by Twkdly= (WKDC <7:0>+1) * 4 * Tosc.

When the device wakes up from idle 0, the WKDC register can be written with any value and the minimum wake up delay is 1 machine cycle. When waking up idle 1, a minimum value $0F_H$ is written to the WKDC register, resulting in wake up delay = 16 machine cycles. The default wake up delay is 1024 Tosc.

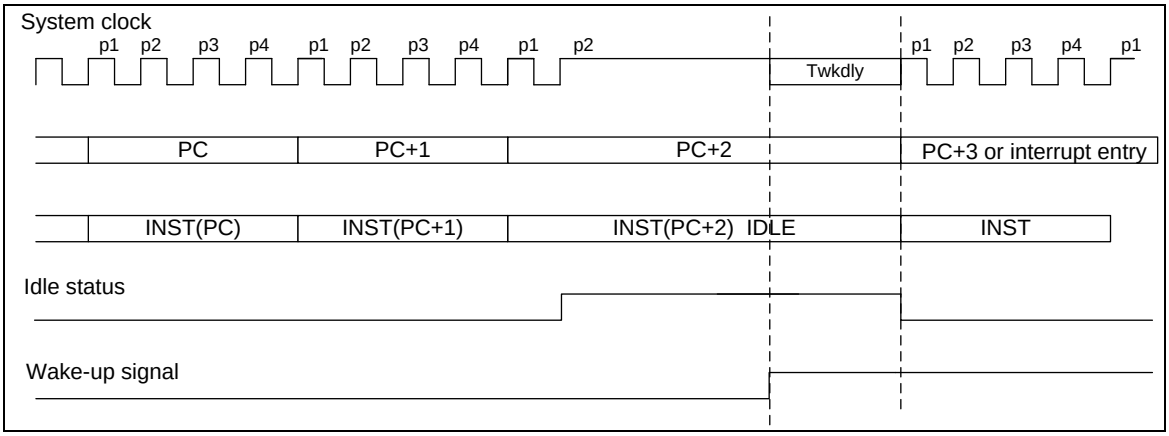


Figure 6-9 Wake up from Idle Mode

6. 5. 3 Special Function Register

Reg. Name	Wake-Up Delay Control Register(WKDC)		
Address	$09B_H$		
Reset Value	1111 1111		
WKDC <7:0>	bit7-0	R/W	Wake up delay control bits WKDC<7:0> = FF_H: the longest …… WKDC<7:0> = 00_H, the shortest

6. 6 Configuration Word

Reg. Name	Configuration Word 1(CONFIG1)	
Address	8001_H	
OSCS <2:0>	bit2-0	Oscillator select bits 000: LP mode: low power crystal is connected to PA6 and PA7 001: RC mode, PA6 is used as CLKO and PA7 is connected to RC 010: HS mode, high speed crystal is connected to PA6 and PA7 011: external clock mode, PA6 is used as I/O and PA7 is used to input system clock 100: INTOSC mode, PA6 is used as CLKO and PA7 is used as I/O 101: INOSCIO mode, PA6 and PA7 are used as I/Os 110: RCIO mode, PA6 is used as I/O and PA7 is connected to RC 111: XT mode, crystal is connected to PA6 and PA7
WDTEN	bit3	Hardware WDT enable bit 0:Disable hardware WDT 1:Enable hardware WDT
N_PWRTEB	bit4	Power-up timer enable bit 0:Enable power-up timer 1:Disable power-up timer
BOREN	bit5	BOR enable bit 0:Disable brown-out reset 1:Enable brown-out reset
N_CP	bit6	Program Encryption enable bit 0:Enabled 1:Disabled
BORVS <1:0>	bit8-7	BOR voltage select bits 11 = 2.1V 10 = 3.5V 01 = 3.8V 00 = 4.2V
-	bit10-9	-
INTVEN1	bit11	Interrupt vector table(priority) enable bit 0:Disabled 1:Enabled
PAES0	bit12	PA port drive strength select bit 0: High drive 1: Low drive
PBES0	bit13	PB port drive strength select bit 0: High drive 1: Low drive
PCES0	bit14	PC port drive strength select bit 0: High drive

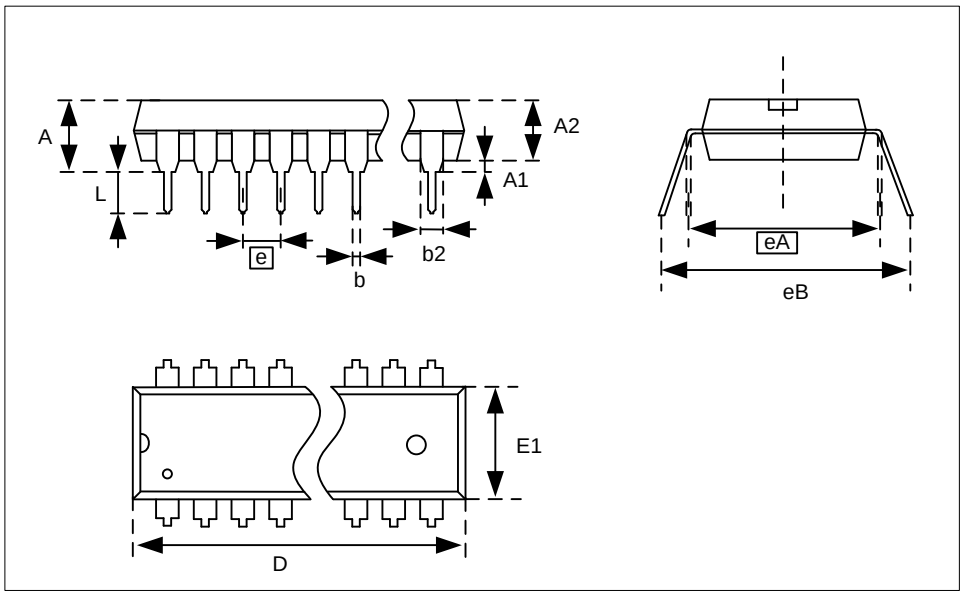
		1: Low drive

Note: Up to 4 high drive ports are supported at a time.

Chapter 7 Packaging Information

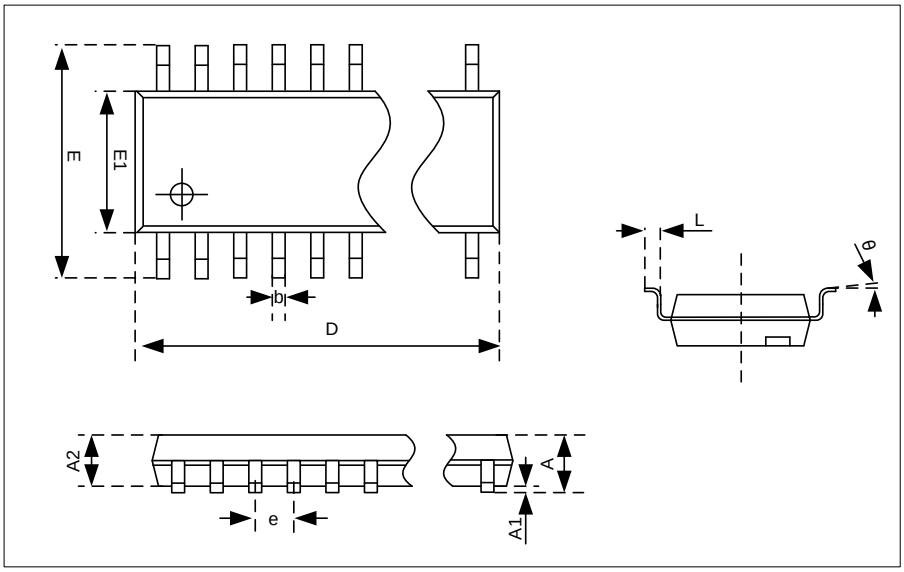
7. 1 20-pin Package Drawing

DIP20



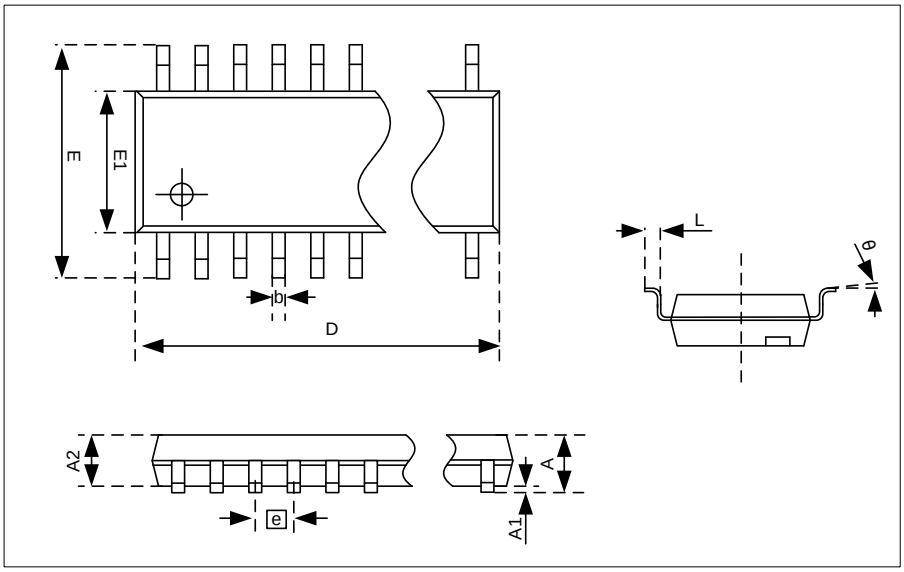
Package: DIP20						
Symbol	(mm)			(inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	4.57	-	-	0.180
A1	0.38	-	-	0.015	-	-
A2	-	3.30	3.56	-	0.130	0.140
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.27	1.52	1.78	0.050	0.060	0.070
D	26.32	26.42	26.52	1.036	1.040	1.044
E1	6.40	6.50	6.65	0.252	0.256	0.262
e	-	2.54	-	-	0.100	-
eA	7.62	-	8.62	0.300	-	0.325
eB	8.38	-	9.65	0.330	-	0.380
L	3.18	-	-	0.125	-	-

SOP20



Package: SOP20						
Symbol	(mm)			(inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.30	2.50	2.70	0.090	0.098	0.107
A1	0.10	0.20	0.30	0.003	0.007	0.012
A2	2.10	2.30	2.50	0.082	0.090	0.099
D	12.60	12.80	13.00	0.496	0.504	0.513
E	10.10	10.30	10.50	0.397	0.405	0.414
E1	7.30	7.50	7.70	0.287	0.295	0.303
b	-	0.40	-	-	0.015	-
e	-	1.27	-	-	0.05	-
L	0.75	0.85	0.95	0.029	0.033	0.038
θ	0°	-	8°	0°	-	8°

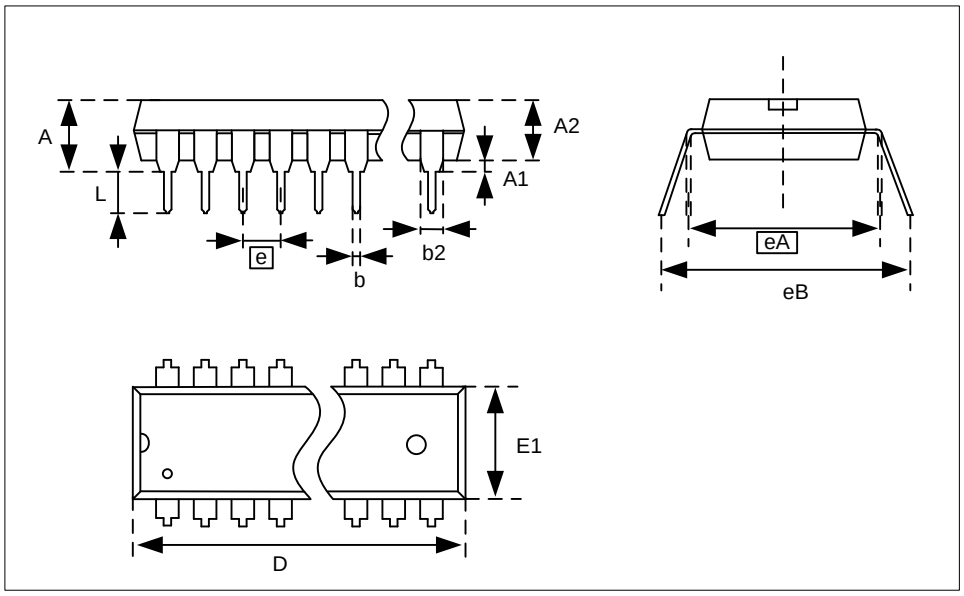
SSOP20



Package: SSOP20						
Symbol	(mm)			(inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.45	1.65	1.85	0.057	0.065	0.073
A1	0.05	0.15	0.25	0.001	0.005	0.010
A2	1.30	1.50	1.70	0.051	0.059	0.067
D	7.00	7.20	7.40	0.275	0.283	0.292
E	7.60	7.80	8.00	0.299	0.307	0.316
E1	7.30	7.50	7.70	0.287	0.295	0.304
b	0.30	0.35	0.40	0.011	0.014	0.016
e	-	0.65	-	-	0.025	-
L	0.80	0.90	1.00	0.031	0.035	0.040
θ	0°	-	8°	0°	-	8°

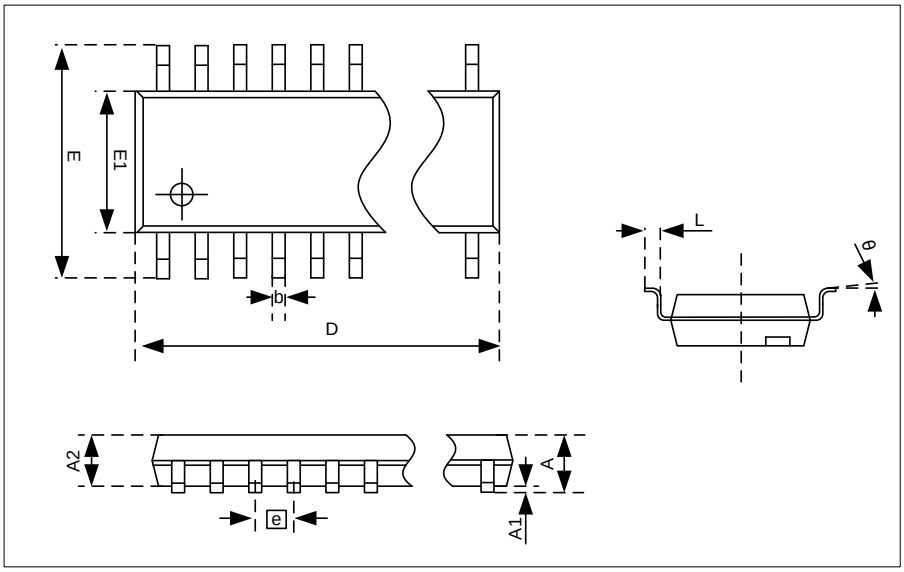
7. 2 18-pin Package Drawing

DIP18



Package：DIP18						
Symbol	(mm)			(inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	4.57	-	-	0.180
A1	0.38	-	-	0.015	-	-
A2	-	3.30	3.56	-	0.130	0.140
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.27	1.52	1.78	0.050	0.060	0.070
D	22.71	22.96	23.11	0.894	0.904	0.910
E1	6.40	6.50	6.65	0.252	0.256	0.262
e	-	2.54	-	-	0.100	-
eA	7.62	-	8.62	0.300	-	0.325
eB	8.38	-	9.65	0.330	-	0.380
L	3.18	-	-	0.125	-	-

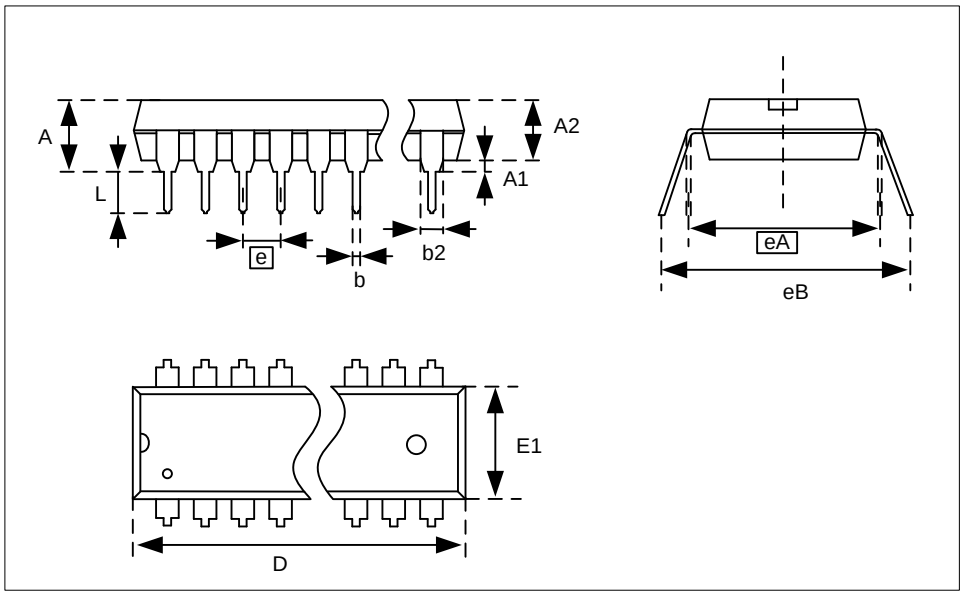
SOP18



Package：SOP18						
Symbol	(mm)			(inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	2.65	0.053	0.063	0.105
A1	0.10	-	0.30	0.003	-	0.012
A2	2.20	2.30	2.40	0.086	0.091	0.095
D	11.25	11.45	11.65	0.443	0.451	0.459
E	10.10	10.30	10.50	0.397	0.405	0.414
E1	7.30	7.50	7.70	0.287	0.295	0.304
b	0.35	-	0.44	0.0137	-	0.018
e	-	1.27	-	-	0.050	-
L	0.70	-	1.00	0.027	-	0.040
θ	0°	-	8°	0°	-	8°

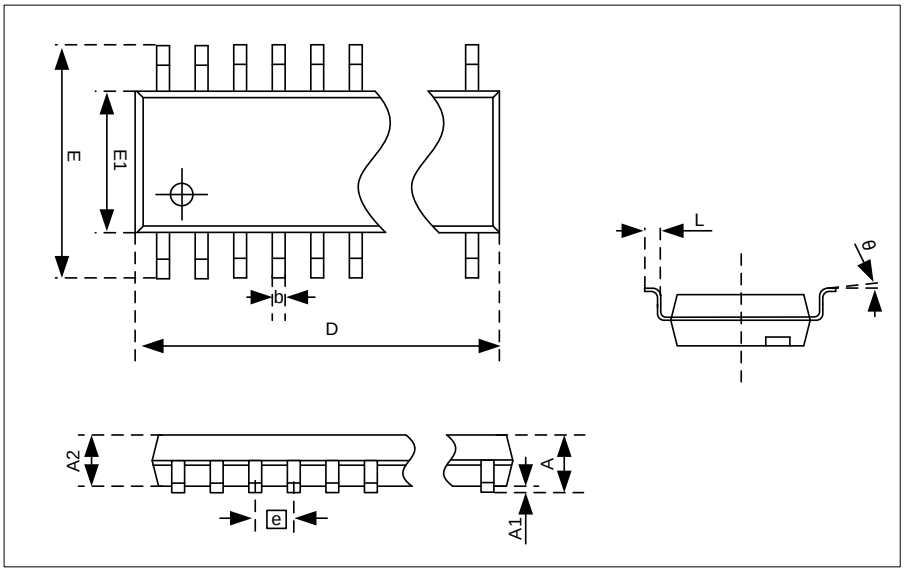
7. 3 16-pin Package Drawing

DIP16



Package:DIP16						
Symbol	(mm)			(inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.60	3.80	4.00	0.141	0.150	0.158
A1	0.51	-	-	0.020	-	-
A2	3.10	3.30	3.50	0.122	0.130	0.138
b	0.44	-	0.53	0.017	-	0.020
b2	-	1.52	-	-	0.060	-
D	18.90	19.10	19.30	0.744	0.752	0.761
E1	6.15	6.35	6.55	0.242	0.250	0.258
e	-	2.54	-	-	0.100	-
eA	-	7.62	-	-	0.300	-
eB	7.62	-	9.50	0.300	-	0.375
L	3.00	-	-	0.118	-	-

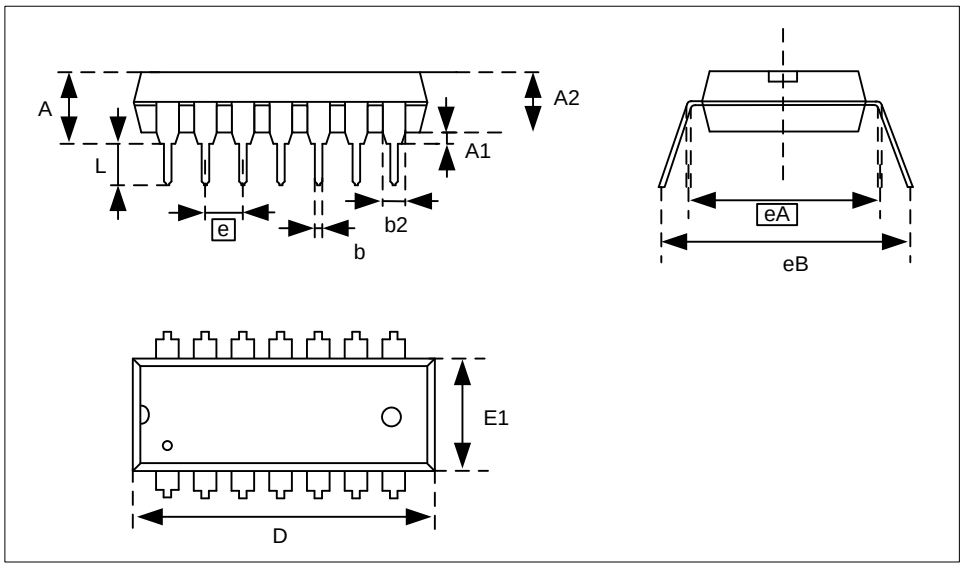
SOP16



Package: SOP16						
Symbol	(mm)			(inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.77	-	-	0.070
A1	0.08	0.18	0.28	0.003	0.007	0.011
A2	1.20	1.40	1.60	0.047	0.057	0.063
D	9.70	9.90	10.10	0.382	0.390	0.398
E	5.80	6.00	6.20	0.228	0.236	0.245
E1	3.70	3.90	4.10	0.145	0.153	0.162
b	0.39	-	0.48	0.015	-	0.019
e	-	1.27	-	-	0.050	-
L	0.50	0.65	0.80	0.020	0.025	0.032
θ	0º	-	8º	0º	-	8º

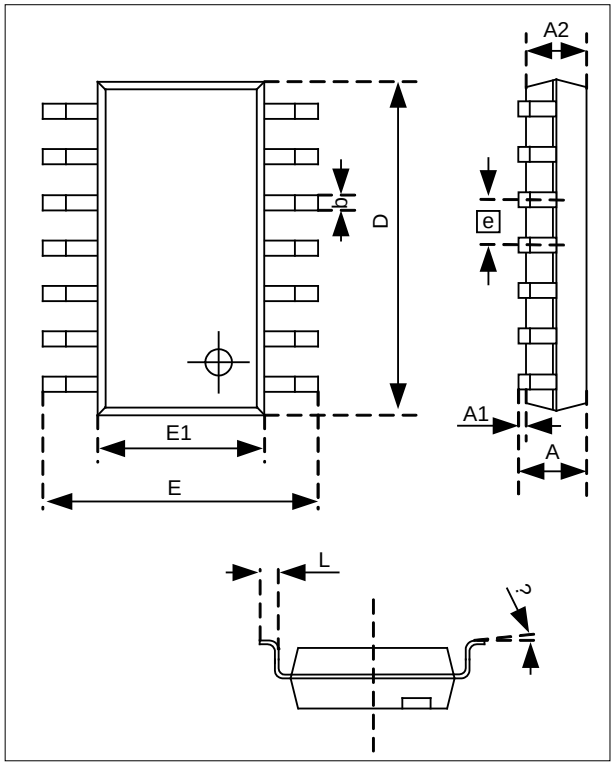
7. 4 14-pin Package Drawing

DIP14



Package: DIP14						
Symbol	(mm)			(inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	4.57	-	-	0.180
A1	0.38	-	-	0.015	-	-
A2	3.25	3.30	3.45	0.128	0.130	0.136
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.27	1.52	1.78	0.050	0.060	0.070
D	18.90	19.15	19.30	0.744	0.754	0.760
E1	6.35	6.50	6.65	0.250	0.256	0.262
e	-	2.54	-	-	0.100	-
eA	7.62	-	8.26	0.300	-	0.325
eB	8.64	-	9.65	0.340	-	0.380
L	3.18	-	-	0.125	-	-

SOP14



Package: SOP14						
Symbol	(mm)			(inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.60	1.75	0.053	0.063	0.069
A1	0.10	-	0.25	0.004	-	0.010
A2	-	1.45	-	-	0.057	-
D	8.55	-	8.75	0.337	-	0.344
E	5.80	-	6.20	0.228	-	0.244
E1	3.80	-	4.00	0.150	-	0.157
b	0.33	-	0.51	0.013	-	0.020
e	-	1.27	-	-	0.050	-
L	0.40	-	1.27	0.016	-	0.050
θ	0º	-	8º	0º	-	8º

Appendix1 Instruction Set

Appendix1. 1 Overview

The HR7P171 provides 66 RISC instructions.

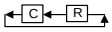
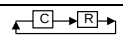
Most of the assembly instruction names are designed in abbreviations of English to make programming easier. After being complied and linked by Assembler and Compiler, the program consisted of these instructions will be converted to corresponding instruction machine codes, which include OP codes and Operands. Each OP code corresponds to one mnemonics.

One machine cycle is 1μs when the device operates at 4MHz. Based on the machine cycles required for individual instruction operations, there are two-cycle instruction and single-cycle instruction. CALL, GOTO, RET, RETIA and RETIE are two-cycle instructions; JBC, JBS, JDEC, JINC, JCAIE, JCAIG, JCAIL, JCRAE, JCRAG and JCRALare two-cycle instructions only when the jump conditions are met, otherwise they are single-cycle instructions. Other instructions are single-cycle instructions.

Appendix1. 2 Register Instructions

No.	Instruction		Affected status bit	Machine cycle	Operation
1	SECTION	N	-	1	Not supported in HR7P171
2	MOV	R, F	Z	1	(R)->(DEST.)
3	MOVA	R	-	1	(A)->(R)
4	MOVAB	F	-	1	F=0,(B)->(A) F=1, (A)->(B)
5	MOVAR	R	-	1	(A)->(R)(0≤R≤511)
6	MOVI	I	-	1	I->(A)
7	MOVRA	R	-	1	(R)->(A) (0≤R≤511)
8	PAGE	N	-	1	N<0> -> (PCRH<3>)

Appendix1. 3 Arithmetic/Logic Operation Instructions

No.	Instruction		Affected status bit	Machine cycle	Operation
9	ADD	R, F	C, DC, Z	1	(R)+(A)->(DEST.)
10	ADDC	R, F	C, DC, Z	1	(R)+(A)+C->(DEST.)
11	ADDCI	I	C, DC, Z	1	I+(A)+C->(A)
12	ADDI	I	C, DC, Z	1	I+(A)->(A)
13	AND	R, F	Z	1	(A).AND.(R)->(DEST.)
14	ANDI	I	Z	1	I.AND.(A)->(A)
15	BCC	R, M	-	1	0->R<M> (0≤M≤7)
16	BSS	R, M	-	1	1->R<M> (0≤M≤7)
17	BTT	R, M	-	1	~(R<M>)->R<M> (0≤M≤7)
18	CLR	R	Z	1	(R) = 0
19	CLRA		Z	1	(A) = 0
20	CLRB		Z	1	(B) = 0
21	COM	R, F	Z	1	~(R)->(DEST.)
22	DAR	R, F	C	1	(R) (BCD)->(DEST.)
23	DAW		C	1	(A) (BCD)->(A)
24	DEC	R, F	C, DC, Z	1	(R)-1->(DEST.)
25	INC	R, F	C, DC, Z	1	(R)+1->(DEST.)
26	IOR	R, F	Z	1	(A).OR.(R)->(DEST.)
27	IORI	I	Z	1	I.OR.(A)->(A)
28	MUL	R, F	-	1	(R).MUL.(A)-> {B, DEST.}
29	MULI	I	-	1	I.MUL.(A)-> {B, A}
30	RL	R,F	C,Z	1	
31	RLNC	R,F	Z	1	
32	RR	R,F	C,Z	1	
33	RRNC	R,F	Z	1	
34	SETR	R	-	1	FF_H->(R)
35	SUB	R, F	C, DC, Z	1	(R)-(A)->(DEST.)
36	SUBC	R, F	C, DC, Z	1	(R)-(A)- (~C)->(DEST.)
37	SUBCI	I	C, DC, Z	1	I-(A)- (~C)->(A)
38	SUBI	I	C, DC, Z	1	I-(A)->(A)
39	SSUB	R, F	C, DC, Z	1	(A)-(R) -> (DEST.)
40	SSUBC	R, F	C, DC, Z	1	(A)-(R) - (~C) ->(DEST.)
41	SSUBCI	I	C, DC, Z	1	(A)-I- (~C)->(A)
42	SSUBI	I	C, DC, Z	1	(A)-I->(A)
43	SWAP	R, F	-	1	R<3:0>->(DEST.)<7:4>, R<7:4>->(DEST.)<3:0>
44	XOR	R, F	Z	1	(A).XOR.(R)->(DEST.)
45	XORI	I	Z	1	I.XOR.(A)->(A)

Appendix1. 4 Program Control Instructions

No.	Instruction		Affected status bit	Machine cycle	Operation
46	CALL	I	-	2	PC+1->TOS, I->PC<10:0>
47	CWDT		N_TO, N_PD	1	00_H->WDT, 0->WDT Prescaler, 1->N_TO, 1->N_PD
48	GOTO	I	-	2	I->PC<10:0>
49	IDLE		N_TO, N_PD	1	00_H->WDT, 0->WDT Prescaler, 1->N_TO, 0->N_PD
50	JBC	R, M	-	1(2)	Skip if R<M> = 0 (0≤M≤7)
51	JBS	R, M	-	1(2)	Skip if R<M> = 1 (0≤M≤7)
52	JCAIE	I	-	1(2)	skip if (A) = i
53	JCAIG	I	-	1(2)	skip if (A) > i
54	JCAIL	I	-	1(2)	skip if (A) < i
55	JCRAE	R	-	1(2)	skip if (R) = (A)
56	JCRAG	R	-	1(2)	skip if (R) > (A)
57	JCRAL	R	-	1(2)	skip if (R) < (A)
58	JDEC	R, F	-	1(2)	(R)-1->(DEST.), Skip if (DEST.) = 0
59	JINC	R, F	-	1(2)	(R)+1->(DEST.), Skip if (DEST.) = 0
60/61	NOP		-	1	No operation
62	POP		-	1	Restore value of A,B,PSW,PCRH,BKSR from corresponding mirror register automatically
63	PUSH		-	1	Save value of A, B, PSW, PCRH, BKSR to corresponding mirror register automatically
64	RET		-	2	TOS->PC
65	RETIA	I	-	2	I->(A),TOS->PC
66	RETIE		-	2	TOS->PC,1->GIE

Note：

1. I—Immediate, F—Flag bit, A—Register A, B—Register B, R—Register R, M—the M^{th}-bit of Register R.
2. C—Carry/Borrow, DC—Half carry / Half borrow bit, Z—Zero flag bit.
3. TOS—Top Of Stack.
4. If F = 0, the destination register (DEST.) is register A; if F = 1, the destination register (DEST.) is register R.
5. The length of immediate N varies from device to device. For HR7P171, only PCRH<3> is used to select the page, so the length of N is 1.

Appendix2 Special Function Register Summary

Special Function Register Area 0:

Address	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	POR vaule
000_H	IAD	Indirect Addressing Data Register								xxxx xxxx
001_H	T8N	T8N Register								xxxx xxxx
002_H	PCRL	Program Counter Register Low Byte								0000 0000
003_H	PSW	-	-	-	-	-	Z	DC	C	0000 0xxx
004_H	IAA	Indirect Addressing Address Register								xxxx xxxx
005_H	PA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	xxxx xxxx
006_H	PB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	xxxx xxxx
007_H	PC	-	-	-	-	-	-	PC1	PC0	xxxx xxxx
008_H	-	-								-
009_H	-	-								-
$00A_H$	PCRH	Program Counter Register High Byte								0000 0000
$00B_H$	INTC0	GIE_GIEH	PEIE_GIEL	T8NIE	PIE0	-	T8NIF	PIF0	-	0000 0000
$00C_H$	BKSR	-	-	-	IRP	-	-	RP		0000 0000
$00D_H$	INTF0	-	ADIF	-	-	ACPIF	TE2IF	T8P1IF	T16GIF	0000 0000
$00E_H$	T16GL	T16G Counter Register Low Byte								xxxx xxxx
$00F_H$	T16GH	T16G Counter Register High Byte								xxxx xxxx
010_H	T16GC	T16GGINV	T16GGEN	T16GPRS		T16GOSCEN	T16GSYN	T16GCS	T16GON	0000 0000
011_H	T8P1	T8P1 Register								xxxx xxxx
012_H	T8P1C	EPWMC	T8P1POS				T8P1E	T8P1PRS		0000 0000
013_H	CALR	Internal Clock Calibration Register								1111 1111
014_H	INTF1	-	-	T8P2IF	-	PIF3	PIF2	PIF1	-	0000 0000
015_H	TE2L	TE2 Register Low Byte								xxxx xxxx

Address	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	POR vaule
016_H	TE2H	TE2 Register High Byte								xxxx xxxx
017_H	TE2C	P1M		EPWMY	EPWMX	TE2M				0000 0000
018_H	TE2PWMC	PRSEN	PDDC							0000 0000
019_H	TE2AS	EPWMASS	EPWMAS1	-	EPWMAS0	PSSAC		PSSBD		0000 0000
$01A_H$	N_PAPU	N_PAPU7	N_PAPU6	N_PAPU5	N_PAPU4	N_PAPU3	N_PAPU2	N_PAPU1	N_PAPU0	1111 1111
$01B_H$	N_PBPU	N_PBPU7	N_PBPU6	N_PBPU5	N_PBPU4	N_PBPU3	N_PBPU2	N_PBPU1	N_PBPU0	1111 1111
$01C_H$	INTF2	KIF7	KIF6	KIF5	KIF4	KIF3	KIF2	KIF1	KIF0	xxxx xxxx
$01D_H$	T8P1P	T8P1 Period Register								1111 1111
$01E_H$	ADCRL	ADC Result Register Low Byte								xxxx xxxx
$01F_H$	ADCC0	ADCS		ADCHS			ADTRG	-	ADON	0000 0000

Special Function Register Area 1:

Address	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	POR vaule
080_H	IAD	Indirect Addressing Data Register								xxxx xxxx
081_H	BSET	-	PEG	T8NCS	T8NSE	PSA	PS			1111 1111
082_H	PCRL	Program Counter Register Low Byte								0000 0000
083_H	PSW	-	-	-	-	-	Z	DC	C	0000 0xxx
084_H	IAA	Indirect Addressing Address Register								xxxx xxxx
085_H	PAT	PAT7	PAT6	PAT5	PAT4	PAT3	PAT2	PAT1	PAT0	1111 1111
086_H	PBT	PBT7	PBT6	PBT5	PBT4	PBT3	PBT2	PBT1	PBT0	1111 1111
087_H	PCT	-	-	-	-	-	-	PCT1	PCT0	0000 0011
088_H	-	-								-
089_H	-	-								-

Address	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	POR vaule
$08A_H$	PCRH	Program Counter Register High Byte								0000 0000
$08B_H$	INTC0	GIE_GIEH	PEIE_GIEL	T8NIE	PIE0	-	T8NIF	PIF0	-	0000 0000
$08C_H$	BKSR	-	-	-	IRP	-	-	RP		0000 0000
$08D_H$	INTE0	-	ADIE	-	-	ACPIE	TE2IE	T8P1IE	T16GIE	0000 0000
$08E_H$	PWRC	-	-	-	LPMS	N_TO	N_PD	N_POR	N_BOR	0100 110x
$08F_H$	INTC1	-	-	-	INTVEN0	SOFTIF	-	INTV		0000 0000
090_H	INTP	IGP7	IGP6	IGP5	IGP4	IGP3	IGP2	IGP1	IGP0	0000 0000
091_H	T8P2	T8P2 Register								xxxx xxxx
092_H	T8P2C	-	T8P2POS				T8P2E	T8P2PRS		0000 0000
093_H	OSCC	-	IRCPRS			-	-	-	-	0110 0000
094_H	INTE1	-	-	T8P2IE	-	PIE3	PIE2	PIE1	-	0000 0000
095_H	ACPC	ACP2O	ACP1O	ACP2INV	ACP1INV	ACPIS	ACPM			0000 0111
096_H	VRC	VREN	-	VRR	-	VR				0000 0000
097_H	TE1L	TE1 Register Low Byte								xxxx xxxx
098_H	TE1H	TE1 Register High Byte								xxxx xxxx
099_H	TE1C	PWMTBS	-	PWMLSB		PWMEN	-	-	-	0000 0000
$09A_H$	ADSEL	ADSEL7	ADSEL6	ADSEL5	ADSEL4	ADSEL3	ADSEL2	ADSEL1	ADSEL0	0000 0000
$09B_H$	WKDC	Weak-up Delay Control Register								1111 1111
$09C_H$	INTE2	KIE7	KIE6	KIE5	KIE4	KIE3	KIE2	KIE1	KIE0	0000 0000
$09D_H$	T8P2P	T8P2 Period Register								1111 1111
$09E_H$	ADCRH	ADC Result Register High Byte								xxxx xxxx
$09F_H$	ADCC1	ADFM	ADVREF	-	-	-	-	-	-	0000 0000

Special Function Register Area 2:

Address	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	POR vaule
100_H	IAD	Indirect Addressing Data Register								xxxx xxxx
101_H	T8N	T8N Register								xxxx xxxx
102_H	PCRL	Program Counter Register Low Byte								0000 0000
103_H	PSW	-	-	-	-	-	Z	DC	C	0000 0xxx
104_H	IAA	Indirect Addressing Address Register								xxxx xxxx
105_H	PA	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	xxxx xxxx
106_H	PB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	xxxx xxxx
107_H	PC	-	-	-	-	-	-	PC1	PC0	xxxx xxxx
108_H	-	-								-
109_H	-	-								-
$10A_H$	PCRH	Program Counter Register High Byte								0000 0000
$10B_H$	INTC0	GIE_GIEH	PEIE_GIEL	T8NIE	PIE0	-	T8NIF	PIF0	-	0000 0000
$10C_H$	BKSR	-	-	-	IRP	-	-	RP		0000 0000
$10D_H$	-	-								-
$10E_H$	-	-								-
$10F_H$	-	-								-

Special Function Register Area 3:

Address	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	POR vaule
180_H	IAD	Indirect Addressing Data Register								xxxx xxxx
181_H	BSET	-	PEG	T8NCS	T8NSE	PSA	PS			1111 1111
182_H	PCRL	Program Counter Register Low Byte								0000 0000
183_H	PSW	-	-	-	-	-	Z	DC	C	0000 0xxx
184_H	IAA	Indirect Addressing Address Register								xxxx xxxx
185_H	PAT	PAT7	PAT6	PAT5	PAT4	PAT3	PAT2	PAT1	PAT0	1111 1111
186_H	PBT	PBT7	PBT6	PBT5	PBT4	PBT3	PBT2	PBT1	PBT0	1111 1111
187_H	PCT	-	-	-	-	-	-	PCT1	PCT0	0000 0011
188_H	-	-								-
189_H	-	-								-
$18A_H$	PCRH	Program Counter Register High Byte								0000 0000
$18B_H$	INTC0	GIE_GIEH	PEIE_GIEL	T8NIE	PIE0	-	T8NIF	PIF0	-	0000 0000
$18C_H$	BKSR	-	-	-	IRP	-	-	RP		0000 0000
$18D_H$	-	-								-
$18E_H$	-	-								-
$18F_H$	-	-								-

Appendix3 Electrical Characteristics

Appendix3. 1 Parameter Characteristics

◆ Absolute Maximum Ratings

Parameter	Symbol	Conditions	Range	Unit
Power supply	VDD	-	-0.3 ~ 7.5	V
Input voltage	V_{IN}	-	-0.3 ~ VDD + 0.3	V
Output voltage	V_{OUT}	-	-0.3 ~ VDD + 0.3	V
Storage temperature	T_{STG}	-	-55 ~ 125	℃
Operation temperature	T_{OPR}	VDD：3.0 ~ 5.5V	-40 ~ 85	℃

◆ Power Consumption Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Conditions
Power Supply	VDD	3.0	-	5.5	V	-40℃ ~ 85℃
Idle 1 current	I_{PD}	-	160	-	μA	25℃, VDD=5V, BOR disabled, WDT disabled.
		-	160	-	μA	25℃, VDD = 5V, BOR disabled, WDT enabled, clock source divided by 256, wake-up delay 1024Tosc.
		-	170	-	μA	25℃, VDD = 5V, BOR enabled, WDT disabled.
Idle 0 current	I_{PD}	-	1.01	-	mA	25℃, VDD = 5V, 8MHz clock input, BOR disabled, WDT disabled.
		-	1.01	-	mA	25℃, VDD = 5V, 8MHz clock input, BOR disabled, WDT enabled, clock source divided by 256, wake-up delay 1024Tosc.
		-	1.02	-	mA	25℃, VDD = 5V,8MHz clock input, BOR enabled, WDT disabled.
Normal operating current	I_{OP1}	—	3.5	—	mA	25℃, VDD = 5V, normal operation mode, internal INTOSCIO mode, 8MHz clock, I/O port output level fixed, no load.
	I_{OP2}	—	4	—	mA	25℃, VDD = 5V, normal operation mode, external HS mode, 8MHz clock, I/O

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Conditions
						port output level fixed, no load.
Max.input current on VDD pin	I_{MDD}	-	80	-	mA	25℃, VDD = 5V
Max. output current on VSS pin	I_{MSS}	-	200	-	mA	25℃, VDD = 5V
Sink current on normal drive I/O	I_{OL}	-	15	-	mA	25℃, VDD = 5V, V_{OL} =0.6V
Source current on normal drive I/O	I_{OH}	-	15	-	mA	25℃, VDD = 5V V_{OH} = 4.4V
Sink current on high drive I/O	I_{OL}	-	30	-	mA	25℃, VDD = 5V, V_{OL} =0.6V
Source current on high drive I/O	I_{OH}	-	15	-	mA	25℃, VDD = 5V V_{OH} = 4.4V

◆ Input Port Characteristics

Operation temperature: -40℃ ~ 85℃						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input high level (with SMT input characteristic)	V_{IH}	0.8VDD	-	VDD	V	3.0V≤VDD≤5.5V
N_MRST input high level (with SMT input characteristic)		0.8VDD	-	VDD	V	
Input low level	V_{IL}	VSS	-	0.18VDD	V	
N_MRST input low level		VSS	-	0.2VDD	V	
Input leakage current	I_{IL}	-	-	±1	μA	3.0V≤VDD≤5.5V (port in high impedance state)
N_MRST input leakage current		-	-	5	μA	VSS≤V_{PIN}≤VDD

Input weak pull up current	I_{WPU}	15	-	70	μA	3.0V≤VDD≤5.5V V_{PIN} = VSS

◆ Output Port Characteristics

Chip Operation temperature: -40℃ ~ 85℃						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output high level	V_{OH}	VDD-0.7	-	-	V	3.0V≤VDD≤5.5V I_{OH} = -3.0mA
Output low level	V_{OL}	-	-	0.6	V	3.0V≤VDD≤5.5V I_{OL} = -8.5mA

◆ Clock Requirements

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
System clock frequency	Fosc	-	-	16	MHz	3.0V≤VDD≤5.5V
System clock period	Tosc	62.5	-	-	ns	3.0V≤VDD≤5.5V
Machine cycle	T_{INST}	250	-	-	ns	-
External clock high and low time	T_{OSL},T_{OSH}	15	-	-	ns	-
External clock rising and falling time	T_{OSR},T_{OSF}	-	-	15	ns	-
WDT overflow time	T_{WDT}	13 (37K)	17 (30K)	21 (25K)	ms	No frequency division, VDD = 5V

◆ ADC AC characteristics

Parameter name	Typ.	Unit
Resolution	10	bit
Difference linearity	±1	LSB
Integral linearity	±1	LSB
Offset Error	2.5	LSB
Reference voltage range	3.0~ VDD+0.3	V
Analog voltage input range	0 ~ VREF	V
Input Capacitance	40	Pf
Recommended analog input resistance	10	KΩ

◆ AD Conversion Time Table

A/D Clock source	Operation Frequency			
	16MHz	8MHz	4MHz	1MHz
Fosc/2	Not recommended[1]	Not recommended[1]	Not recommended[1]	Tad = 2us
Fosc/8	Not recommended[1]	Not recommended[1]	Tad = 2us	Tad = 8us
Fosc/32	Tad = 2us	Tad = 4us	Tad = 8us	Not recommended[2]
Frc	Tad = 2~6us	Tad = 2~6us	Tad = 2~6us	Tad = 2~6us

Note：

1. Tad value does not meet the design requirement, so not recommended.
2. The conversion time takes too long, so other settings are recommended.

◆ Analog comparator ACP AC characterristics

Characteristics	MIX.	TYP.	MAX.	Unit
Input offset voltage	-	±5	±10	mV
Input common mode voltage	0	-	VDD-1.5	V
Response time	-	-	10	us

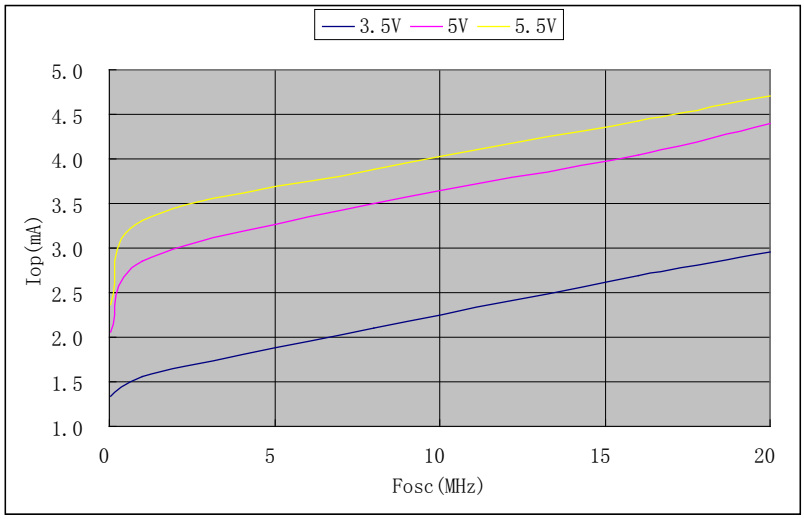
◆ Internal 16MHz clock calibration characteristics

Standard condition	Operation condition	Min.	Typ.	Max.	Unit
Frequency calibrated to 16MHz at 25℃	25℃, VDD =3.0V~ 5V	15.68	16	16.32	MHz
	-40℃～85℃, VDD = 3.0V~ 5.5V	13.5	16	17.5	MHz

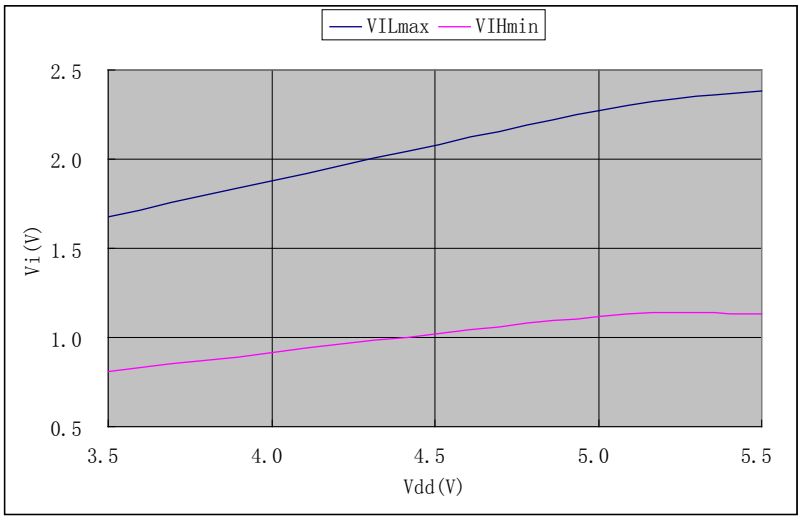
Appendix3. 2 Characteristics Graphs

All the graphs provided are a statistical summary based on a limited number of samples and are provided for design reference only. Some data in part of the graphs are beyond specification and the device is guaranteed to operate normally only within the specified range.

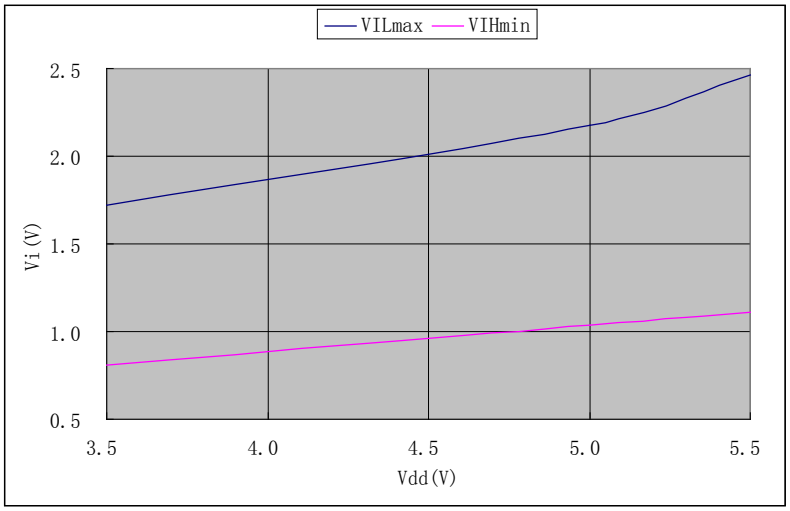
◆ Operation Current (Iop) vs.Oscillator Frequency (F_{OSC}) in normal operation mode (Room Temperature: 25℃)



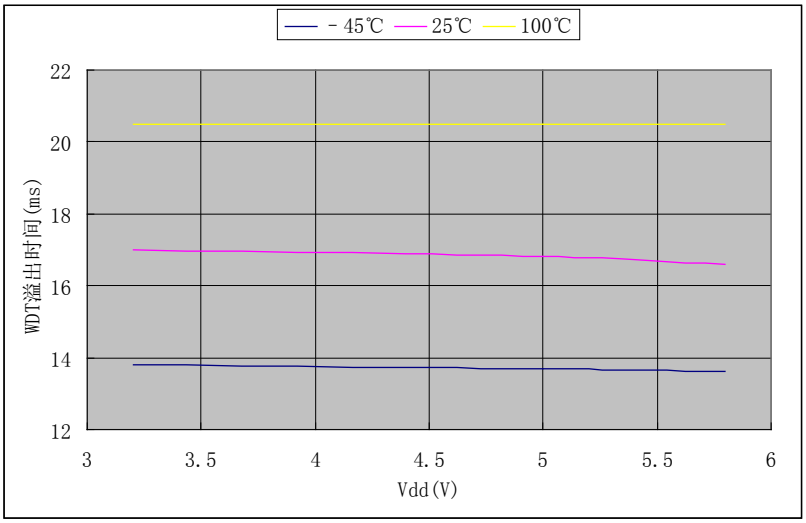
◆ External Reset Signal Input Characteristics (Room Temperature:25℃)



◆ I/O Ports Input Characteristics (Room Temperature:25℃)

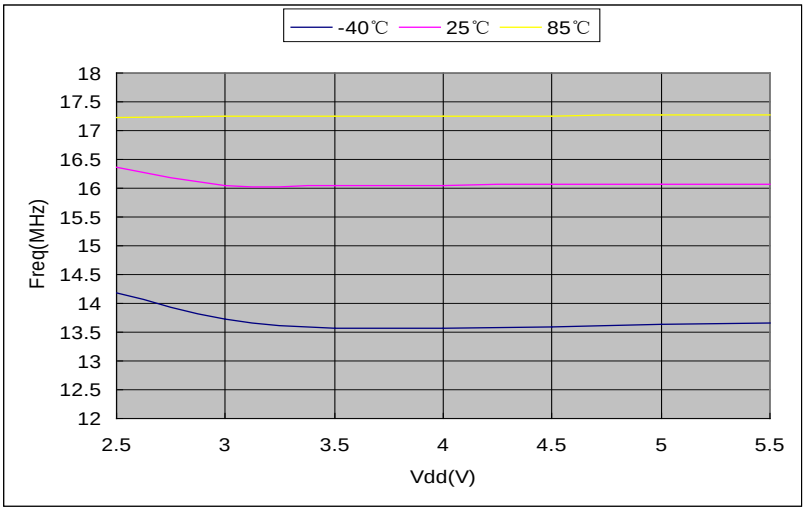


◆ WDT overflow time vs. VDD under different temperatures



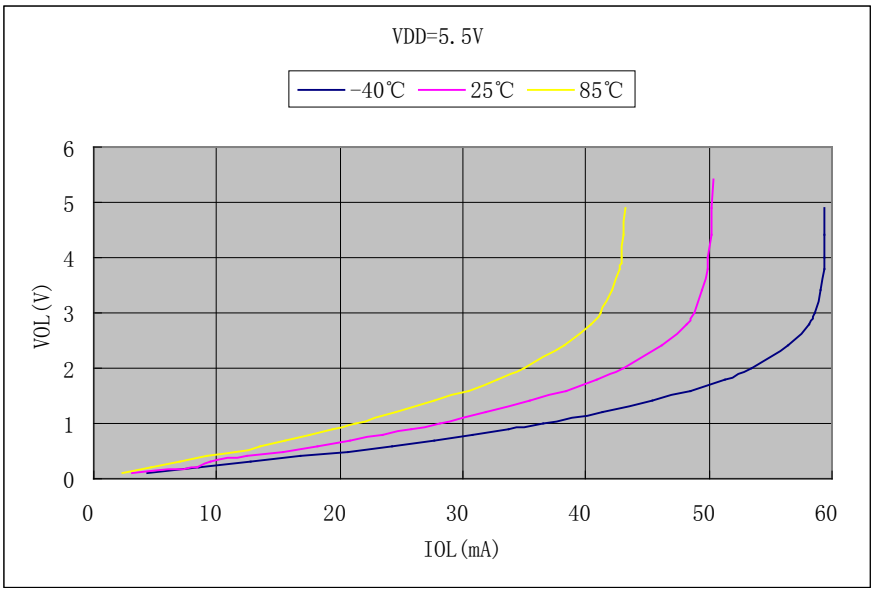
◆ Internal 16MHz clock frequency vs. Vdd under different temperatures

First calibrate to 16MHz at VDD=3.3V, 25℃, then see how frequency behaves as VDD increases from 2.5V to 5.5V under different temperature conditions.

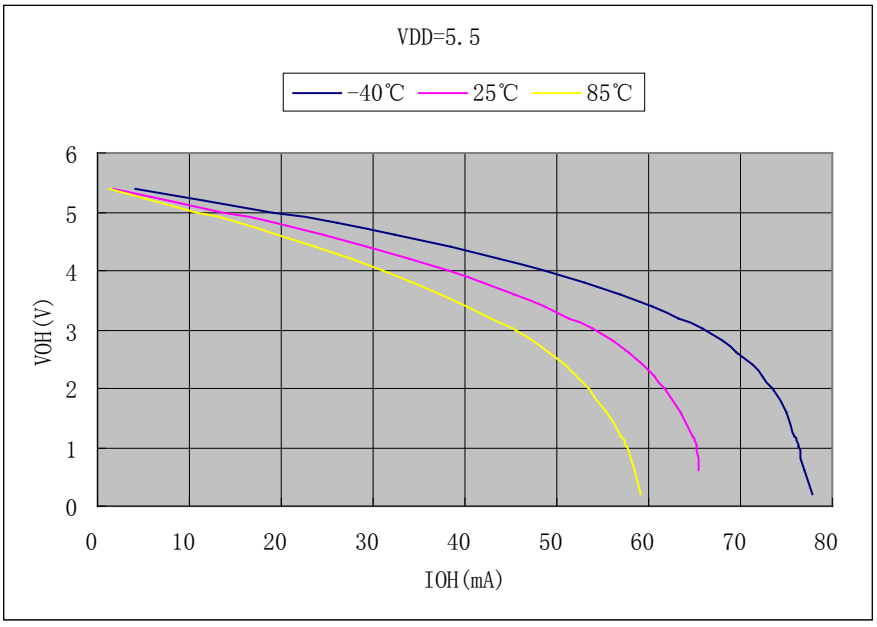


◆ I/O port output characteristics (normal drive)

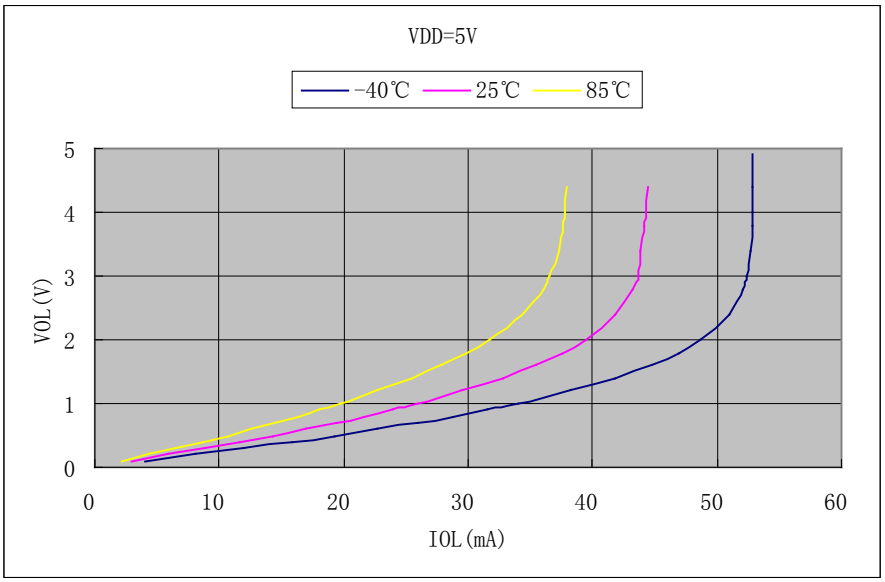
A：V_{OL} vs. I_{OL} @VDD = 5.5V (normal drive)



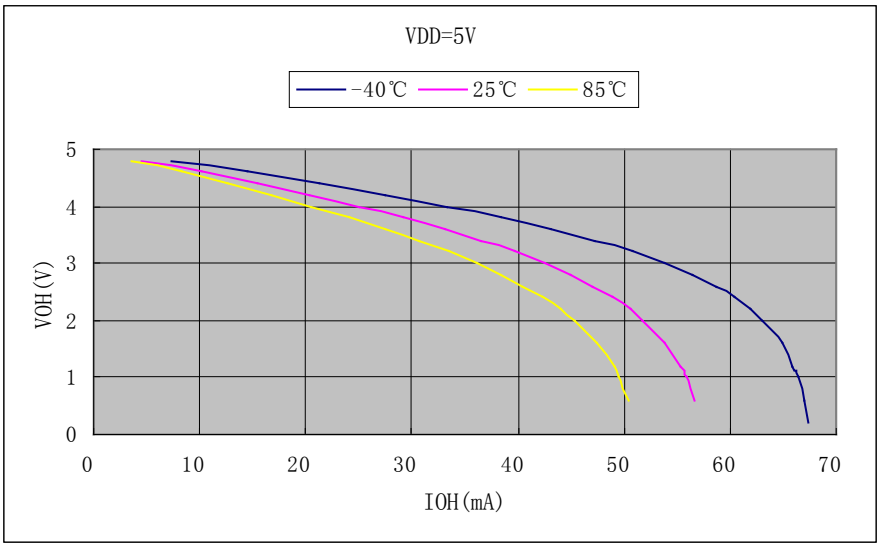
B：V_{OH} vs. I_{OH} @VDD = 5.5V (normal drive)



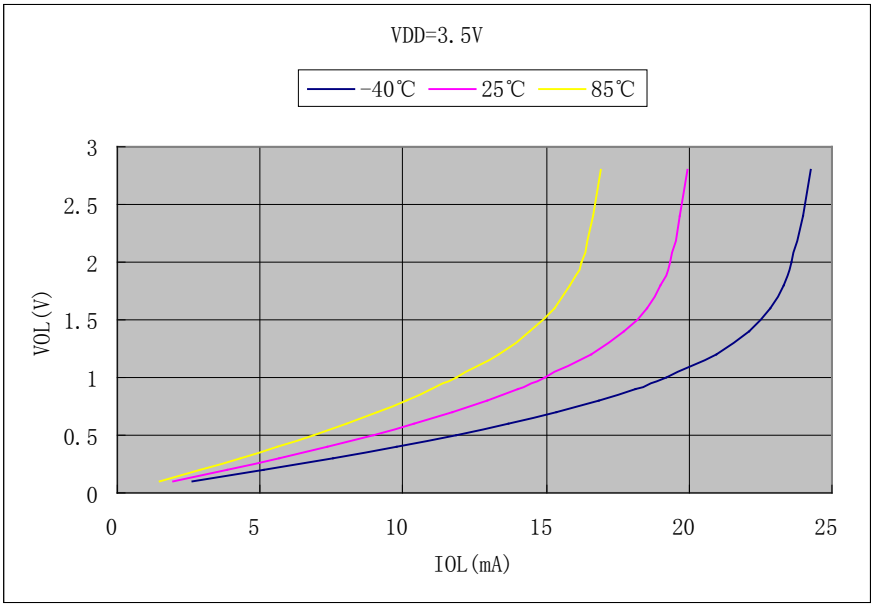
C：V_{OL} vs. I_{OL} @VDD = 5.0V (normal drive)



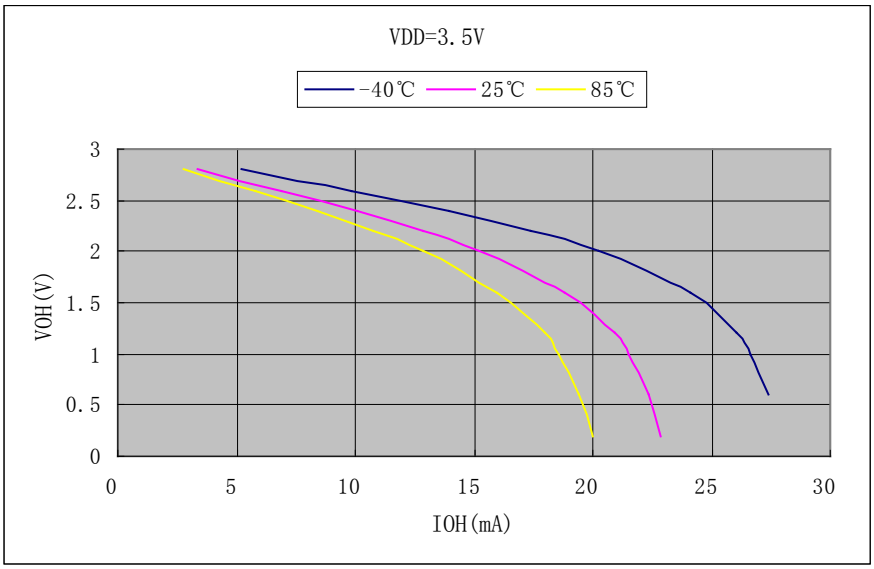
D：V_{OH} vs. I_{OH} @VDD = 5.0V (normal drive)



E：V_{OL} vs. I_{OL} @VDD = 3.5V (normal drive)

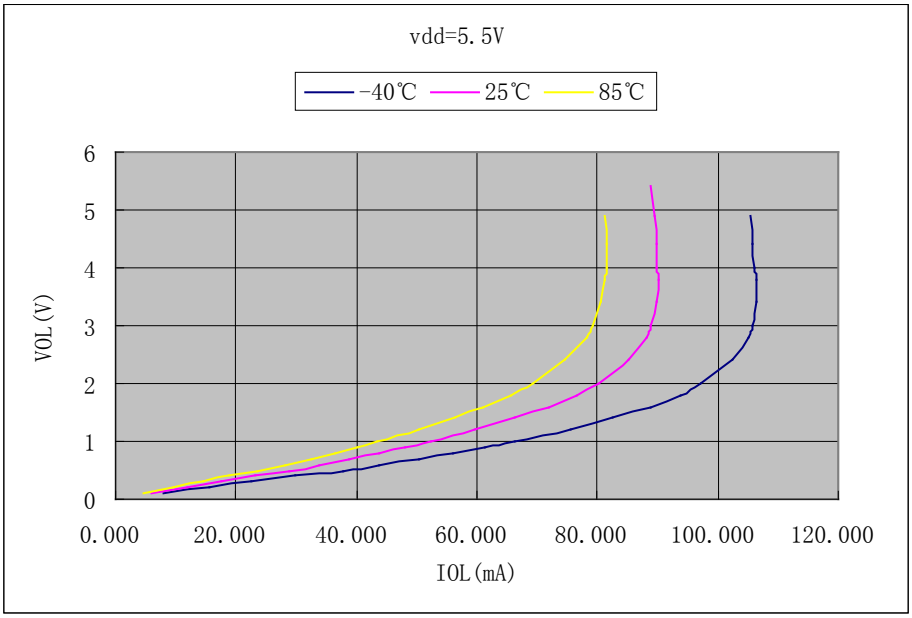


F：V_{OH} vs. I_{OH} @VDD = 3.5V (normal drive)

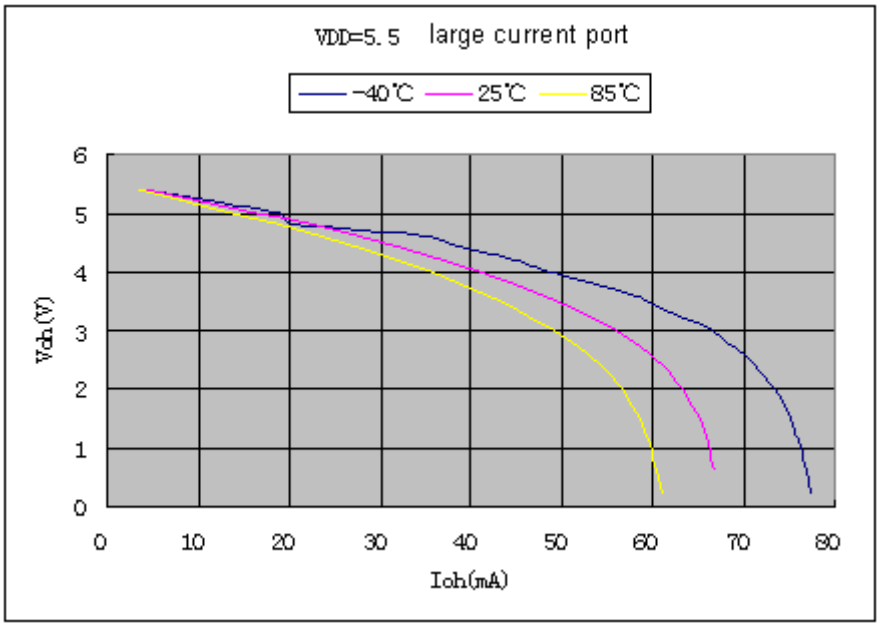


◆ I/O port output characteristics(high drive)

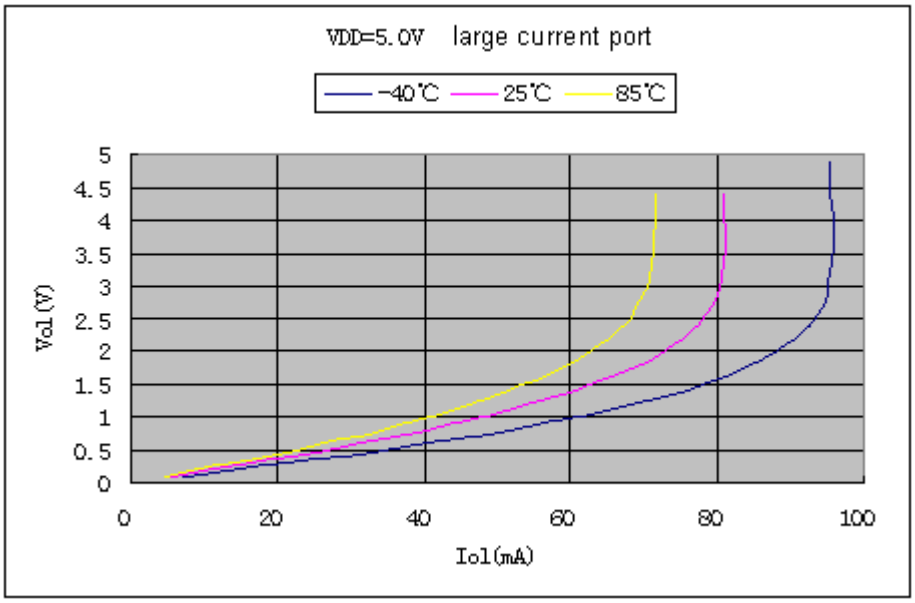
A：V_{OL} vs. I_{OL} @VDD = 5.5V(high drive)



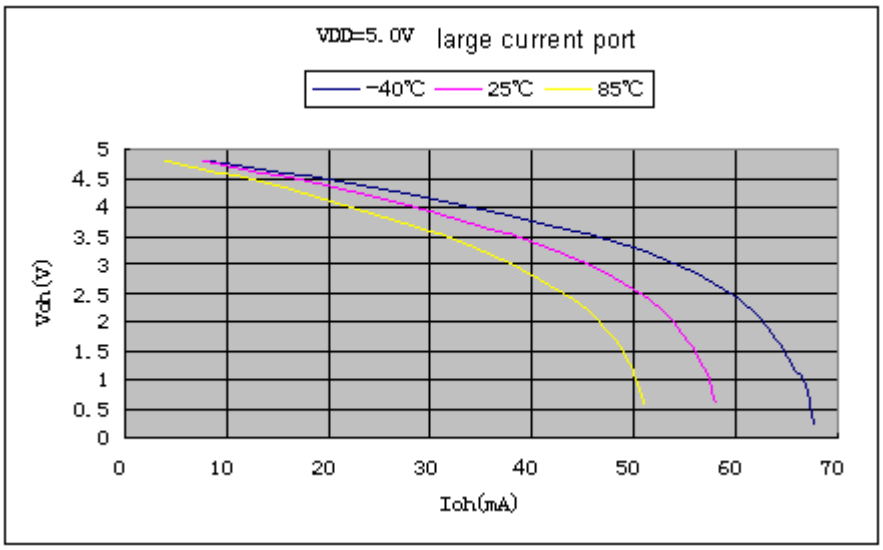
B：V_{OH} vs. I_{OH} @VDD = 5.5V(high drive)



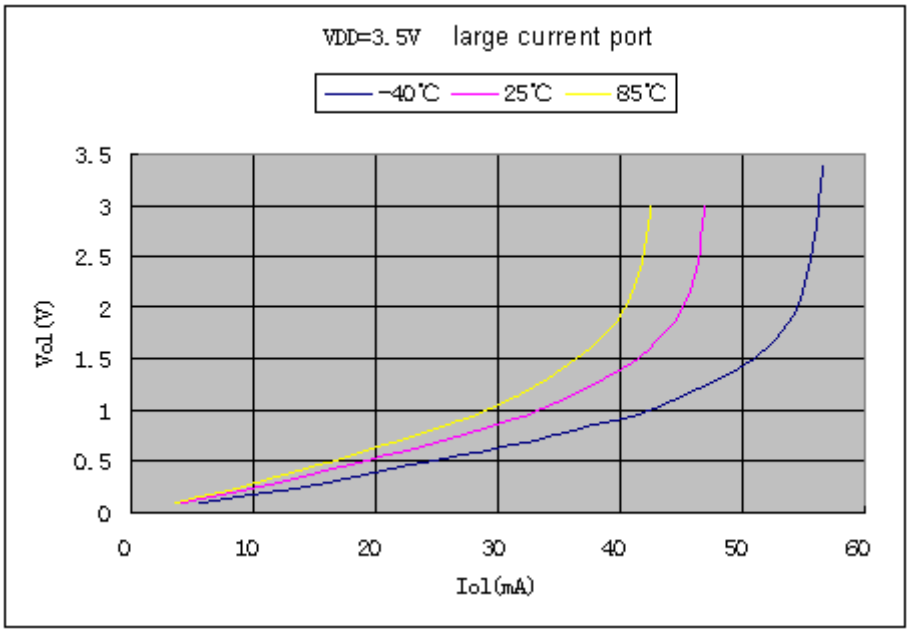
C：V_{OL} vs. I_{OL} @VDD = 5.0V(high drive)



D：V_{OH} vs. I_{OH} @VDD = 5.0V(high drive)



E：V_{OL} vs. I_{OL} @VDD = 3.5V(high drive)



F：V_{OH} vs. I_{OH} @VDD = 3.5V(high drive)