

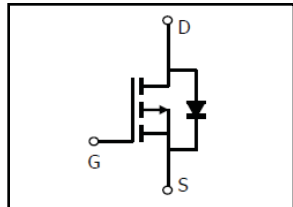
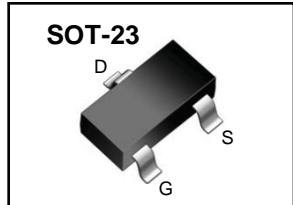
HRLE550P03K

-30V P-Channel MOSFET

$BV_{DSS} = -30\text{ V}$
 $R_{DS(on)max} = 55\text{ m}\Omega$
 $I_D = -4\text{ A}$

FEATURES

- Super High Dense Cell Design
- Reliable and Rugged
- Lower $R_{DS(ON)}$: 55 mΩ (Max.) @ $V_{GS}=-10V$
- Lower $R_{DS(ON)}$: 65 mΩ (Max.) @ $V_{GS}=-4.5V$
- Lower $R_{DS(ON)}$: 100 mΩ (Max.) @ $V_{GS}=-2.5V$
- 100% Avalanche Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units	
V_{DSS}	Drain-Source Voltage	-30	V	
V_{GS}	Gate-Source Voltage	± 12	V	
I_D	Drain Current	$T_A = 25^\circ\text{C}$	-4	A
		$T_A = 70^\circ\text{C}$	-3.1	A
I_{DM}	Pulsed Drain Current	-12	A	
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	1.4	W
		$T_A = 100^\circ\text{C}$	0.6	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$	

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	--	95	$^\circ\text{C}/\text{W}$

Electrical Characteristics $T_A=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1.0	--	-2.5	V
$R_{DS(ON)}^1$	Static Drain-Source On-Resistance	$V_{GS} = -10\ \text{V}, I_D = -4\ \text{A}$	--	45	55	m Ω
		$V_{GS} = -4.5\ \text{V}, I_D = -3\ \text{A}$	--	57	65	m Ω
		$V_{GS} = -2.5\ \text{V}, I_D = -2\ \text{A}$	--	80	100	m Ω

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\ \text{V}, I_D = -250\ \mu\text{A}$	-30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\ \text{V}, V_{GS} = 0\ \text{V}$	--	--	-1	μA
		$V_{DS} = -24\ \text{V}, T_J = 70\text{ }^\circ\text{C}$	--	--	-10	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 12\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	± 100	nA

Dynamic Characteristics ²

C_{iss}	Input Capacitance	$V_{DS} = -10\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1.0\ \text{MHz}$	--	885	--	pF
C_{oss}	Output Capacitance		--	75	--	pF
C_{rss}	Reverse Transfer Capacitance		--	65	--	pF
R_g	Gate Resistance	$V_{GS} = 0\ \text{V}, V_{DS} = 0\ \text{V}, f = 1\ \text{MHz}$	--	6	--	Ω

Switching Characteristics ²

$t_{d(on)}$	Turn-On Time	$V_{DS} = -15\ \text{V}, I_D = -1\ \text{A},$ $R_G = 6\ \Omega$	--	5.5	--	ns
t_r	Turn-On Rise Time		--	12	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	58	--	ns
t_f	Turn-Off Fall Time		--	28	--	ns
Q_g	Total Gate Charge	$V_{DS} = -15\ \text{V}, I_D = -4\ \text{A},$ $V_{GS} = -10\ \text{V}$	--	18	--	nC
Q_{gs}	Gate-Source Charge		--	1.5	--	nC
Q_{gd}	Gate-Drain Charge		--	2.9	--	nC

Source-Drain Diode Maximum Ratings and Characteristics

I_S	Continuous Source-Drain Diode Forward Current	--	-1	--	A	
V_{SD}^1	Source-Drain Diode Forward Voltage	$I_S = -1\ \text{A}, V_{GS} = 0\ \text{V}$	--	--	-1.1	V
t_{rr}	Reverse Recovery Time	$I_S = -4\ \text{A}, V_{GS} = 0\ \text{V}$ $di_F/dt = 100\ \text{A}/\mu\text{s}$	--	13	--	ns
Q_{rr}	Reverse Recovery Charge		--	7	--	nC

Notes ;

1. Pulse test : pulse width $\leq 300\text{ns}$, duty cycle $\leq 2\%$
2. Guaranteed by design, not subject to production testing

Typical Characteristics

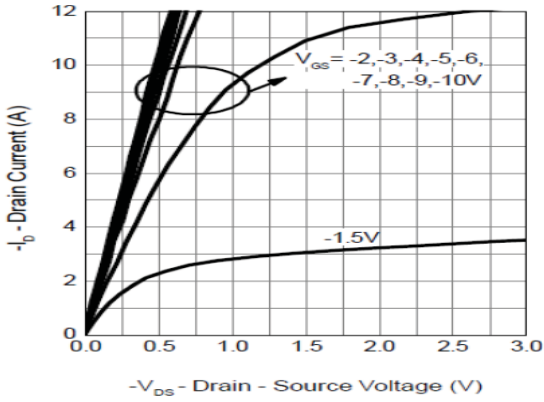


Figure 1. On Region Characteristics

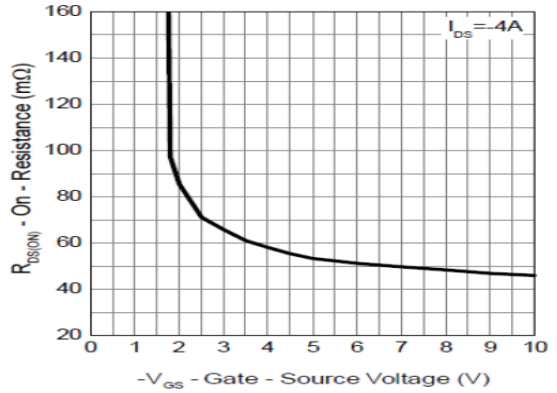


Figure 2. Gate-Source On Resistance

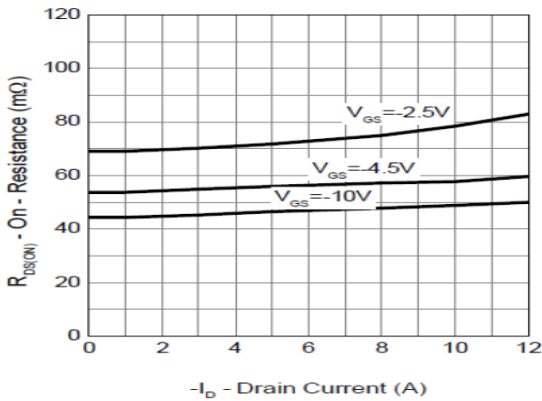


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

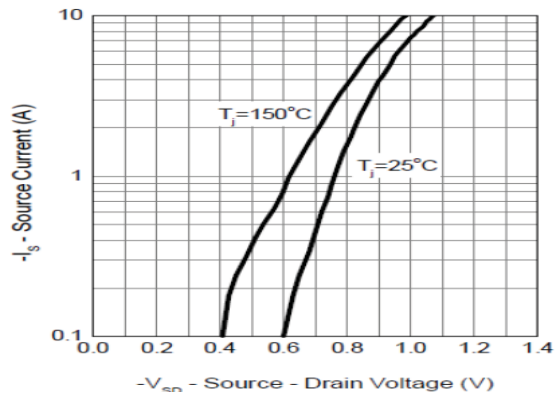


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

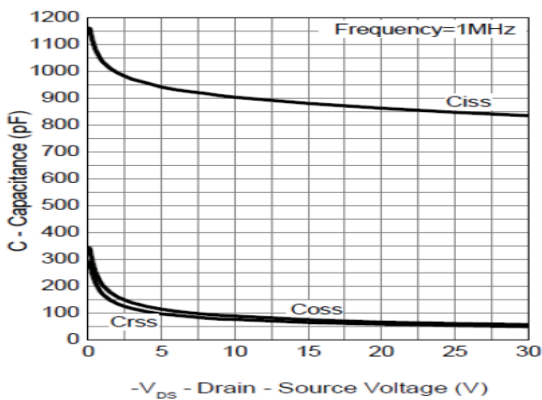


Figure 5. Capacitance Characteristics

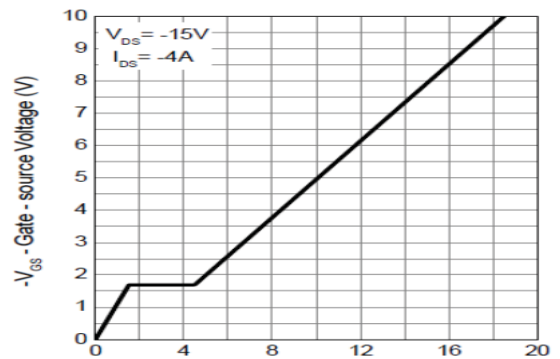


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

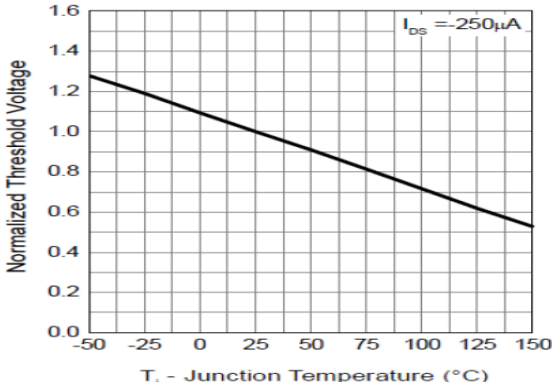


Figure 7. Gate Threshold Voltage vs Temperature

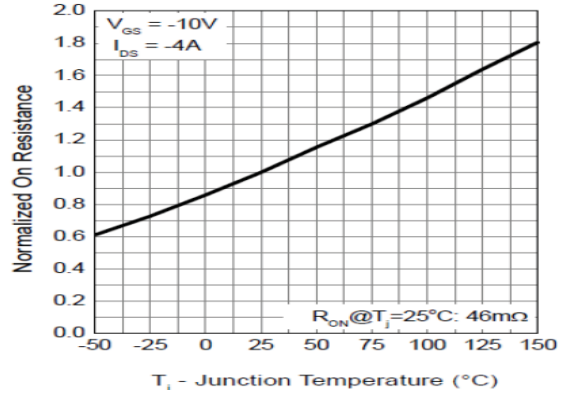


Figure 8. On-Resistance Variation vs Temperature

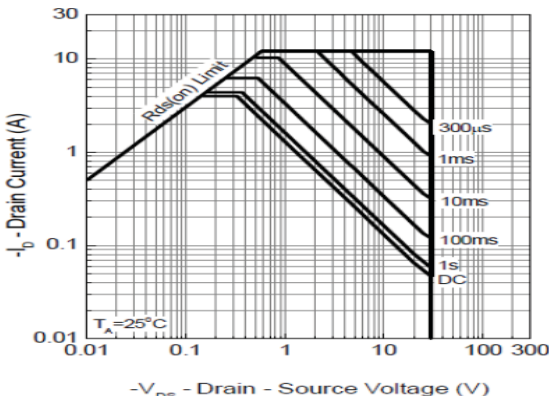


Figure 9. Maximum Safe Operating Area

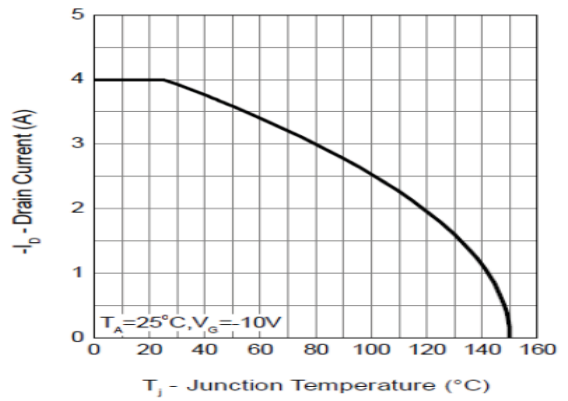


Figure 10. Maximum Drain Current vs Case Temperature

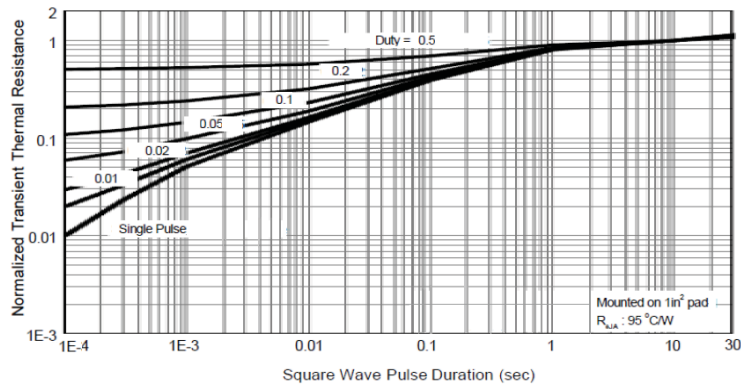


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

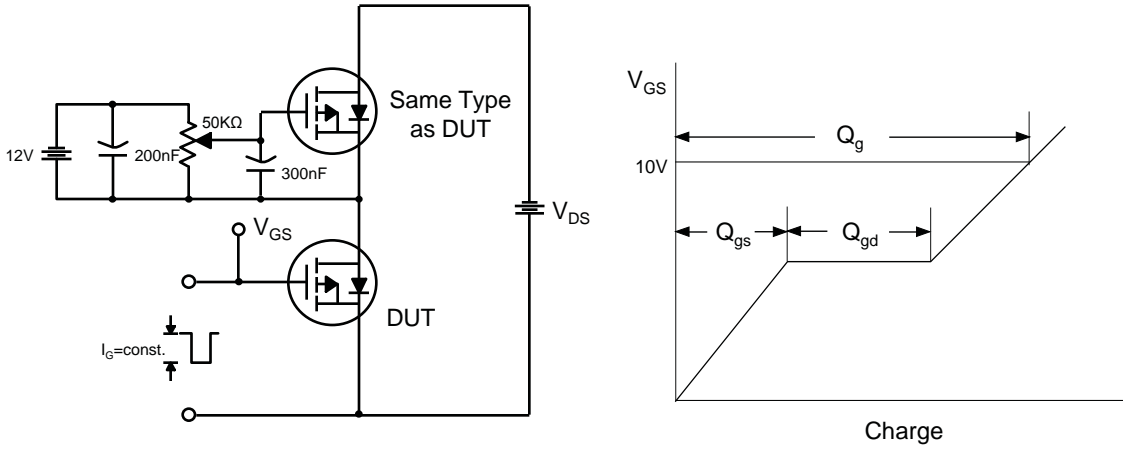


Fig 13. Resistive Switching Test Circuit & Waveforms

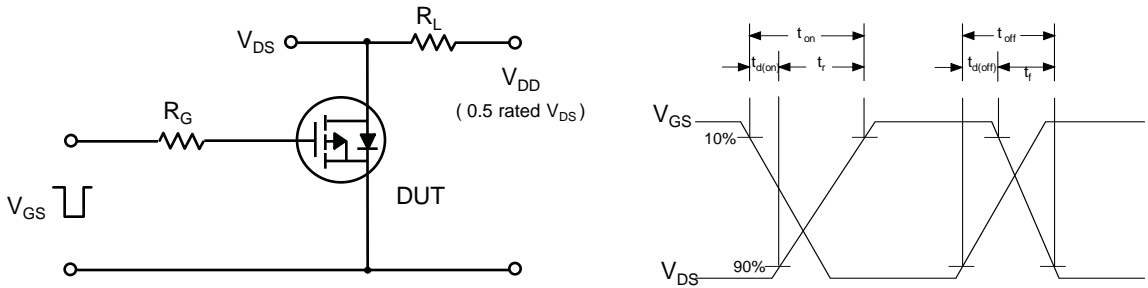


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

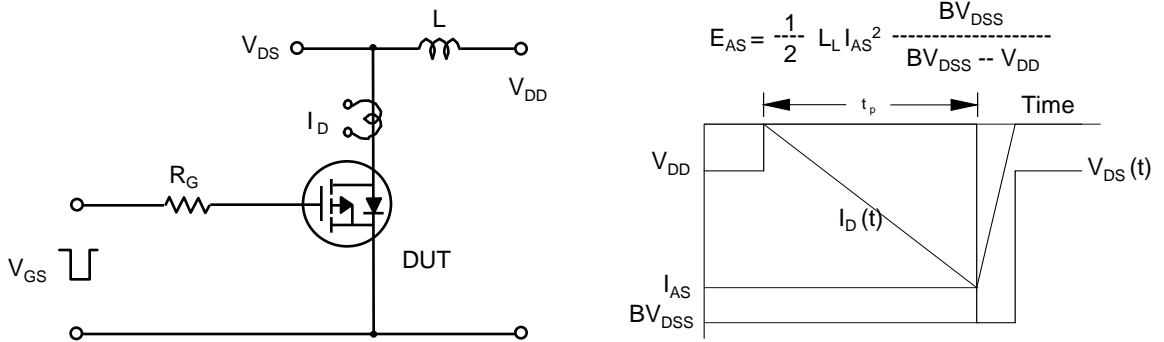
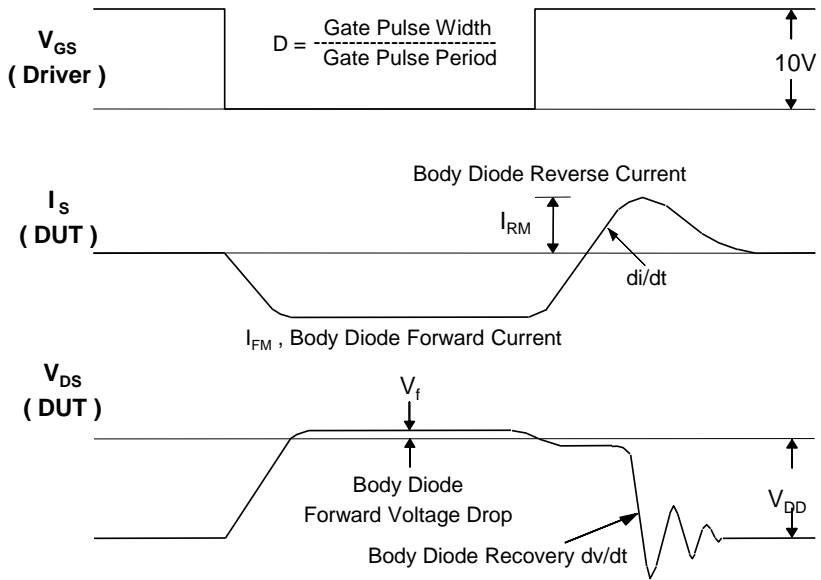
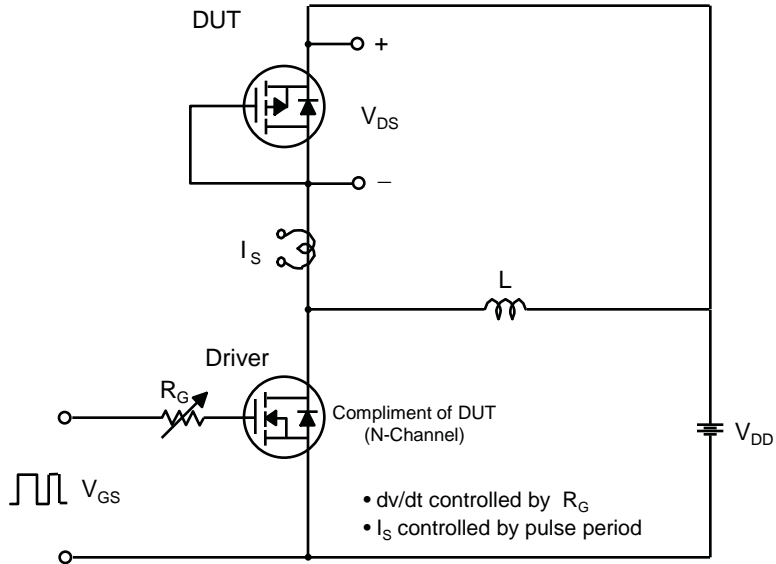
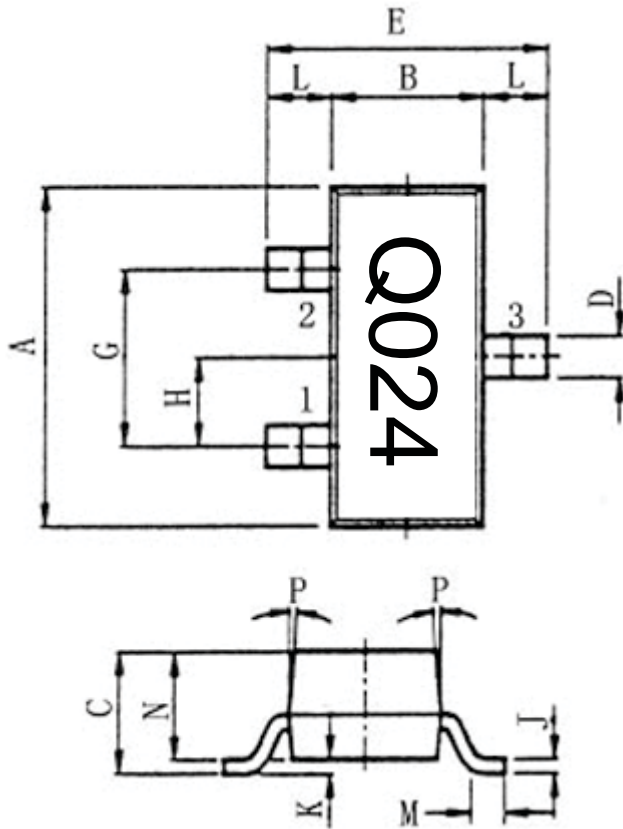


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension & Marking Information

SOT-23



A	2.90±0.20
B	1.30+0.20/-0.15
C	1.30MAX
D	0.40+0.15/-0.05
E	2.40+0.30/-0.20
G	1.90±0.2
H	0.95±0.1
J	0.10+0.10/-0.05
K	0.00~0.10
L	0.55±0.1
M	0.20MIN
N	1.00+0.20/-0.10
P	7°