

HRLF53N06H

60V N-Channel Trench MOSFET

Features

- Optimized for High Speed Switching, Logic Level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead free, Halogen Free

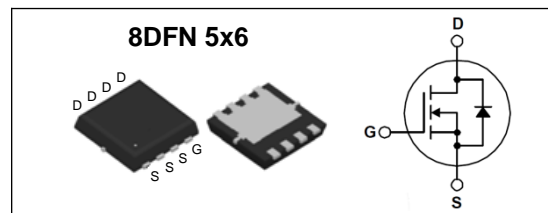
Application

- Synchronous Rectification in SMPS
- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Industrial

Key Parameters

Parameter	Value	Unit
BV_{DSS}	60	V
I_D	90	A
$R_{DS(on), typ @10V}$	4.1	m Ω
$R_{DS(on), typ @4.5V}$	5.6	m Ω

Package & Internal Circuit



Absolute Maximum Ratings $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current	$T_C = 25^\circ\text{C}$	90 A
		$T_C = 100^\circ\text{C}$	57 A
I_{DM}	Pulsed Drain Current	250	A
E_{AS}	Single Pulsed Avalanche Energy	L=1mH	80 mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	83 W
		$T_A = 25^\circ\text{C}$	2.0 W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient (steady state)	--	62	$^\circ\text{C}/\text{W}$

Electrical Characteristics $T_J=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	--	3.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\ \text{V}, I_D = 20\ \text{A}$	--	4.1	5.3	m Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 20\ \text{A}$	--	5.6	7.5	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}, I_D = 20\ \text{A}$	--	48	--	S

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\ \text{V}, I_D = 250\ \mu\text{A}$	60	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\ \text{V}, V_{GS} = 0\ \text{V}$	--	--	1	μA
		$V_{DS} = 60\ \text{V}, T_J = 100\text{ }^\circ\text{C}$	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	± 100	nA

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 30\ \text{V}, V_{GS} = 0\ \text{V}, f = 1.0\ \text{MHz}$	--	2274	--	pF
C_{oss}	Output Capacitance		--	793	--	pF
C_{riss}	Reverse Transfer Capacitance		--	35	--	pF
R_g	Gate Resistance	$V_{GS} = 0\ \text{V}, V_{DS} = 0\ \text{V}, f = 1\ \text{MHz}$	--	1.5	--	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DS} = 30\ \text{V}, I_D = 20\ \text{A}, R_G = 10\ \Omega$	--	11	--	ns
t_r	Turn-On Rise Time		--	7	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	--	ns
t_f	Turn-Off Fall Time		--	10	--	ns
$Q_{g(10V)}$	Total Gate Charge	$V_{DS} = 30\ \text{V}, I_D = 20\ \text{A}, V_{GS} = 10\ \text{V}$	--	36	--	nC
$Q_{g(4.5V)}$	Total Gate Charge		--	18	--	nC
Q_{gs}	Gate-Source Charge		--	4.5	--	nC
Q_{gd}	Gate-Drain Charge		--	7.5	--	nC

Source-Drain Diode Maximum Ratings and Characteristics

I_S	Continuous Source-Drain Diode Forward Current	--	--	90	A	
I_{SM}	Pulsed Source-Drain Diode Forward Current	--	--	250		
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 20\ \text{A}, V_{GS} = 0\ \text{V}$	--	0.9	1.2	V
t_{rr}	Reverse Recovery Time	$I_S = 20\ \text{A}, V_R = 30\ \text{V}, di_F/dt = 300\ \text{A}/\mu\text{s}$	--	30	--	ns
Q_{rr}	Reverse Recovery Charge		--	53	--	nC

Typical Characteristics

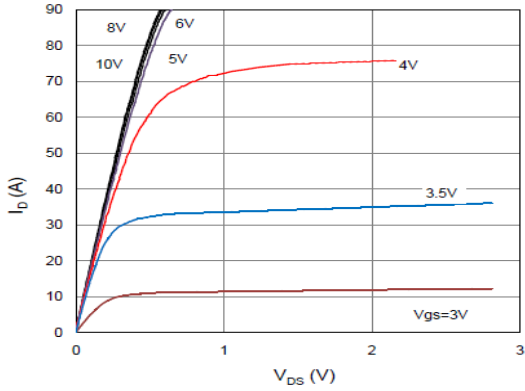


Figure 1. On Region Characteristics

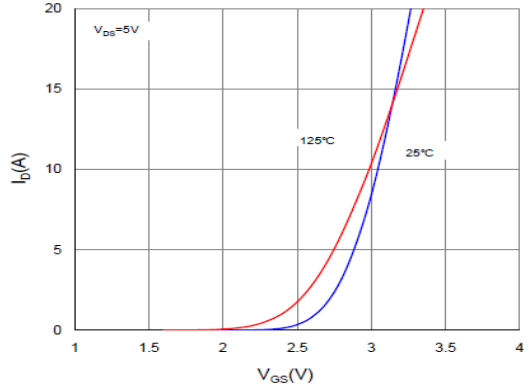


Figure 2. Transfer Characteristics

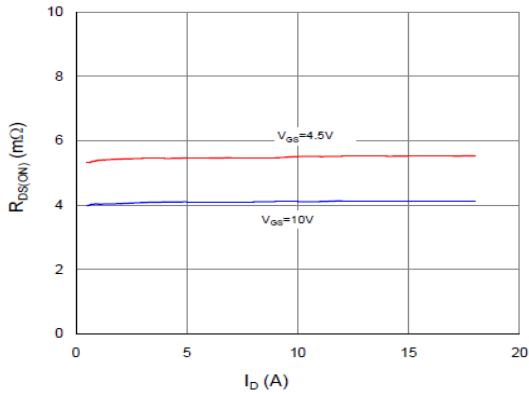


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

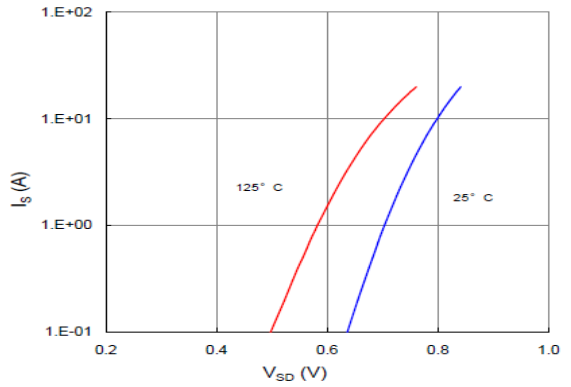


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

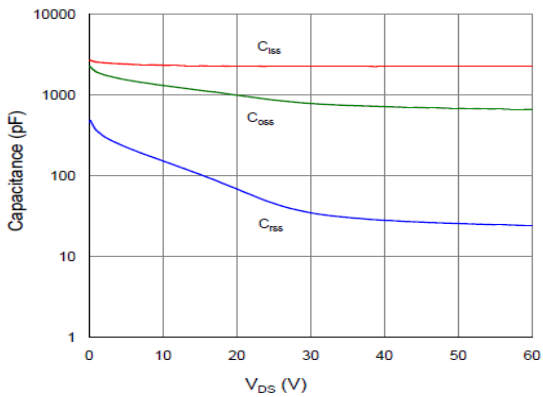


Figure 5. Capacitance Characteristics

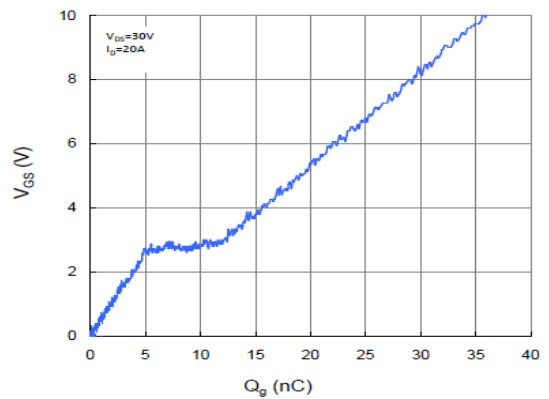


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

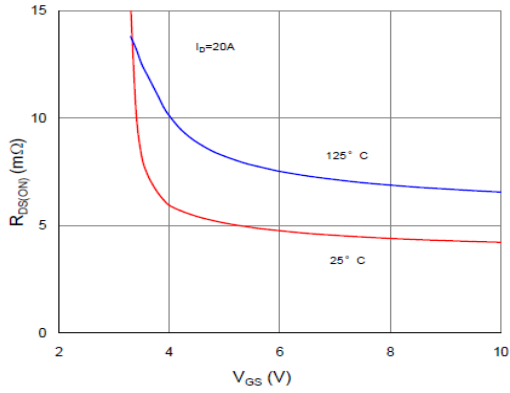


Figure 7. On-Resistance Variation vs Gate-Source Voltage

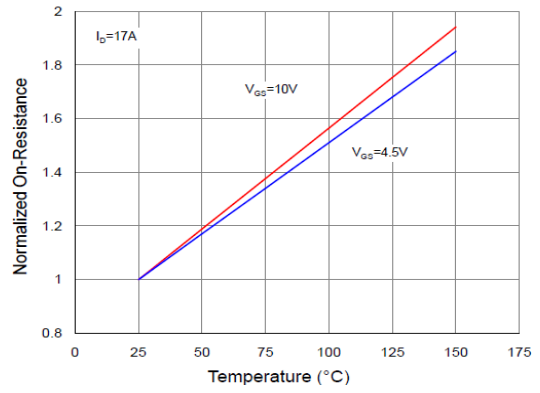


Figure 8. On-Resistance Variation vs Temperature

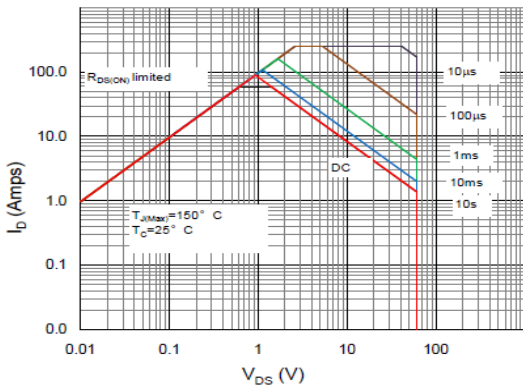


Figure 9. Maximum Safe Operating Area

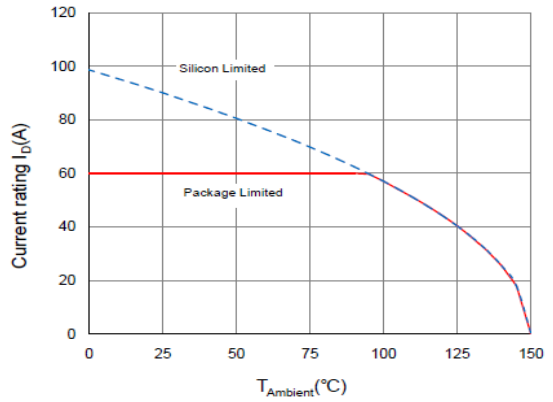


Figure 10. Maximum Drain Current vs Case Temperature

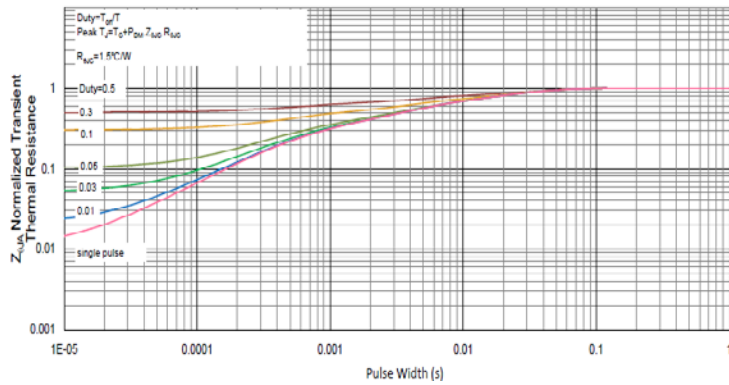


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

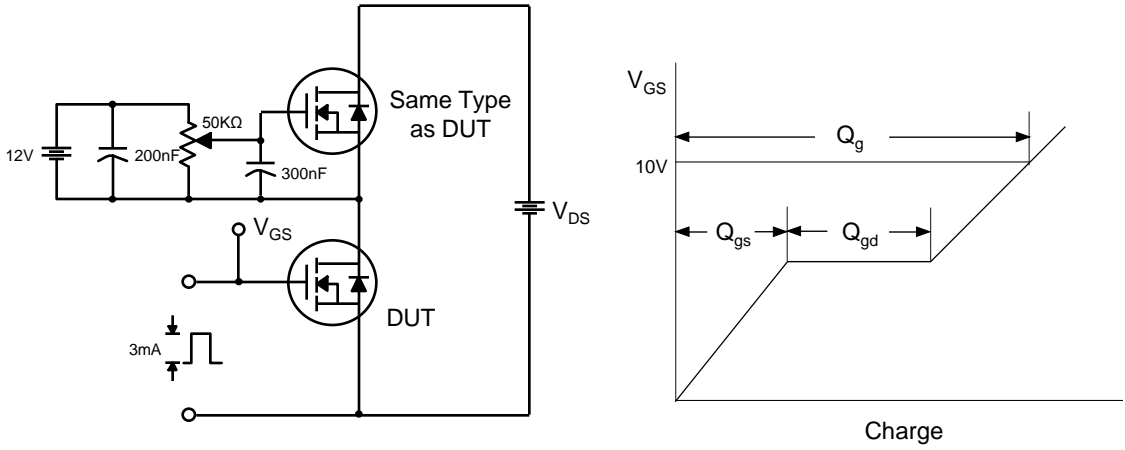


Fig 13. Resistive Switching Test Circuit & Waveforms

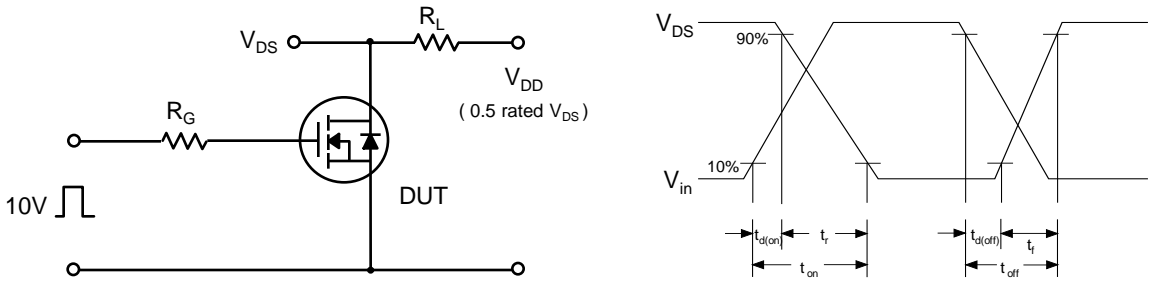


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

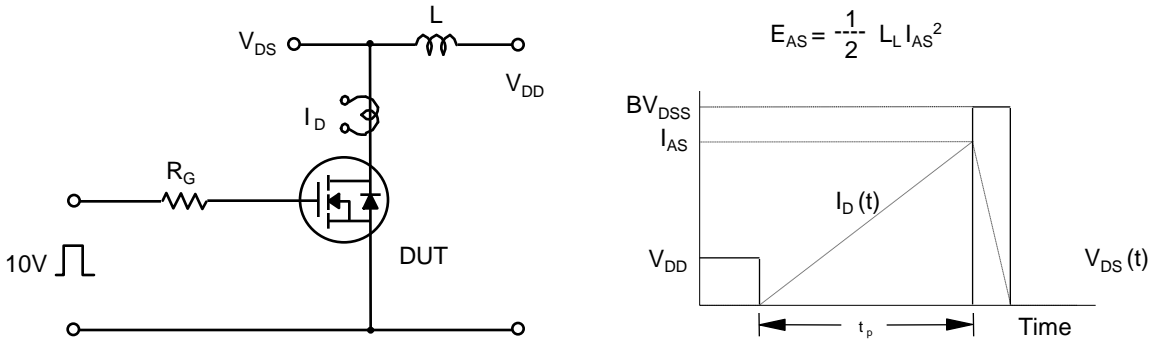
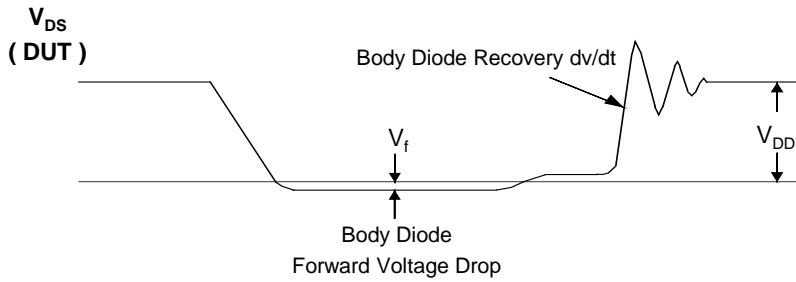
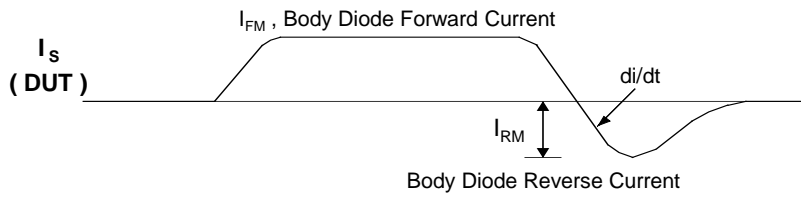
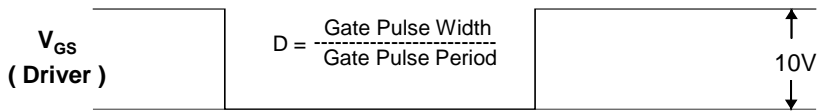
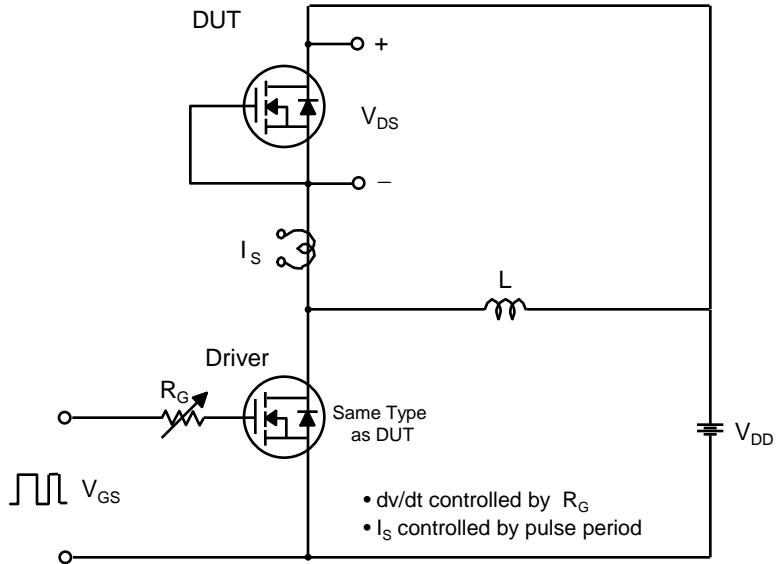
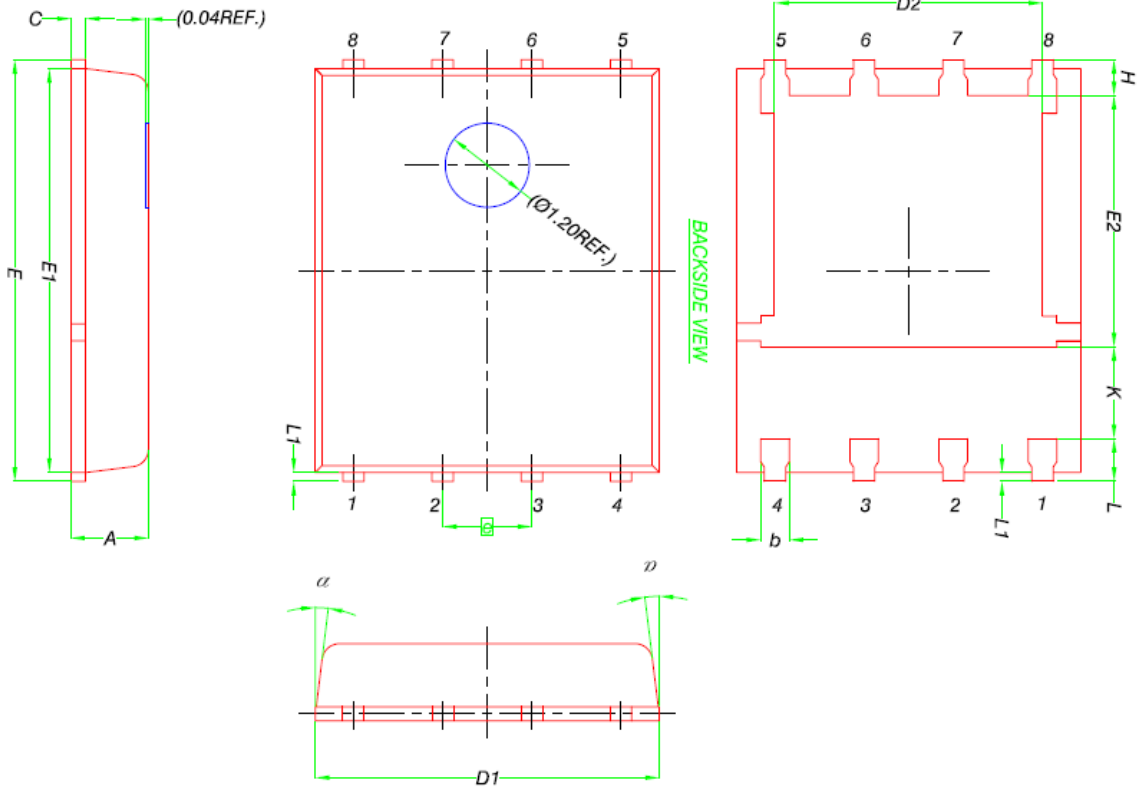


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

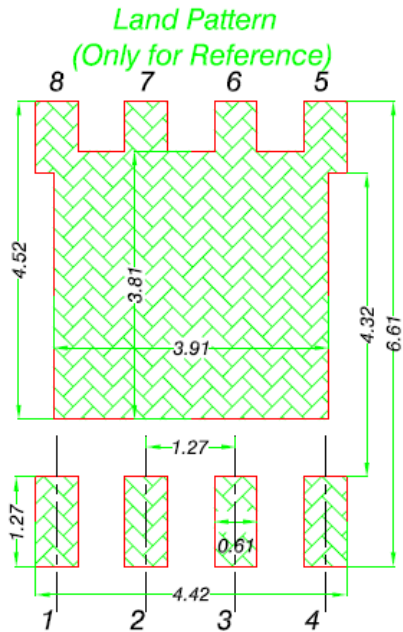


Package Dimension

8DFN 5x6



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°



Revision History

VERSION	DESCRIPTION	DATE	APPROVED
0	Initiate specification	20161208	YGCHO
1			
2			
3			
4			
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9			
10			