

HRLO250N10K

100V N-Channel Trench MOSFET

Features

- High Dense Cell Design
- Reliable and Rugged
- Advanced Trench Process Technology

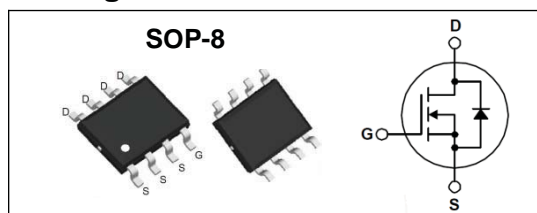
Application

- Power Management in Inverter System
- Synchronous Rectification

Key Parameters

Parameter	Value	Unit
BV_{DSS}	100	V
I_D	7.9	A
$R_{DS(on)}$, typ @10V	20	m Ω
$R_{DS(on)}$, typ @4.5V	22	m Ω

Package & Internal Circuit



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	100	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current	$T_A = 25^\circ\text{C}$	7.9 A
		$T_A = 70^\circ\text{C}$	6.3 A
I_{DM}	Pulsed Drain Current (Note 1)	32	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	96	mJ
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	3.1 W
		$T_A = 70^\circ\text{C}$	2.0 W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Lead	--	24	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient ($t \leq 10\text{s}$)	--	40	$^\circ\text{C}/\text{W}$
	Junction-to-Ambient (steady state)	--	75	$^\circ\text{C}/\text{W}$

Electrical Characteristics $T_J=25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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On Characteristics

V_{GS}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	--	2.4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\ \text{V}, I_D = 7.9\ \text{A}$	--	20.0	25.0	m Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 6\ \text{A}$	--	22.0	27.5	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5, I_D = 7.9\ \text{A}$	--	28	--	S

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\ \text{V}, I_D = 250\ \mu\text{A}$	100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}$	--	--	1	μA
		$V_{DS} = 80\ \text{V}, T_J = 125\text{ }^\circ\text{C}$	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	± 100	nA

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}, V_{GS} = 0\ \text{V}, f = 1.0\ \text{MHz}$	--	4200	--	pF
C_{oss}	Output Capacitance		--	190	--	pF
C_{riss}	Reverse Transfer Capacitance		--	135	--	pF
R_g	Gate Resistance	$V_{GS} = 0\ \text{V}, V_{DS} = 0\ \text{V}, f = 1\ \text{MHz}$	--	1.6	--	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Time	$V_{DS} = 50\ \text{V}, I_D = 7.9\ \text{A}, R_G = 6\ \Omega$	--	32	--	ns
t_r	Turn-On Rise Time		--	23	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	220	--	ns
t_f	Turn-Off Fall Time		--	25	--	ns
Q_g	Total Gate Charge	$V_{DS} = 80\ \text{V}, I_D = 7.9\ \text{A}, V_{GS} = 10\ \text{V}$	--	90	120	nC
Q_{gs}	Gate-Source Charge		--	9	--	nC
Q_{gd}	Gate-Drain Charge		--	18	--	nC

Source-Drain Diode Maximum Ratings and Characteristics

I_S	Continuous Source-Drain Diode Forward Current	--	--	7.9	A	
I_{SM}	Pulsed Source-Drain Diode Forward Current	--	--	32		
V_{SD}	Source-Drain Diode Forward Voltage	$I_S = 7.9\ \text{A}, V_{GS} = 0\ \text{V}$	--	--	1.3	V
t_{rr}	Reverse Recovery Time	$I_S = 7.9\ \text{A}, V_{GS} = 0\ \text{V}, di_F/dt = 100\ \text{A}/\mu\text{s}$	--	45	--	ns
Q_{rr}	Reverse Recovery Charge		--	75	--	nC

Notes :

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L=1\ \text{mH}, I_{AS}=12\ \text{A}, V_{DD}=25\ \text{V}, R_G=25\ \Omega,$ Starting $T_J=25\text{ }^\circ\text{C}$

Typical Characteristics

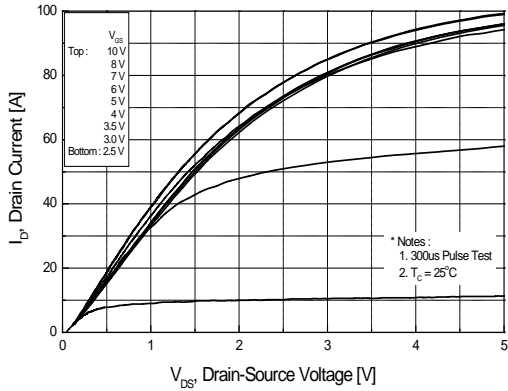


Figure 1. On Region Characteristics

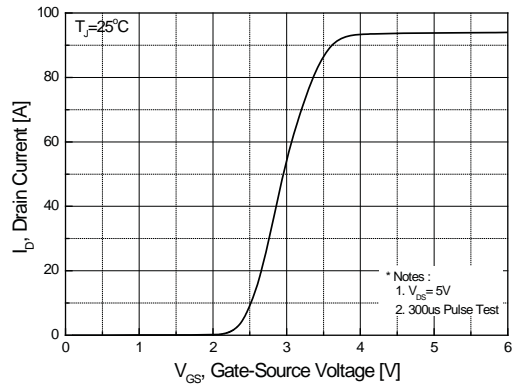


Figure 2. Transfer Characteristics

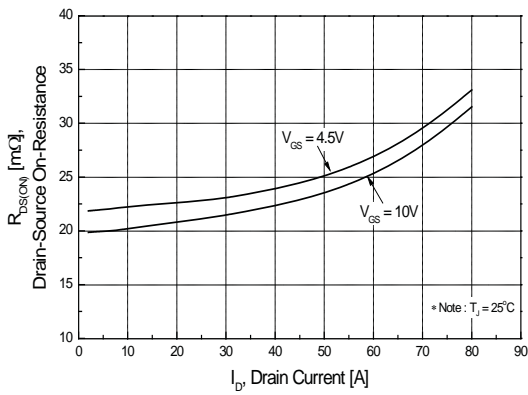


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

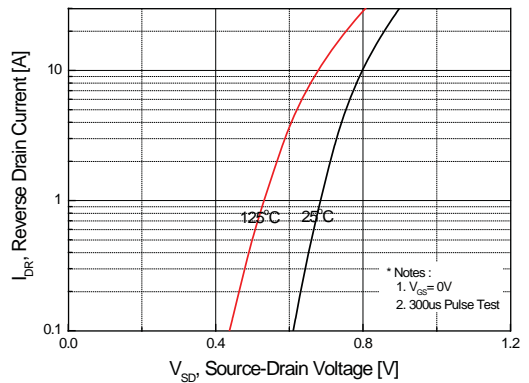


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

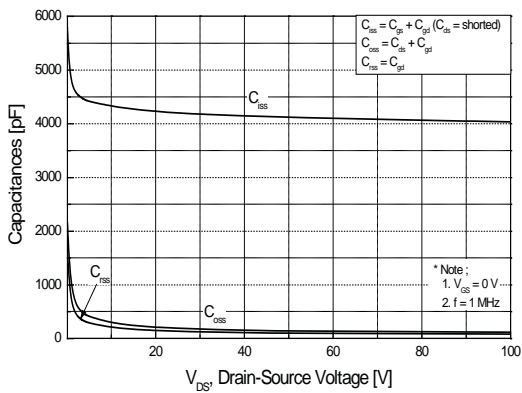


Figure 5. Capacitance Characteristics

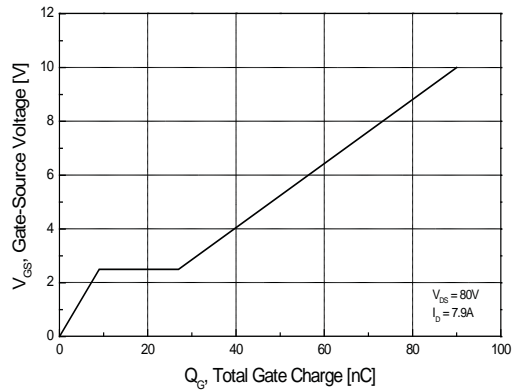


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

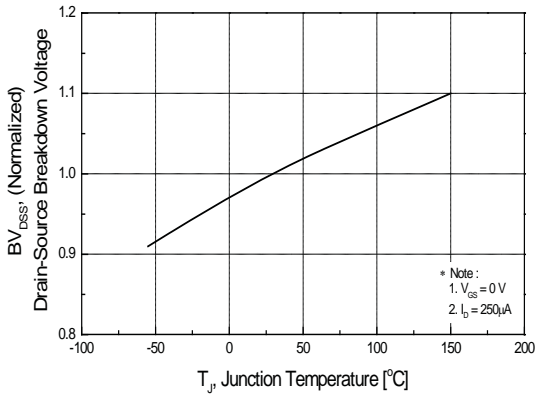


Figure 7. Breakdown Voltage Variation vs Temperature

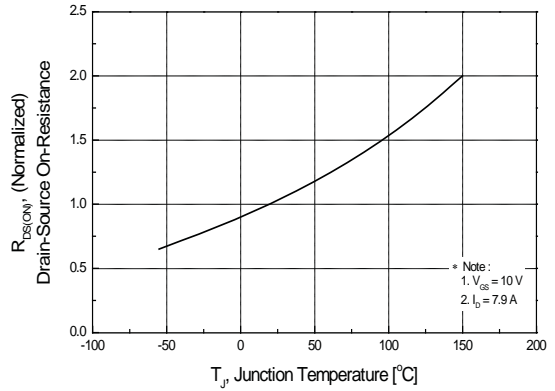


Figure 8. On-Resistance Variation vs Temperature

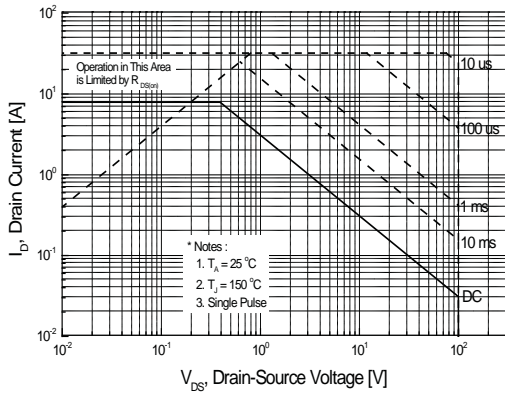


Figure 9. Maximum Safe Operating Area

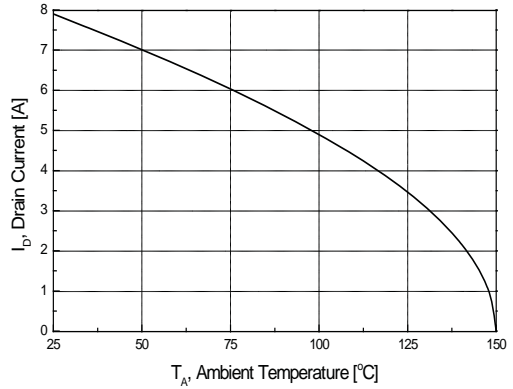


Figure 10. Maximum Drain Current vs Case Temperature

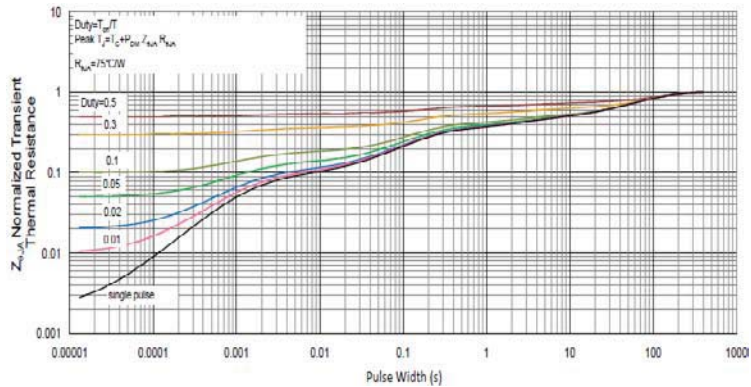


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform



Fig 13. Resistive Switching Test Circuit & Waveforms



Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms



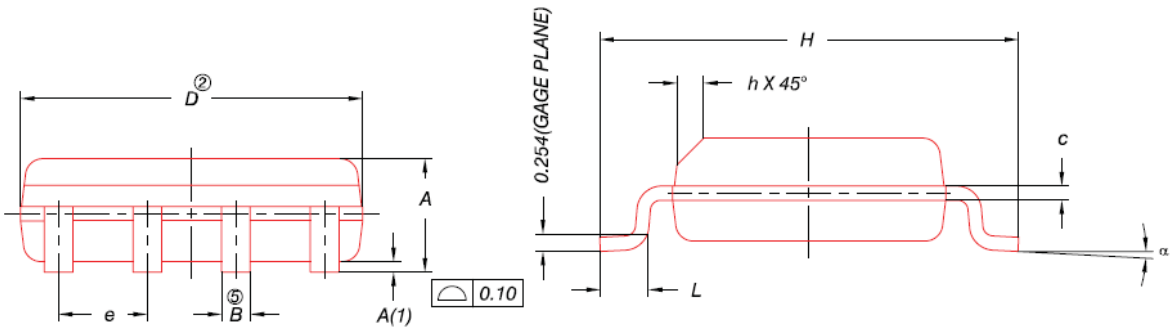
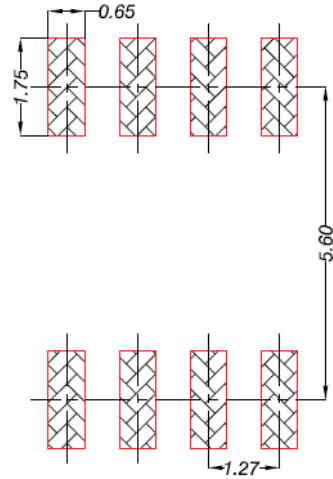
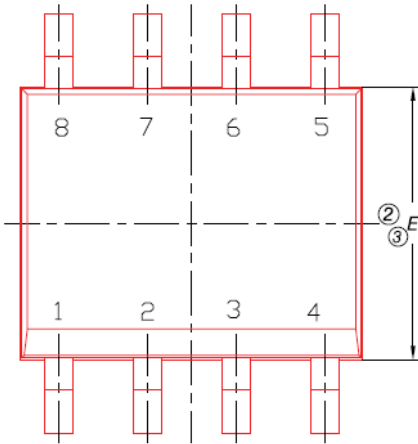
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

SOP-8

Land Pattern
(Only for Reference)



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.35	1.55	1.75
A(1)	0.10	0.18	0.25
B	0.38	0.45	0.51
C	0.19	0.22	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
e	1.27 BSC		
H	5.80	6.00	6.20
L	0.50	0.72	0.93
α	0°	4°	8°
h	0.25	0.38	0.50