

# HRLP33N03K

## 30V N-Channel Trench MOSFET

### Features

- Low Dense Cell Design, Logic Level
- Reliable and Rugged
- Advanced Trench Process Technology
- 100% UIS Tested, 100% Rg Tested

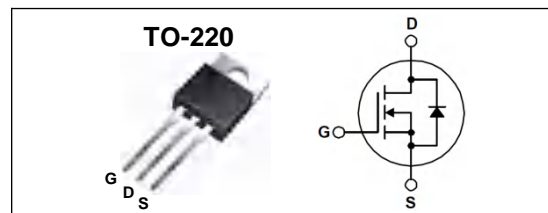
### Application

- Power Management in Inverter System
- Synchronous Rectification

### Key Parameters

Parameter	Value	Unit
$BV_{DSS}$	30	V
$I_D$ (Silicon Limited)	150	A
$R_{DS(on)}$ , typ @10V	2.7	m $\Omega$
$R_{DS(on)}$ , typ @4.5V	3.2	m $\Omega$

### Package & Internal Circuit



### Absolute Maximum Ratings $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units	
$V_{DSS}$	Drain-Source Voltage	30	V	
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V	
$I_D$	Drain Current (Silicon Limited)	$T_C = 25^\circ\text{C}$	150	A
		$T_C = 100^\circ\text{C}$	105	A
	Drain Current (Package Limited)	$T_C = 25^\circ\text{C}$	120	A
$I_{DM}$	Pulsed Drain Current	525	A	
$E_{AS}$	Single Pulsed Avalanche Energy	L=1mH	1200	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	115	W
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$	

### Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	$^\circ\text{C}/\text{W}$

**Electrical Characteristics**  $T_J=25\text{ }^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>On Characteristics</b>						
$V_{GS}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.7	--	2.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\ \text{V}, I_D = 30\ \text{A}$	--	2.7	3.3	m $\Omega$
		$V_{GS} = 4.5\ \text{V}, I_D = 25\ \text{A}$	--	3.2	4.0	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\ \text{V}, I_D = 30\ \text{A}$	--	65	--	S
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\ \text{V}, I_D = 250\ \mu\text{A}$	30	--	--	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\ \text{V}, V_{GS} = 0\ \text{V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 24\ \text{V}, T_J = 125\text{ }^\circ\text{C}$	--	--	100	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$	--	--	$\pm 100$	nA
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\ \text{V}, V_{GS} = 0\ \text{V}, f = 1.0\ \text{MHz}$	--	4900	--	pF
$C_{oss}$	Output Capacitance		--	550	--	pF
$C_{rss}$	Reverse Transfer Capacitance		--	500	--	pF
$R_g$	Gate Resistance	$V_{GS} = 0\ \text{V}, V_{DS} = 0\ \text{V}, f = 1\ \text{MHz}$	--	1	--	$\Omega$
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Time	$V_{DS} = 15\ \text{V}, I_D = 30\ \text{A}, R_G = 6\ \Omega$	--	30	--	ns
$t_r$	Turn-On Rise Time		--	50	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	230	--	ns
$t_f$	Turn-Off Fall Time		--	70	--	ns
$Q_{g(10V)}$	Total Gate Charge	$V_{DS} = 24\ \text{V}, I_D = 30\ \text{A}, V_{GS} = 10\ \text{V}$	--	110	--	nC
$Q_{g(4.5V)}$	Total Gate Charge		--	50	--	nC
$Q_{gs}$	Gate-Source Charge		--	15	--	nC
$Q_{gd}$	Gate-Drain Charge		--	20	--	nC
<b>Source-Drain Diode Characteristics</b>						
$V_{SD}$	Source-Drain Diode Forward Voltage	$I_S = 30\ \text{A}, V_{GS} = 0\ \text{V}$	--	--	1.3	V
$t_{rr}$	Reverse Recovery Time	$I_S = 25\ \text{A}, V_{GS} = 0\ \text{V}, di_F/dt = 50\ \text{A}/\mu\text{s}$	--	60	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	30	--	nC

Typical Characteristics

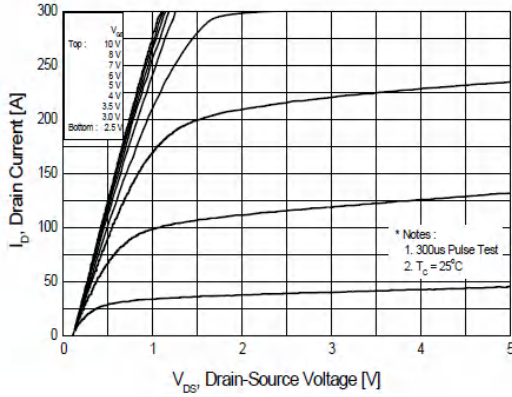


Figure 1. On Region Characteristics

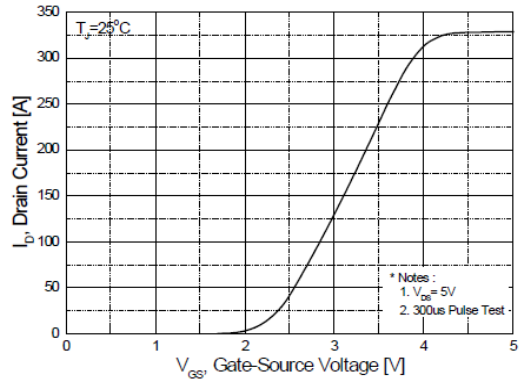


Figure 2. Transfer Characteristics

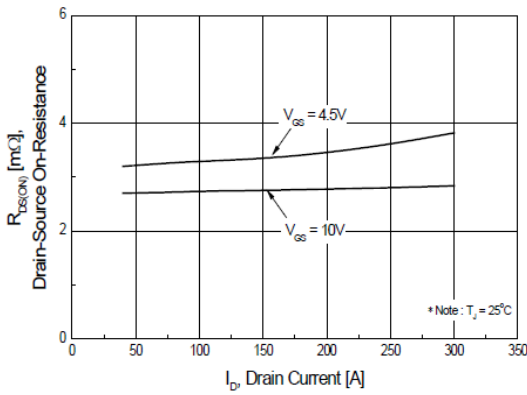


Figure 3. On Resistance Variation vs Drain Current and Gate Voltage

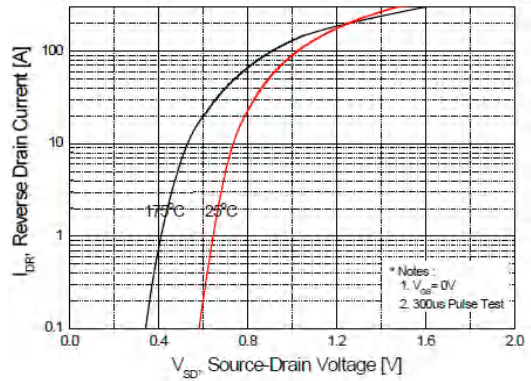


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

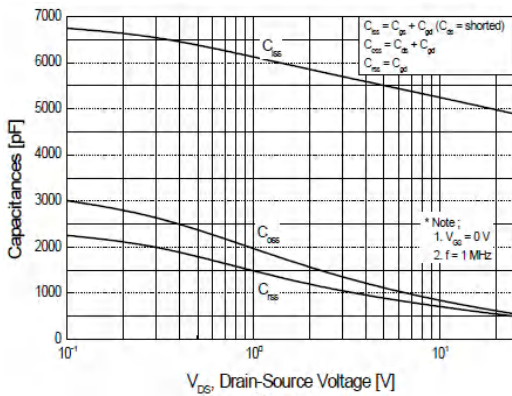


Figure 5. Capacitance Characteristics

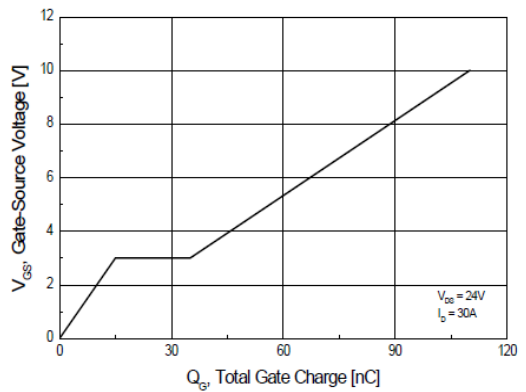
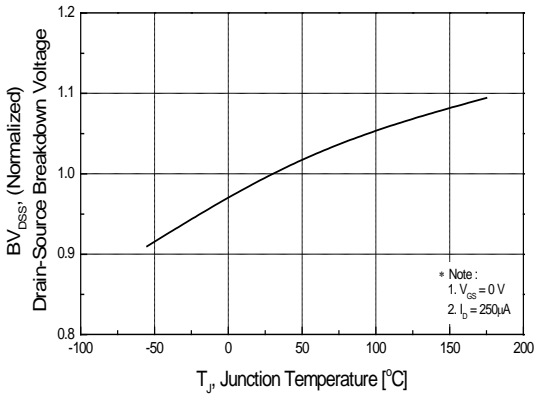
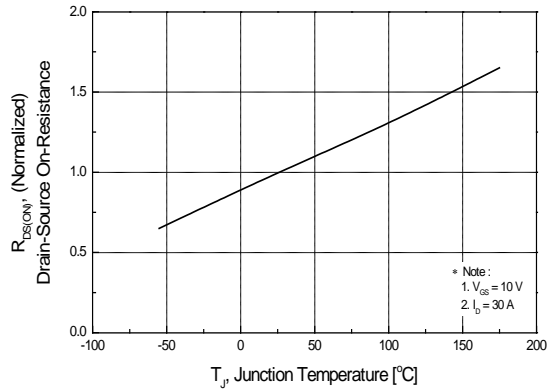


Figure 6. Gate Charge Characteristics

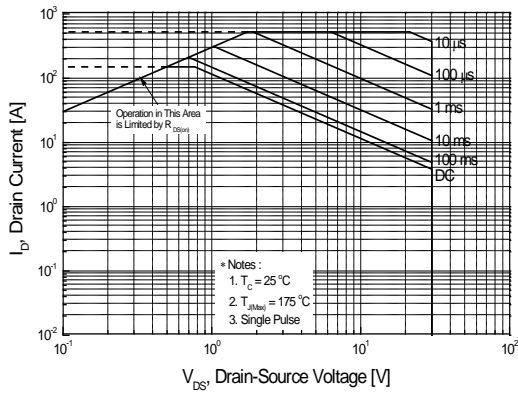
**Typical Characteristics (continued)**



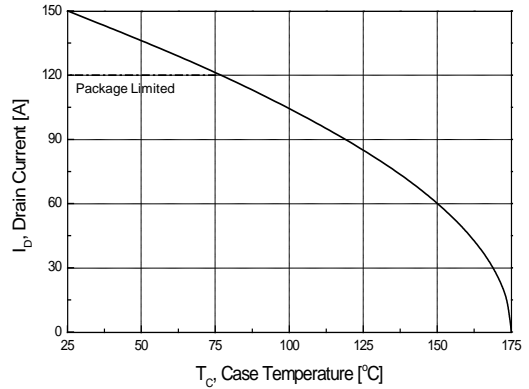
**Figure 7. On-Resistance Variation vs Gate-Source Voltage**



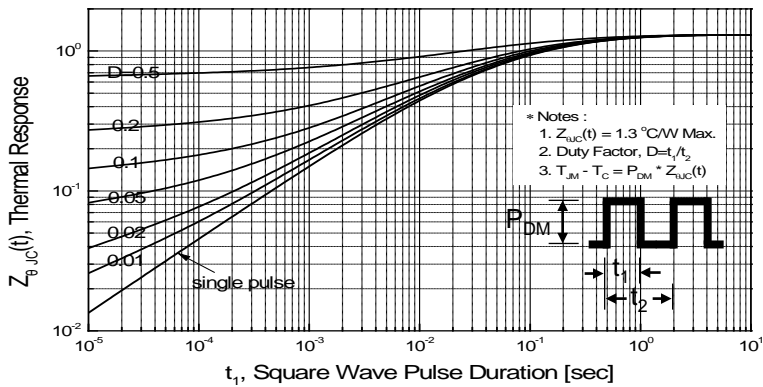
**Figure 8. On-Resistance Variation vs Temperature**



**Figure 9. Maximum Safe Operating Area**

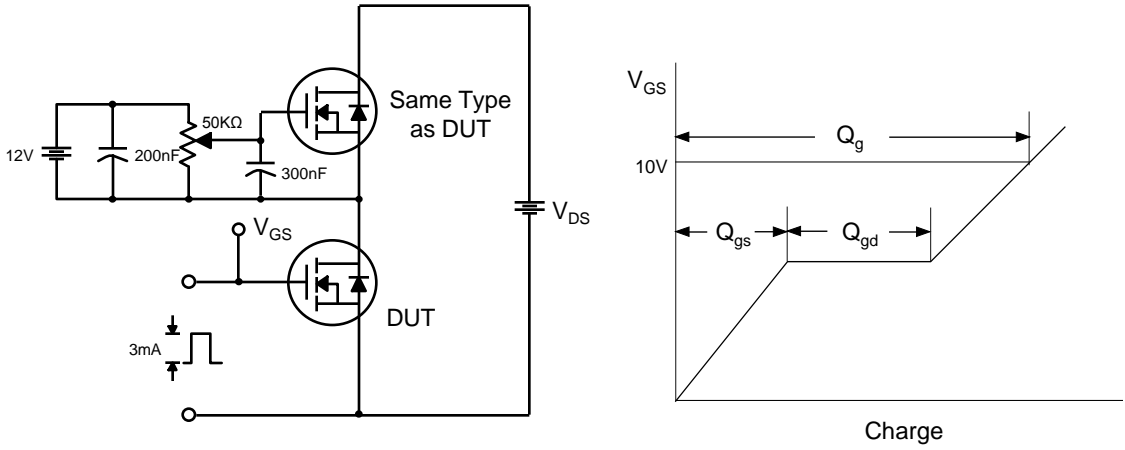


**Figure 10. Maximum Drain Current vs Case Temperature**

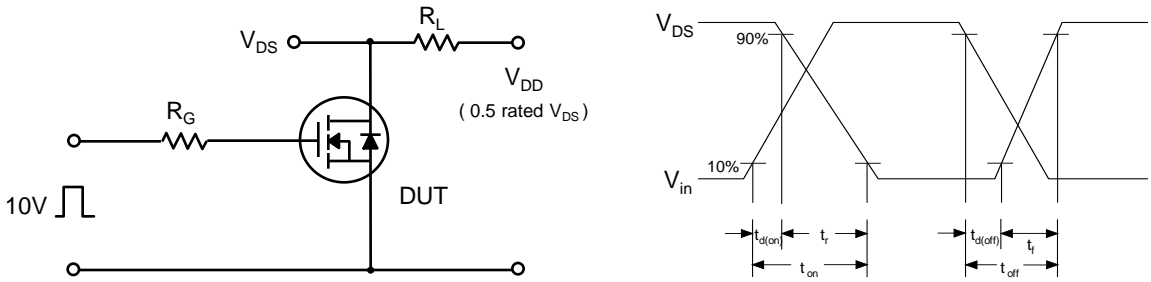


**Figure 11. Transient Thermal Response Curve**

**Fig 12. Gate Charge Test Circuit & Waveform**



**Fig 13. Resistive Switching Test Circuit & Waveforms**



**Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms**

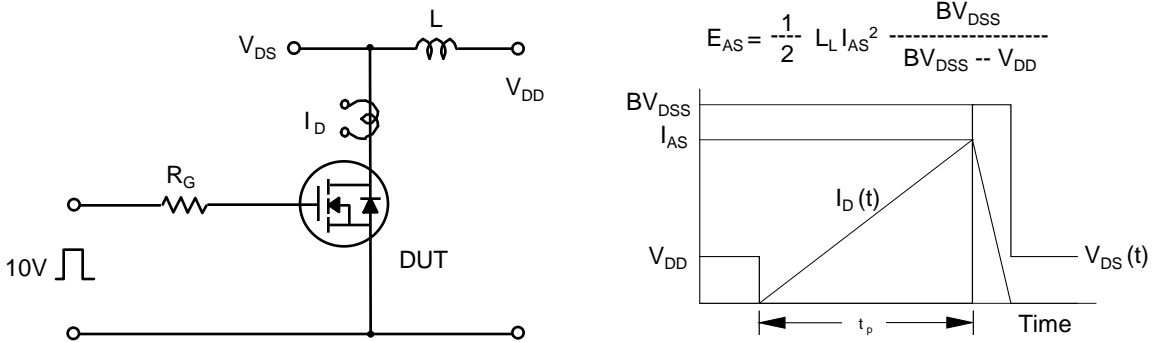
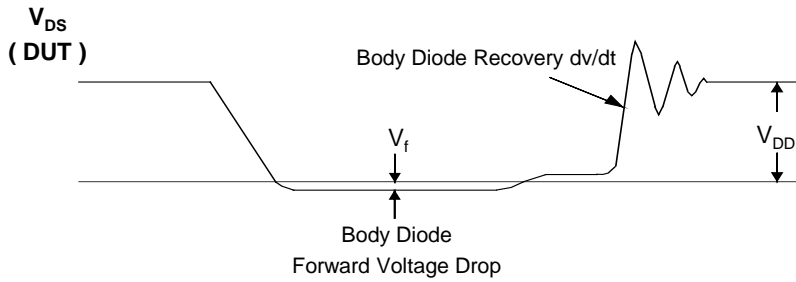
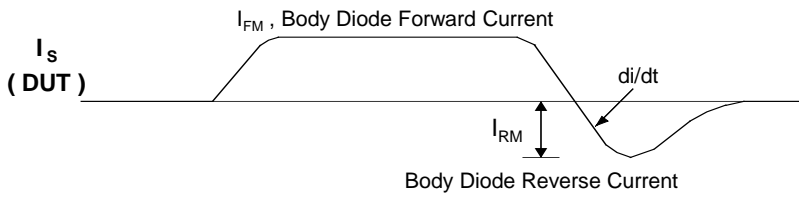
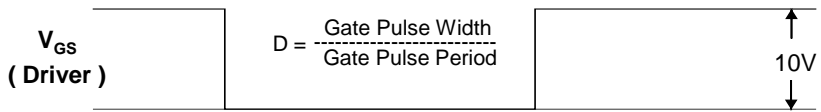
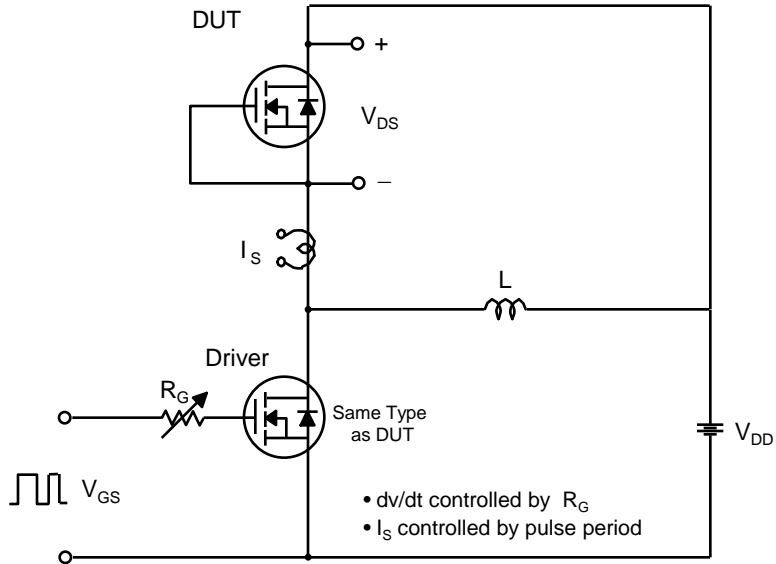


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

TO-220

