

# HRLP72N06

## 65V N-Channel Trench MOSFET

### Features

- High Speed Power Switching, Logic Level
- Enhanced Body diode dv/dt capability
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead free, Halogen Free

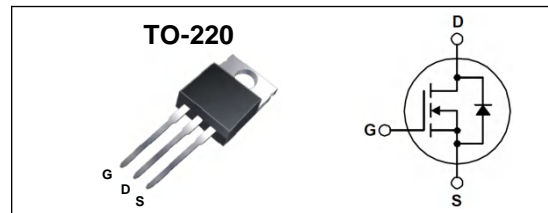
### Application

- Synchronous Rectification in SMPS
- Hard Switching and High-Speed Circuit
- DC/DC in Telecoms and Industrial

### Key Parameters

Parameter	Value	Unit
$BV_{DSS}$	65	V
$I_D$	90	A
$R_{DS(on), max @10V}$	7.2	m $\Omega$
$R_{DS(on), max @4.5V}$	12.5	m $\Omega$

### Package & Internal Circuit



### Absolute Maximum Ratings $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units	
$V_{DSS}$	Drain-Source Voltage	65	V	
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V	
$I_D$	Drain Current	$T_C = 25^\circ\text{C}$	90	A
		$T_C = 100^\circ\text{C}$	53	A
$I_{DM}$	Pulsed Drain Current	292	A	
$E_{AS}$	Single Pulsed Avalanche Energy	12.5	mJ	
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	104	W
		$T_A = 25^\circ\text{C}$	2.0	W
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$	

### Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient (steady state)	--	62	$^\circ\text{C/W}$

**Electrical Characteristics**  $T_J=25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>On Characteristics</b>						
$V_{GS}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.0	--	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	--	6.0	7.2	$\text{m}\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$	--	9.6	12.5	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 3 \text{ A}$	--	10	--	S
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	65	--	--	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 48 \text{ V}, T_J = 85^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	$\pm 1$	$\mu\text{A}$
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	--	1575	--	$\text{pF}$
$C_{oss}$	Output Capacitance		--	785	--	$\text{pF}$
$C_{rss}$	Reverse Transfer Capacitance		--	30	--	$\text{pF}$
$R_g$	Gate Resistance	$V_{GS} = 0 \text{ V}, V_{DS} = 0 \text{ V}, f = 1\text{MHz}$	--	1.25	--	$\Omega$
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Time	$V_{DS} = 30 \text{ V}, I_D = 10 \text{ A}, R_G = 10 \Omega$	--	15	--	ns
$t_r$	Turn-On Rise Time		--	21	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	136	--	ns
$t_f$	Turn-Off Fall Time		--	27	--	ns
$Q_g$	Total Gate Charge	$V_{DS} = 30 \text{ V}, I_D = 10 \text{ A}, V_{GS} = 10 \text{ V}$	--	38.5	--	nC
$Q_{gs}$	Gate-Source Charge		--	7.5	--	nC
$Q_{gd}$	Gate-Drain Charge		--	4.5	--	nC
<b>Source-Drain Diode Characteristics</b>						
$V_{SD}$	Source-Drain Diode Forward Voltage	$I_S = 1 \text{ A}, V_{GS} = 0 \text{ V}$	--	0.9	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_S = 10 \text{ A}, V_{GS} = 10 \text{ V}, di_F/dt = 100 \text{ A}/\mu\text{s}$	--	48.4	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	54.2	--	nC

**Notes :**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $I_{AS}=5\text{A}, V_{DD}=30\text{V}, R_G=25\Omega, \text{Starting } T_J=25^\circ\text{C}$

Typical Characteristics

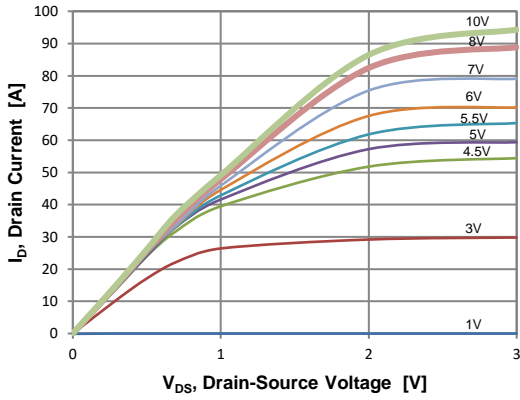


Figure 1. On Region Characteristics

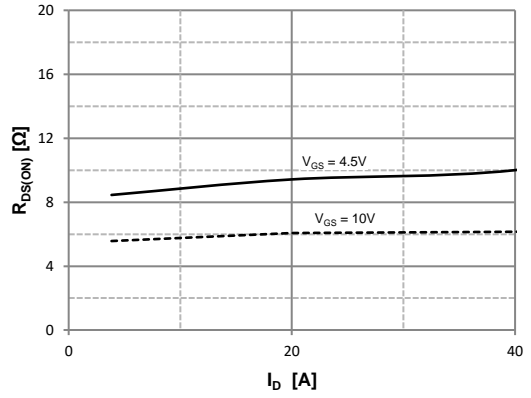


Figure 2. On Resistance Variation vs Drain Current and Gate Voltage

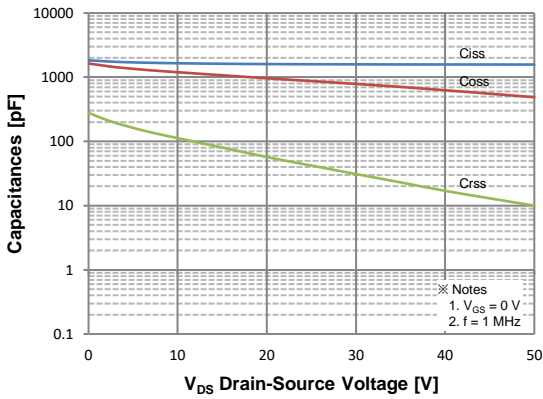


Figure 3. Capacitance Characteristics

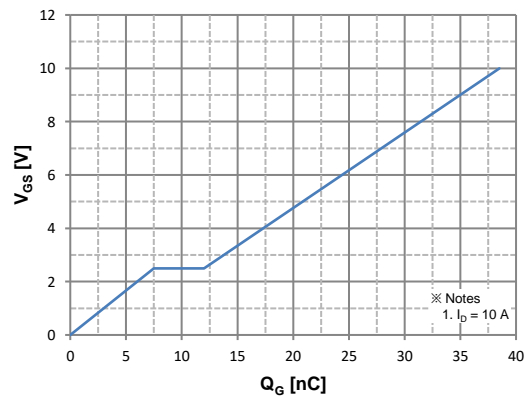


Figure 4. Gate Charge Characteristics

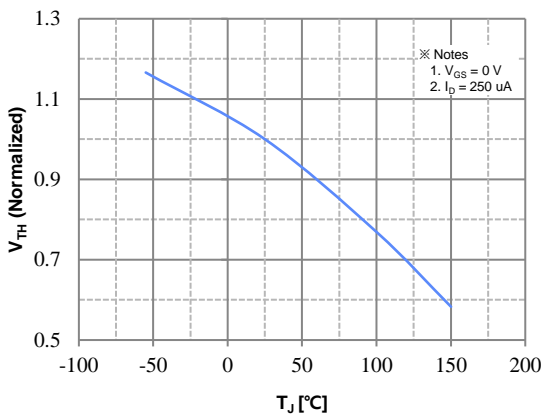


Figure 4. Gate Threshold Voltage vs Temperature

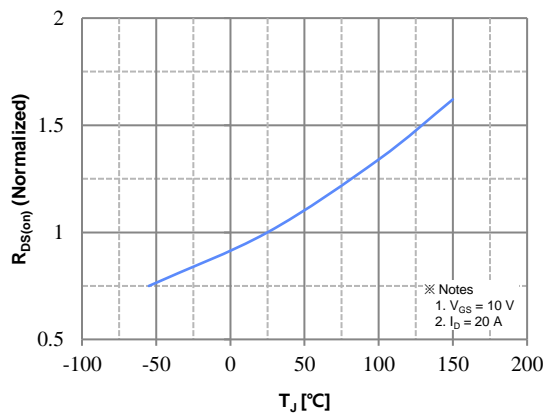
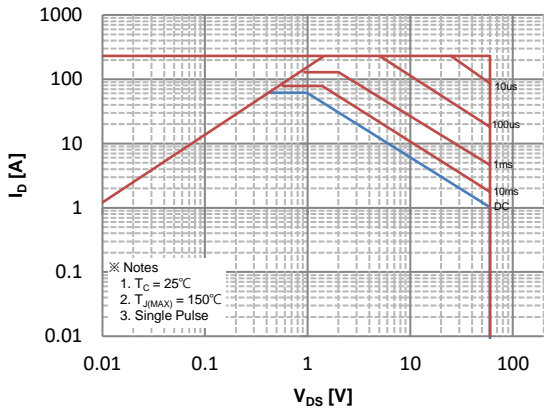
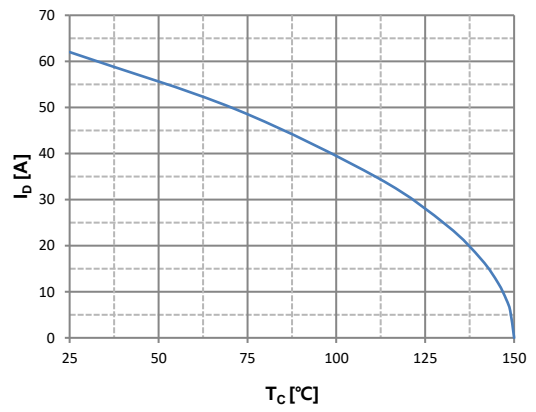


Figure 6. On-Resistance Variation vs Temperature

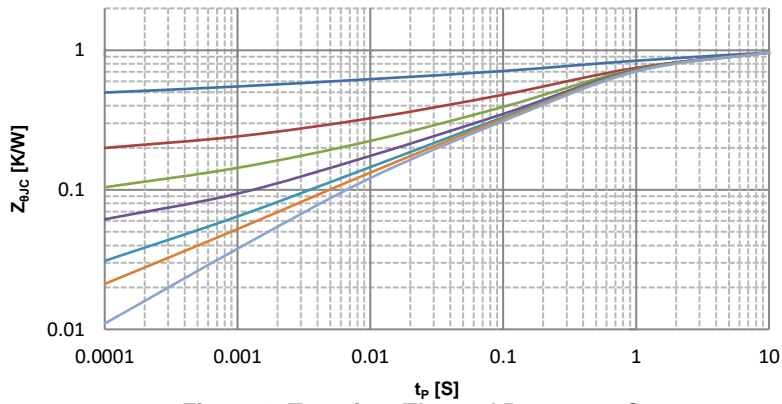
**Typical Characteristics (continued)**



**Figure 7. Maximum Safe Operating Area**

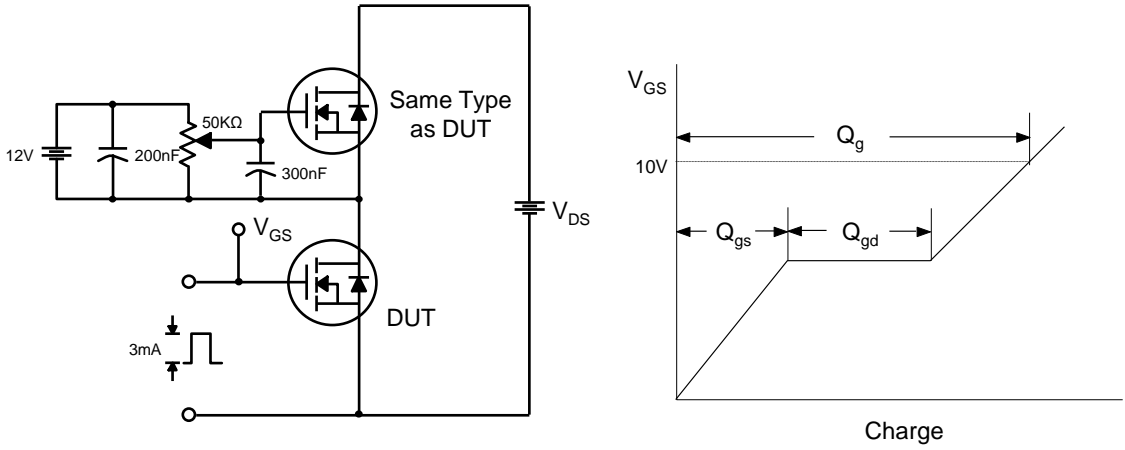


**Figure 8. Maximum Drain Current vs Case Temperature**

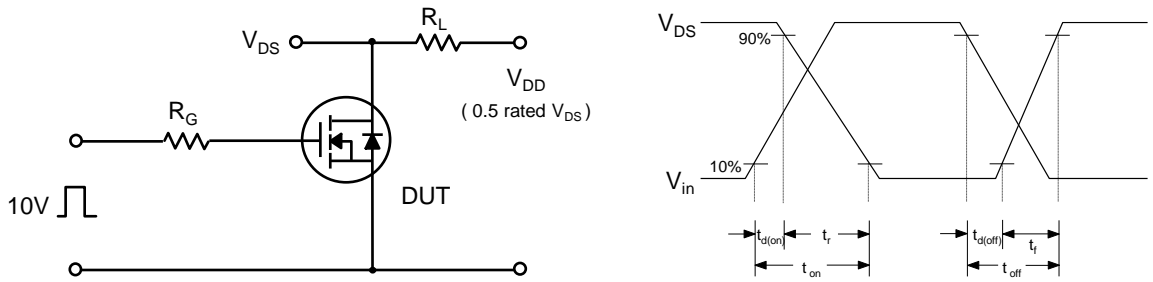


**Figure 9. Transient Thermal Response Curve**

**Fig 12. Gate Charge Test Circuit & Waveform**



**Fig 13. Resistive Switching Test Circuit & Waveforms**



**Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms**

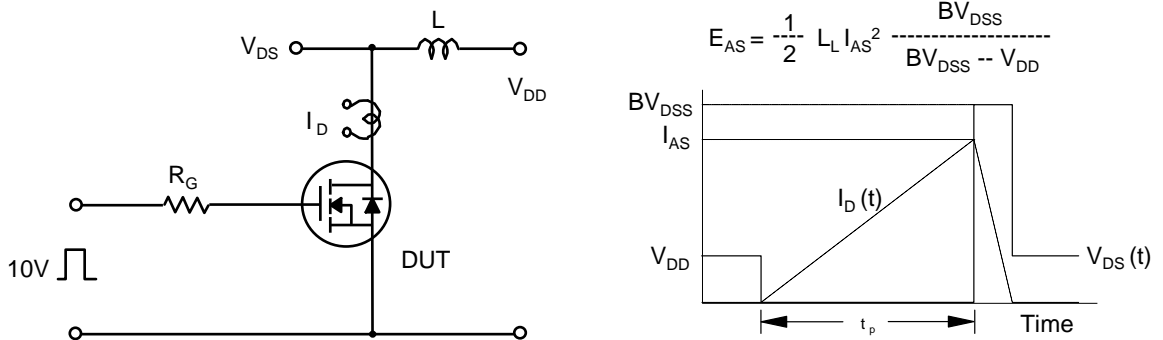
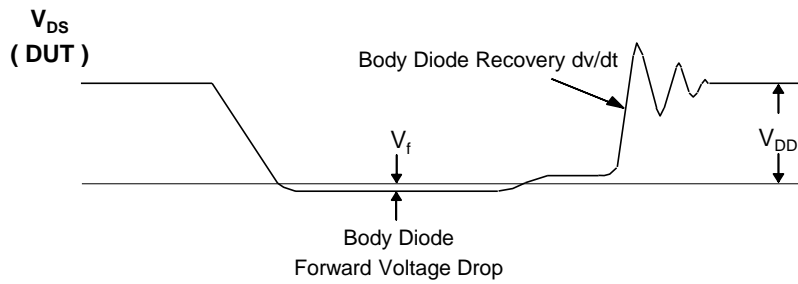
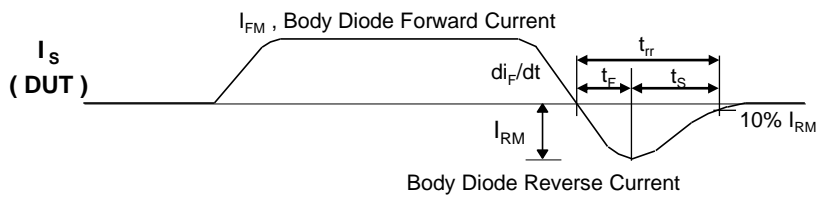


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimension

TO-220

