

## HS-4424RH, HS-4424EH, HS-4424BRH, HS-4424BEH

Radiation Hardened Dual, Non-Inverting Power MOSFET Drivers

The radiation hardened [HS-4424RH](#), [HS-4424EH](#), [HS-4424BRH](#) and [HS-4424BEH](#) are non-inverting, dual, monolithic high-speed MOSFET drivers designed to convert TTL level signals into high current outputs at voltages up to 18V.

The inputs of these devices are TTL compatible and can be directly driven by our HS-1825ARH PWM device or by our ACS/ACTS and HCS/HCTS type logic devices. The fast rise times and high current outputs allow very quick control of high gate capacitance power MOSFETs in high frequency applications.

The high current outputs minimize power losses in MOSFETs by rapidly charging and discharging the gate capacitance. The output stage incorporates a low voltage lockout circuit that puts the outputs into a three-state mode when the supply voltage drops below 10V for the HS-4424RH, HS-4424EH and 7.5V for the HS-4424BRH, HS-4424BEH.

Constructed with the dielectrically isolated Rad Hard Silicon Gate (RSG) BiCMOS process, these devices are immune to single event latch-up and have been specifically designed to provide highly reliable performance in harsh radiation environments.

Detailed Electrical Specifications for these devices are contained in SMD [5962-99560](#).

### Related Literature

For a full list of related documents, visit our website:

- [HS-4424RH](#), [HS-4424EH](#), [HS-4424BRH](#) and [HS-4424BEH](#) device pages

### Features

- Electrically screened to DESC SMD # [5962-99560](#)
- QML qualified per MIL-PRF-38535 requirements
- Radiation environment
  - High dose rate (50-300rad(Si)/s): 300krad(Si)
  - Latch-up immune
  - Low dose rate (0.01rad(Si)/s): 50krad(Si) (EH products only)
- I<sub>PEAK</sub>: >2A (min)
- Matched rise and fall times (C<sub>L</sub> = 4300pF): 75ns (maximum)
- Low voltage lockout feature
  - HS-4424RH, HS-4424EH: <10.0V
  - HS-4424BRH, HS-4424BEH: <7.5V
- Wide supply voltage range: 12V to 18V
- Prop delay: 250ns (maximum)
- Consistent delay times with V<sub>CC</sub> changes
- Low power consumption
  - 40mW with inputs high
  - 20mW with inputs low
- Low equivalent input capacitance: 3.2pF (typical)
- ESD protected: >4000V

### Applications

- Switching power supplies
- DC/DC converters
- Motor controllers

**Table 1. Table of Differences**

Part Number	Dose Rate (rad(Si)/s)
HS-4424RH, HS-4424BRH	50-300
HS-4424EH, HS-4424BEH	0.01

# 1. Overview

## 1.1 Ordering Information

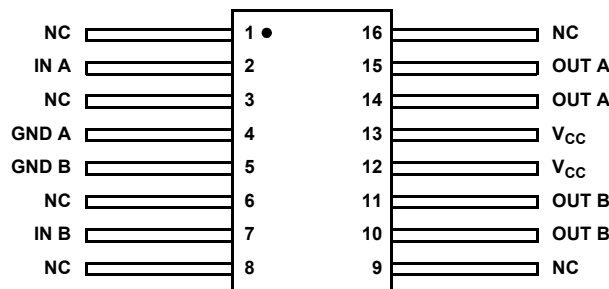
Ordering SMD Number (Note 2)	Part Number (Notes 1, 3)	Temperature Range (°C)	Package (RoHS Compliant)	Pkg. Dwg. #
5962F9956004V9A	HS0-4424BEH-Q	-55 to +125	DIE	
5962F9956002V9A	HS0-4424BRH-Q	-55 to +125	DIE	
N/A	HS0-4424BRH/SAMPLE	-55 to +125	DIE SAMPLE	
5962F9956003V9A	HS0-4424EH-Q	-55 to +125	DIE	
5962F9956001V9A	HS0-4424RH-Q	-55 to +125	DIE	
N/A	HS0-4424RH/SAMPLE	-55 to +125	DIE SAMPLE	
5962F9956001VXC	HS9-4424RH-Q	-55 to +125	16 Ld Flatpack	K16.A
5962F9956004VXC	HS9-4424BEH-Q	-55 to +125	16 Ld Flatpack	K16.A
5962F9956003VXC	HS9-4424EH-Q	-55 to +125	16 Ld Flatpack	K16.A
5962F9956002QXC	HS9-4424BRH-8	-55 to +125	16 Ld Flatpack	K16.A
5962F9956002VXC	HS9-4424BRH-Q	-55 to +125	16 Ld Flatpack	K16.A
N/A	HS9-4424BRH/PROTO	-55 to +125	16 Ld Flatpack	K16.A
N/A	HS9-4424RH/PROTO	-55 to +125	16 Ld Flatpack	K16.A
5962F9956001QXC	HS9-4424RH-8	-55 to +125	16 Ld Flatpack	K16.A

Notes:

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers must be used when ordering.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.

## 1.2 Pin Configuration

Flatpack CDFP4-F16  
Top View

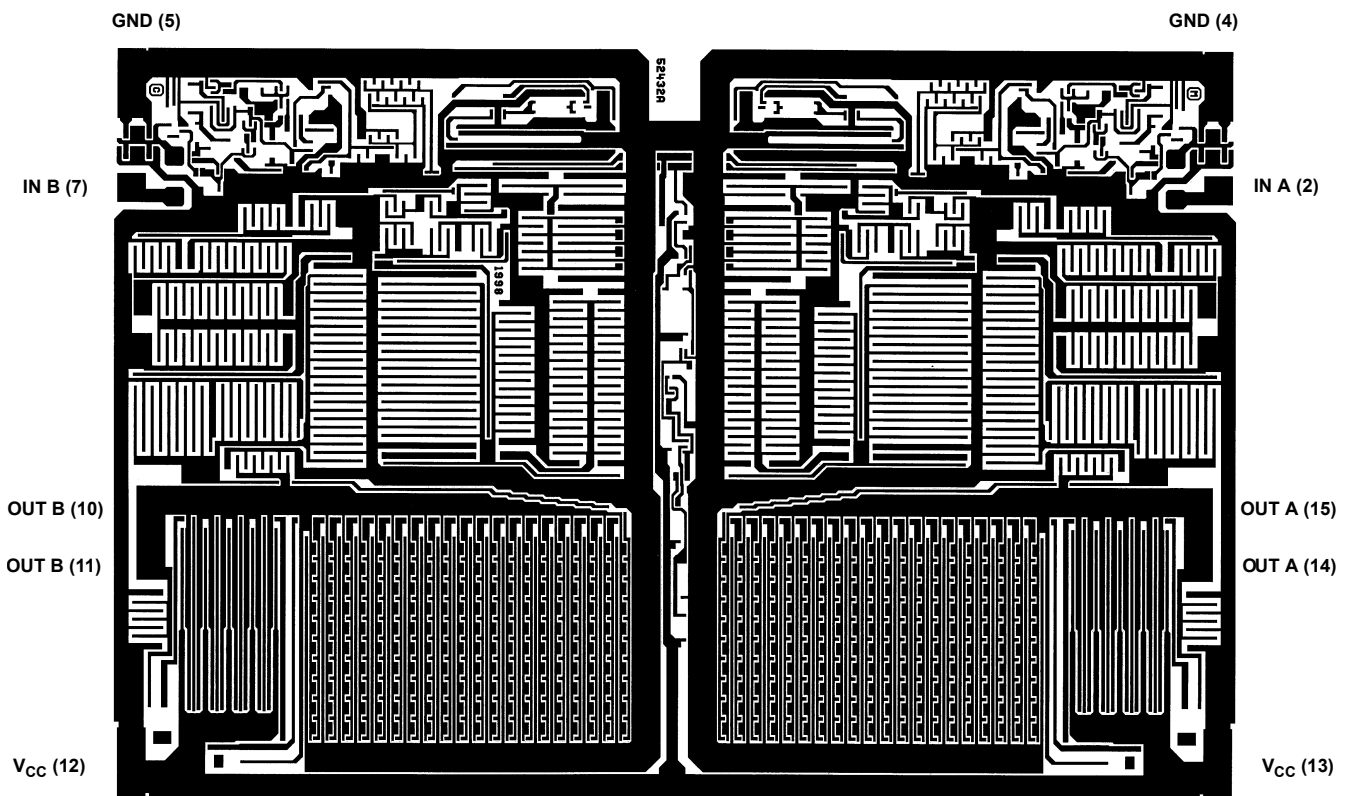


## 2. Die Characteristics

**Table 2. Die and Assembly Related Information**

Die Information	
Dimensions	4890µm x 3370µm (193 mils x 133 mils) Thickness: 483µm ±25.4µm (19 mils ±1 mil)
Interface Materials	
Glassivation	Type: PSG (Phosphorous Silicon Glass) Thickness: 8.0kÅ ±1.0kÅ
Top Metallization	Type: AlSiCu Thickness: 16.0kÅ ±2kÅ
Substrate	Radiation Hardened Silicon Gate, Dielectric Isolation
Backside Finish	Silicon
Assembly Information	
Substrate Potential	Unbiased (DI)
Additional Information	
Worst Case Current Density	<2.0 x 10 <sup>5</sup> A/cm <sup>2</sup>
Transistor Count	125

### 2.1 Metallization Mask Layout



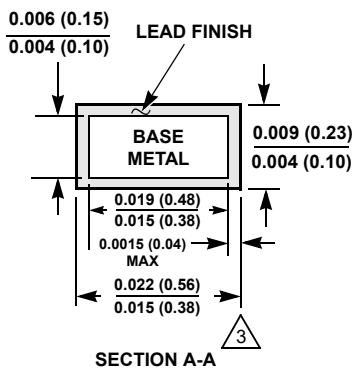
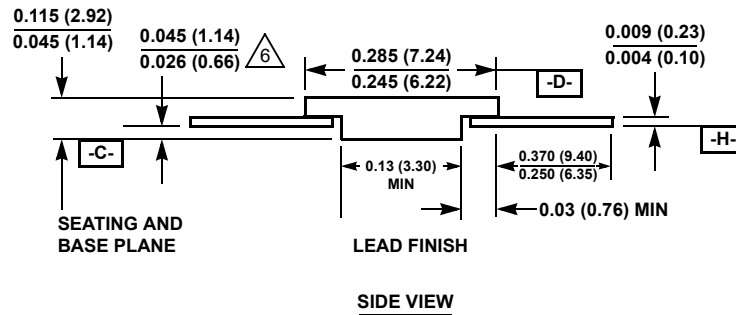
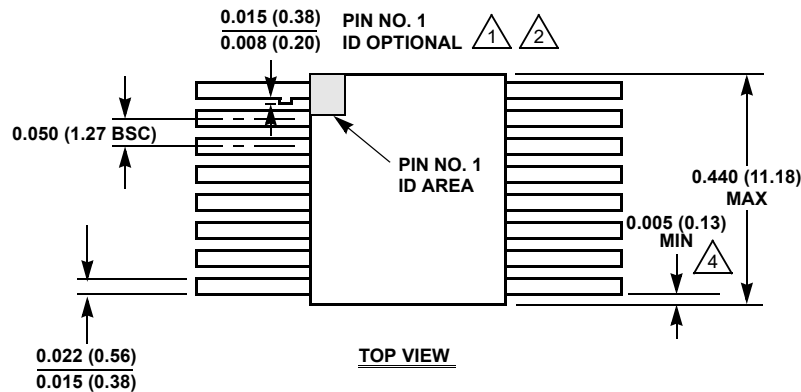
### 3. Revision History

Rev.	Date	Description
3.00	Jun.11.19	Applied new formatting. Added Related Literature. Added Table 1. Removed 3rd bullet Updated third sub-bullet under radiation environment feature bullet. Removed Note from pin configuration. Added Note 3. Added package outline drawing. Added Revision History Updated disclaimer.

### 4. Package Outline Drawing

For the most recent package outline drawing, see [K16.A](#).

K16.A  
 16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE  
 Rev 2, 1/10



**NOTES:**

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

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