HS2950P
29V 5A Load Protection HotSwitch® with Adjustable OVP, OCP and SS

PROTECTION PRODUCTS

Description

The HS2950P is a high side HotSwitch® for a variety of load conditions in industrial, telecom and consumer applications. It features a wide input voltage range of 2.7V to 29V and is capable of providing up to 5A output current.

The HS2950P utilizes flexible and programmable protection features and is able to handle multiple fault conditions. Programmable features include adjustable over current protection, precise over voltage protection, under voltage lockout, and soft start to protect against inrush currents for a range of load requirements.

An adjustable turn on delay feature allows the user to sequence multiple rails and efficiently limit start up current. The automatic output discharge protects the load during fault conditions, and the HS2950P will automatically restart from fault conditions as long as over and under voltage conditions have been removed for safe operation.

The HS2950P is offered in a small 3.0 x 3.0 x 0.55mm DFN 12 Lead package enabling very small board area implementations.

Features

- Integrated Load Switch
- Input Voltage Range – 2.7V to 29V
- Up to 5A Output Current
- Low R_{on} – 25mΩ
- Adjustable Current Limit
- Adjustable Over Voltage Protection
- Automatic Output Discharge
- Adjustable Soft Start
- Automatic Restart from All Faults Except OVP & UVLO
- Fault Flag Output

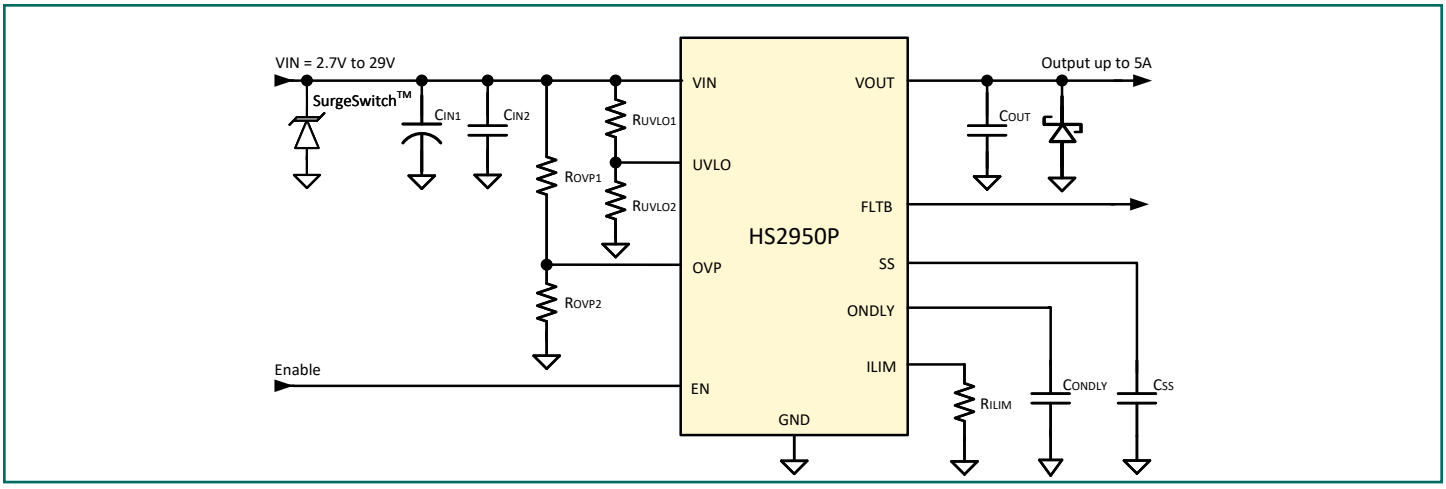
Mechanical Characteristics

- DFN 3.0 x 3.0 x 0.55mm 12 Lead package
- Pb-Free, Halogen Free, RoHS/WEEE compliant
- Pb Free Lead Finish
- Marking: Marking code
- Packaging: Tape and Reel

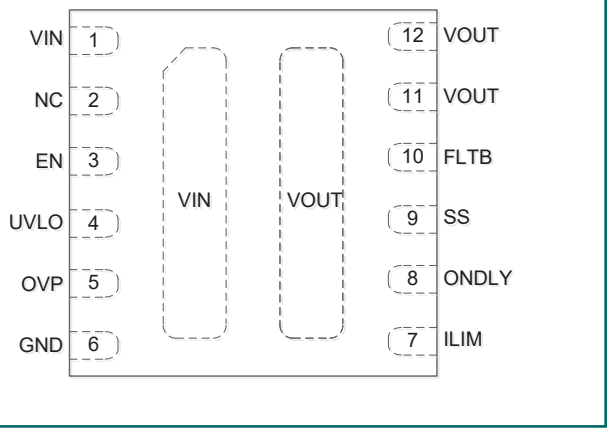
Applications

- Telecommunication, Networking Equipment
- Office Automation Equipment
- Industrial Equipment
- White Goods
- Consumer Products

Schematic



Pin Configuration



Pin Descriptions

Pin	Pin Name	Pin Function
1	VIN	Input voltage.
2	NC	No Connect Pin.
3	EN	Enable input, logic high turn on power switch.
4	UVLO	Externally programmable under voltage lockout threshold. Connect UVLO to an external resistor-divider to define a threshold externally. When UVLO pin is grounded, a default position is set internally.
5	OVP	Externally programmable over voltage lockout protection. Connect OVP to an external resistor-divider to define a threshold externally. When OVP pin is grounded, a default position is set internally.
6	GND	Ground connection.
7	ILIM	External resistor is used to set current-limit threshold.
8	ONDLY	When ONDLY pin is OPEN as default, the delay time will be 585µs (typ). The delay time can be programmed by adding an external capacitor to this pin. There is a pull down of about 10kΩ to discharge the ONDLY cap.
9	SS	When SS pin is OPEN as default, the output rise time will be 37µs. The rise time can be programmed by adding an external capacitor to this pin. To avoid excess power issues at startup, the C_{SS} capacitor must be less than 3.3nF at 29V_{IN} and 5A output current.
10	FLTB	Active-low open-drain output, asserted during over current (OCP), over voltage (OVP), under voltage lockout (UVLO), soft start (SS), turn on delay (ONDLY) or over temperature condition. If VOUT is turned off by enable, OVP or UVLO then the timer will be reset. If there is an OCP, FLTB will be held low while the 0.5ms timer counts.
11	VOUT	Power switch output.
12	VOUT	Power switch output.
-	Thermal Pad	Both VIN and VOUT thermal pad for heat-sinking purposes.

Absolute Maximum Rating

Rating	Symbol	Value	Units
VIN, EN, FLTB to GND	V_{IN}, V_{EN}, V_{FLTB}	-0.3 to +36.0	V
SS to GND	V_{SS}	-0.3 to +36.0	V
OVP, ILIM, ONDLY to GND		-0.3 to +6.0	V
UVLO to GND	V_{UVLO}	-0.3 to (+6.0 or V_{VIN} + 0.3 whichever is lower)	V
VOUT to GND	V_{OUT}	-0.3 to (V_{VIN} + 0.3)	V
ESD Protection Level[1]		2	kV

Recommended Operating Conditions

Rating	Symbol	Value	Units
Input Voltage	V_{IN}	2.7 to 29	V
Enable Voltage	V_{EN}	0 to 29	V
Maximum Output Current	I_O	5	A
Operating Ambient Temperature	T_A	-40 to 85	°C

Thermal Information

Rating	Value	Units
Thermal Resistance, Junction to Ambient[2]	42	°C/W
Maximum Junction Temperature	+150	°C
Storage Temperature Range	-65 to +150	°C
Peak IR Reflow Temperature (10s to 30s)	+260	°C

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:

(1) Tested according to JEDEC standard JS-001-2012.

(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless noted otherwise, -40°C ≤ T_A ≤ +85°C, T_J ≤ 125°C. V_{IN} = 29V, C_{IN} = 10µF, C_{OUT} = 10µF, V_{EN} = V_{IN}.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Voltage Range	V_{IN}		2.7		29	V
Maximum Output Current	I_{MAX}		5			A
Ron	R_{ON}	V_{IN}>5.5V, T_J = 25°C		25		mΩ
		V_{IN}>5.5V, T_J = -40°C to 125°C			43	
		V_{IN}<5.5V, T_J = -40°C to 125°C			50	
Shutdown Current	I_{QOFF}	V_{IN}=29V, V_{EN}=0V , V_{OUT} = 0V		1	2.87	µA
Quiescent Current	I_{QON}	V_{IN}=29V, V_{EN}=5.5V , I_{OUT} = 0A		340		µA
EN Logic Input						
Enable Voltage High Level Threshold	V_{EN-IH}		2.0			V
Enable Voltage Low Level Threshold	V_{EN-UL}				0.8	V
Enable Input Current	I_{EN}	V_{IN}= V_{EN}=5V			1	µA
ONDLY Sourcing Current	I_{ONDLY}		1.75	2.5	3.25	µA
ONDLY Threshold Voltage	V_{ONDLY}		0.56	0.82	1.1	V
Turn On Delay Time (Default)	t_{ON_DFT}	EN rising edge to ONDLY peak, C_{ONDLY} = Open	255	585	800	µs
Turn On Delay Time (Programmable)	t_{ON}	C_{ONDLY} = 10nF		4		ms
		Depending on C_{ONDLY} (1)	0		500	ms
Output Rise Time (Default)	t_{RT_DFT}	C_{SS}=open, R_{ILIM}=20kΩ , C_{OUT}=10µF, I_{OUT} = 0A		37		µs
SS Sourcing Current	I_{SS}		60	100	140	µA
Turn Off Delay	t_{OFF}				16	µs
Output Fall Time	t_{FT}	V_{IN}=29V, C_{OUT}=10µF, R_{OUT} = 100Ω		2		ms
Output Pull-down Resistance	R_{PD}	V_{OUT}=29V, T_J = 25°C		1.5		kΩ
Current Limit						
Current Limit (Programmable)	I_{LIMIT}	R_S Adjustable	0.5		6.5	A
Over Current Limit Accuracy	I_{THA}	R_{ILIM} = 20kΩ, V_{OUT}=0V, onset of current limit	5	5.5	6	A
Over Current Response Time	t_{OCP}			7		µs
ILIM Pin						
ILIM Pin Voltage	V_{ILIM}		284	298	312	mV

Electrical Characteristics (continued)

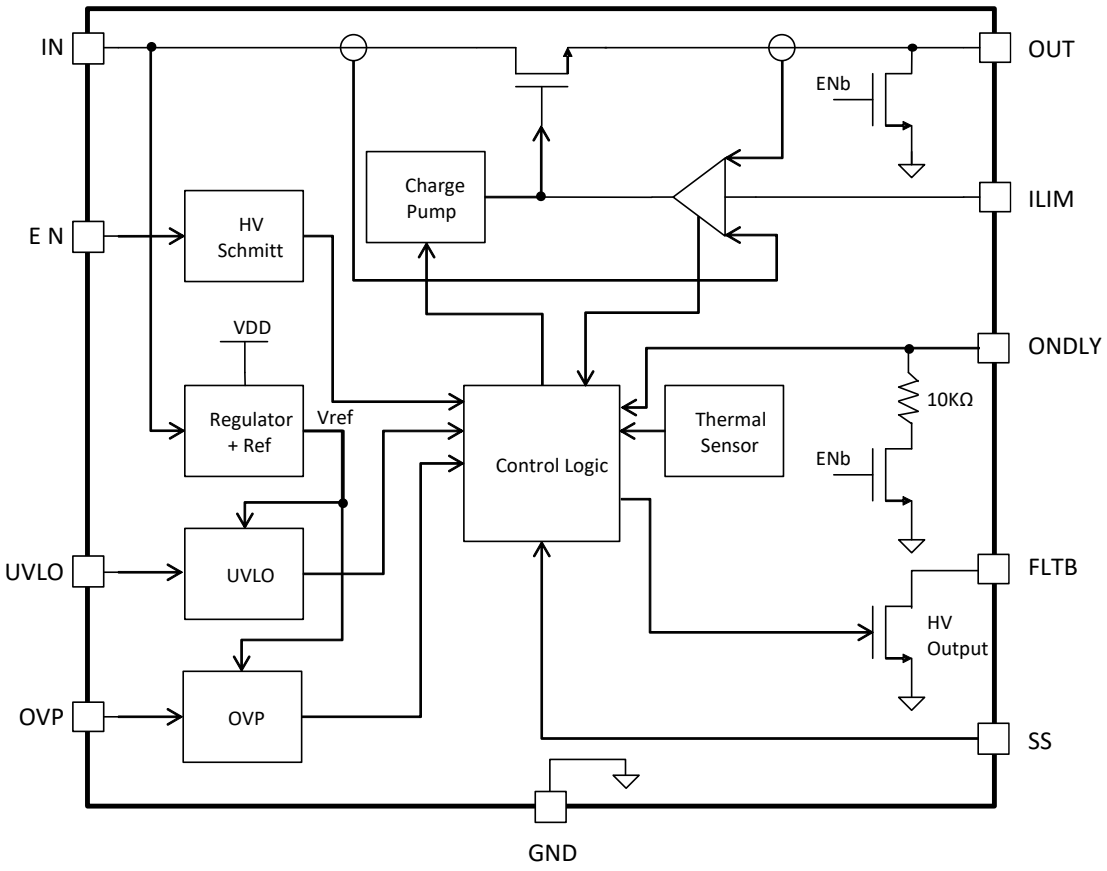
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
R_{ILIM} Out of Range High Limit	R_{ILIMH}		280			kΩ
R_{ILIM} Out of Range Low Limit	R_{ILIML}				10	kΩ
Recommended R_{ILIM} Range	$R_{ILIMRANGE}$		15.4		200	kΩ
Under Voltage Lock Out (UVLO)						
UVLO Voltage Threshold	V_{UVLO}	V_{IN} Rising	263	283	302	mV
UVLO Hysteresis	$V_{UVLO-TH}$	T_J = 25°C		13		mV
UVLO Leakage Current	I_{UVLO}		-100		100	nA
UVLO Voltage (Default)	V_{UVLO_DEF}	V_{IN} Rising	2.42	2.6	2.78	V
UVLO Hysteresis (Default)	$V_{UVLO\_DFT\_HYS}$			120		mV
Over Voltage Protection						
Over Voltage Protection Threshold	V_{OVP}	V_{IN} Rising	570	600	630	mV
OVP Hysteresis	V_{OVP_HYST}	T_J = 25°C		21		mV
OVP Leakage Current	I_{OVP}		-100		100	nA
OVP Voltage (Default)	V_{OVP_DFT}	V_{IN} Rising	3.60	3.80	4.00	V
OVP Hysteresis (Default)	$V_{OVP\_DFT\_HYST}$			140		mV
FLTB						
FLTB Pin Output Low Voltage	V_{FON}	I_{FLTB} = 1mA		180		mV
FLTB Pin Off State Leakage Current	I_{FOFF}	V_{FLTB} = 5.5V			1	µA
FLTB Pin Blanking Time	t_{FBLK}	OTP(1)		2		µs
		OVP, 100mV overdrive		19		µs
		UVLO, 100mV overdrive		8		µs
		OCP		0.5		ms
FLTB Pin De-assert Time	t_{FDA}	SS		0.5		ms
Thermal Shutdown Protection(1)						
Thermal Shutdown Threshold	T_{SP}			150		°C
Thermal Shutdown Threshold at ILIM	T_{SPILIM}			130		
Thermal Shutdown Hysteresis	T_{HYST}			30		
Thermal Shutdown Delay Time	T_{DELAY}			0.5		µs

(1) Test guaranteed by design

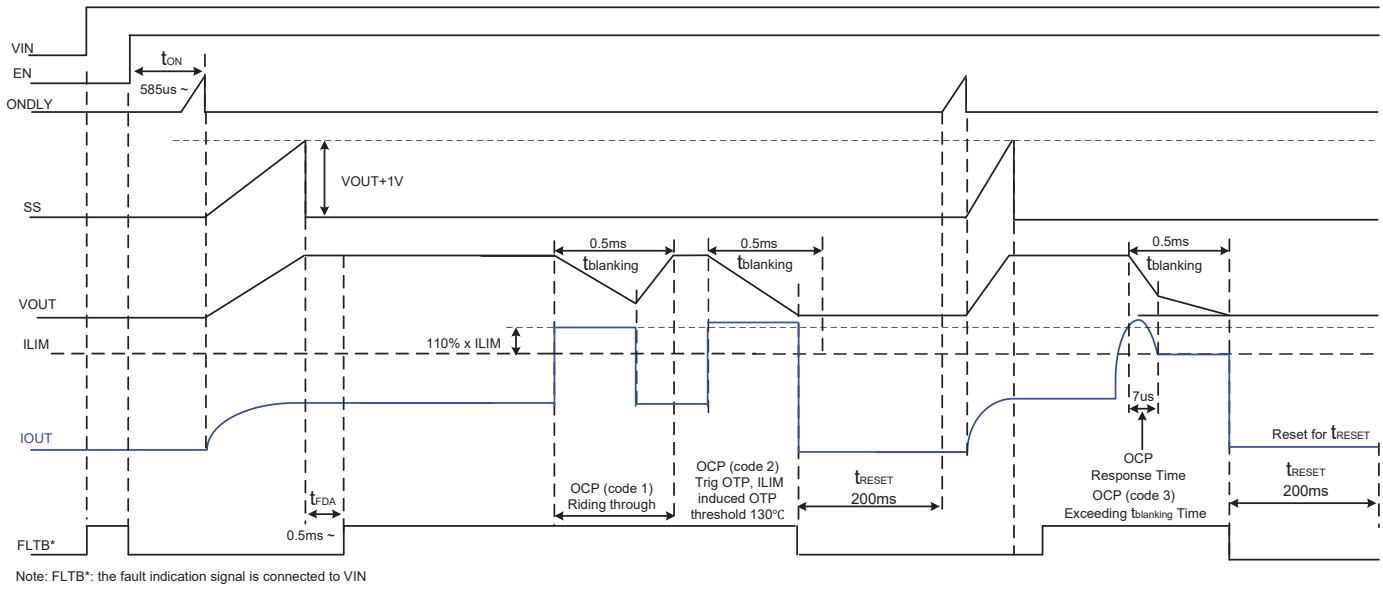
Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Timing Characteristics						
Reset Time	t_{RESET}	After OCP or OTP		200		ms

HS2950P Block Diagram



Typical Timing Diagram



Note: FLTB*: the fault indication signal is connected to VIN

Figure (1)

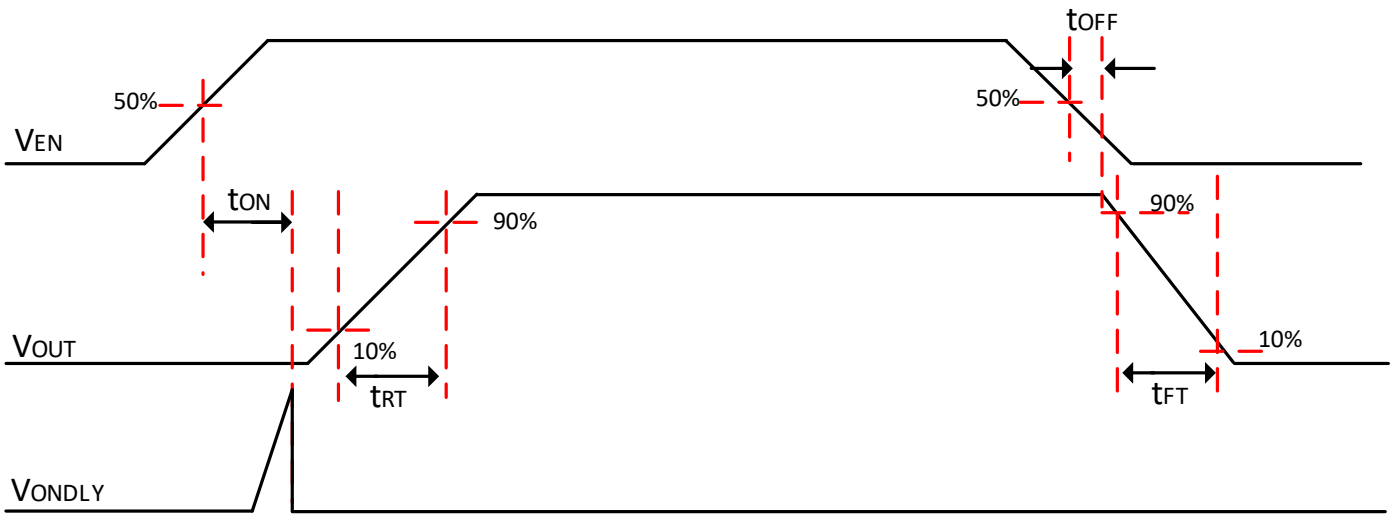
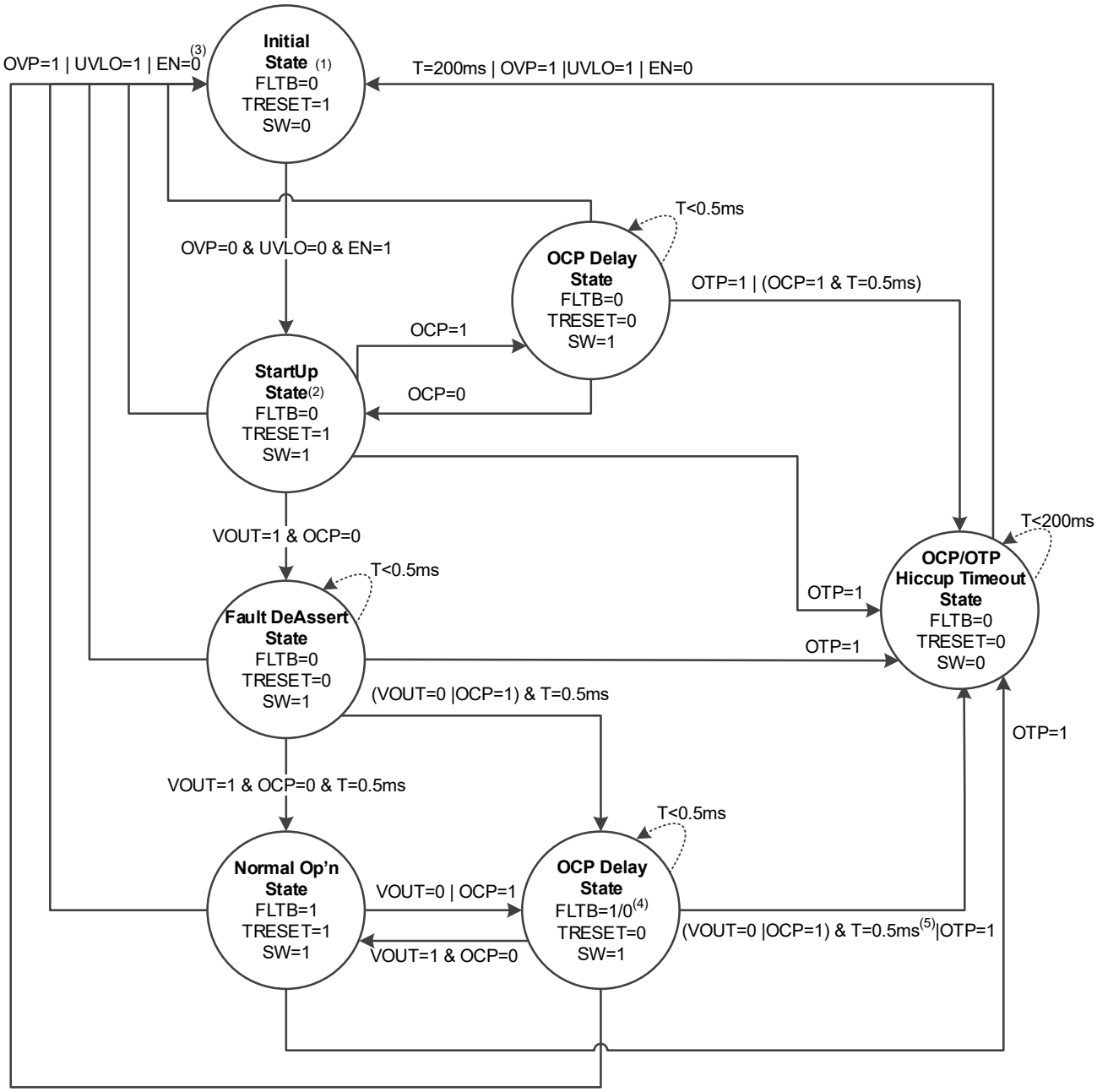


Figure (2)

State Diagram



FLTB = Fault indicative signal, 0.5ms De-assert time
TRESET = Internal timer reset signal
SW = Switch On/Off indicator
T = timer count

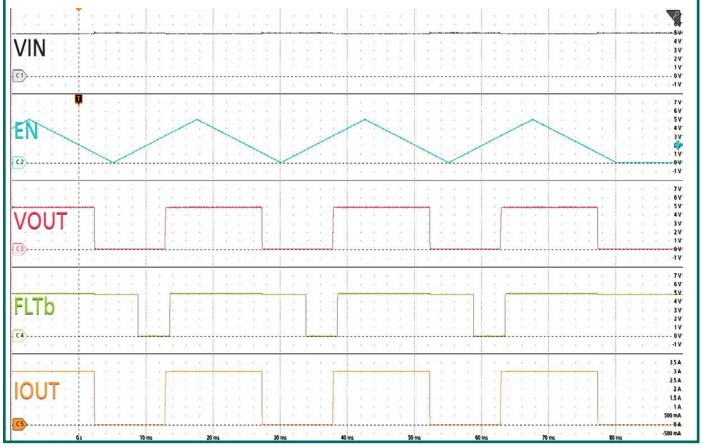
(1) ONDLY is just an input to the Initial State and ignored for the other states.
(2) SS requires = FLTB = 0. Before releasing FLTB, it must continue to stay low for another 0.5ms which is what Fault De-assert state does.
(3) Turn off the SW and report the fault immediately.
(4) FLTB keeps the same value as previous state.
(5) If previous state is Fault DeAssert, there is no extra 0.5ms blanking time for OCP Delay State to enter Hiccup Timeout State.

Typical Characteristics

Startup by Enable

V_{IN} = 5V, I_{OUT} = 3A, R_{ILIM}=18kΩ, C_{IN} = C_{OUT}=10µF

Time Scale: 10ms/div, Voltage Scale: 1V/div, Current Scale: 500mA/div

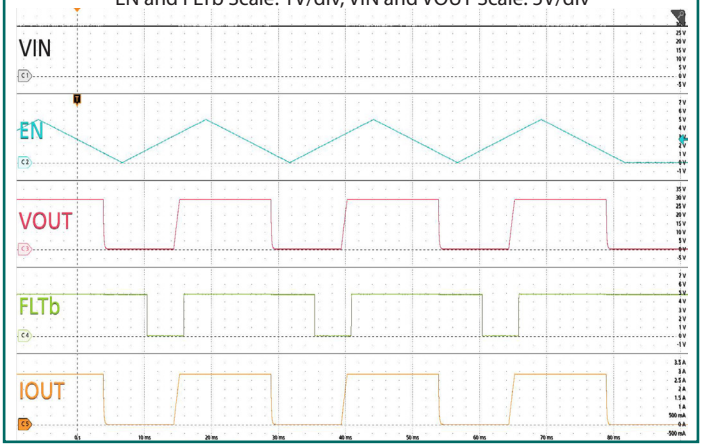


Startup by Enable

V_{IN} = 29V, I_{OUT} = 3A, R_{ILIM}=18kΩ, C_{IN} = C_{OUT}=10µF

Time Scale: 10ms/div, Current Scale: 500mA/div,

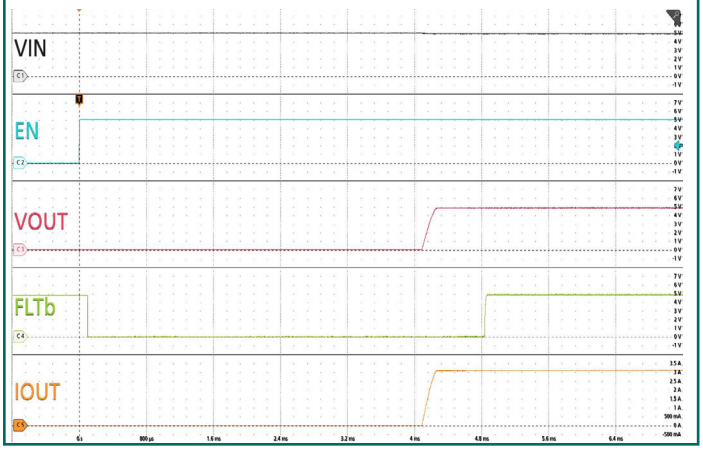
EN and FLTb Scale: 1V/div, VIN and VOUT Scale: 5V/div



Startup by Enable

V_{IN} = 5V, I_{OUT} = 3A, R_{ILIM}=18kΩ, C_{IN} = C_{OUT}=10µF

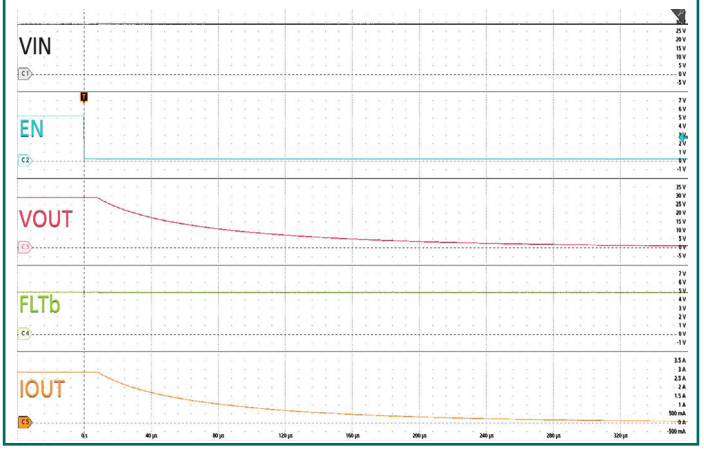
Time Scale: 800µs/div, Voltage Scale: 1V/div, Current Scale: 500mA/div



Shut Down by Enable

V_{IN} = 29V, I_{OUT} = 3A, R_{ILIM}=18kΩ, C_{IN} = C_{OUT}=10µF

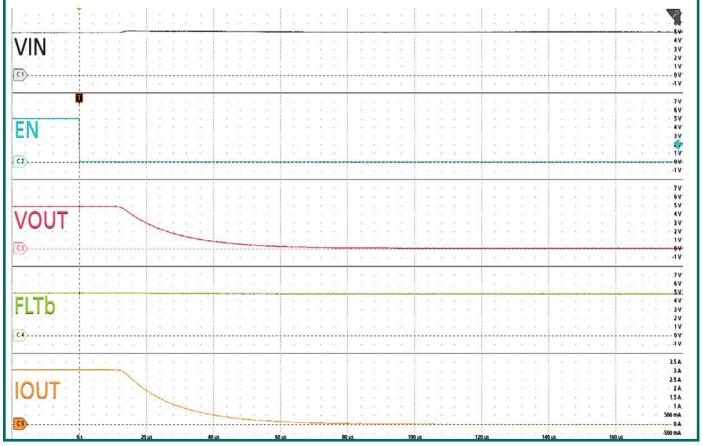
Time Scale: 40µs/div, Voltage Scale: 1V/div, Current Scale: 500mA/div



Shut Down by Enable

V_{IN} = 5V, I_{OUT} = 3A, R_{ILIM}=18kΩ, C_{IN} = C_{OUT}=10µF

Time Scale: 20µs/div, Voltage Scale: 1V/div, Current Scale: 500mA/div



Over Current Protection

V_{IN} = 29V, I_{OUT} = 7A, R_{ILIM}=18kΩ, C_{IN} = C_{OUT}=10µF

Time Scale: 100ms/div, Current Scale: 1A/div,

FLTb Scale: 1V/div, VIN and VOUT Scale: 5V/div

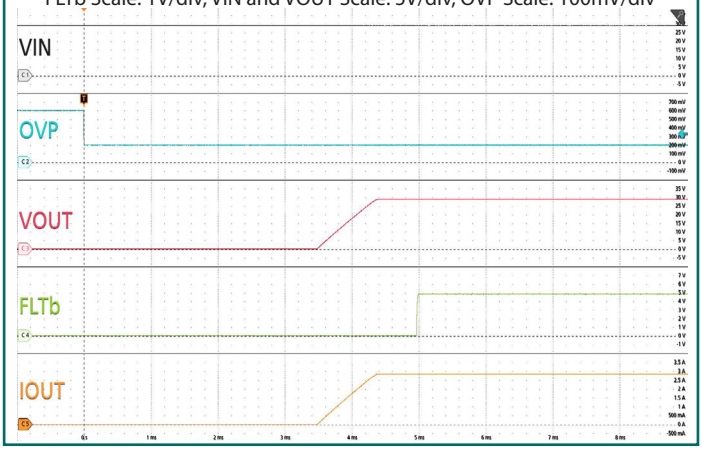
Typical Characteristics

Over Voltage Protection Mode On

V_{IN} = 29V, I_{OUT} = 3A, R_{ILIM}=18kΩ, C_{IN} = C_{OUT}=10µF
Time Scale: 40µs/div, Current Scale: 500mA/div,
FLTb Scale: 1V/div, VIN and VOUT Scale: 5V/div, OVP Scale: 100mV/div

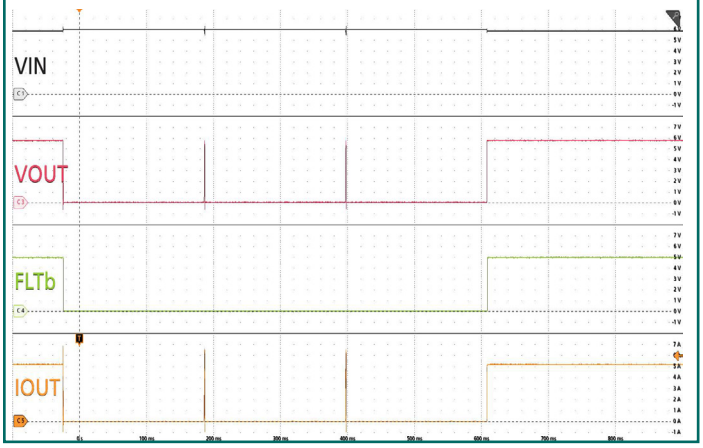
Over Voltage Protection Mode Off

V_{IN} = 29V, I_{OUT} = 3A, R_{ILIM}=18kΩ, C_{IN} = C_{OUT}=10µF
Time Scale: 1ms/div, Current Scale: 500mA/div,
FLTb Scale: 1V/div, VIN and VOUT Scale: 5V/div, OVP Scale: 100mV/div



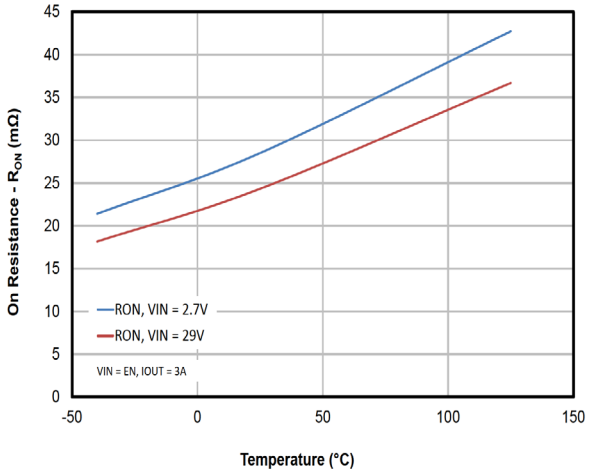
Over Current Protection

V_{IN} = 6V, I_{OUT} = 7A, R_{ILIM}=18kΩ, C_{IN} = C_{OUT}=10µF
Time Scale: 100ms/div, Voltage Scale: 1V/div, Current Scale: 1A/div



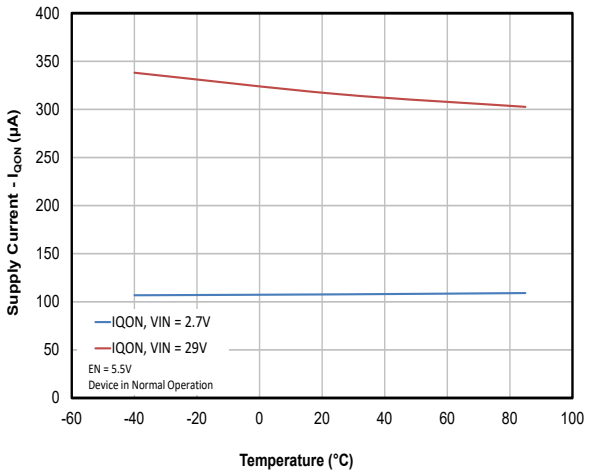
On Resistance vs. Temperature

V_{IN} = EN, C_{IN} = C_{OUT}=10µF



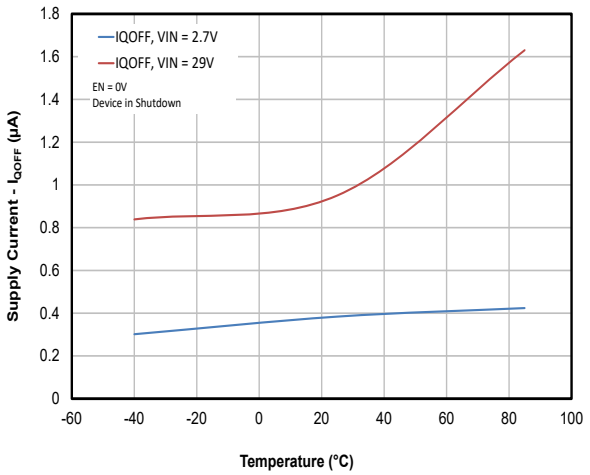
Quiescent Current On vs. Temperature

EN = 5.5V, C_{IN} = C_{OUT}=10µF, Normal Operation



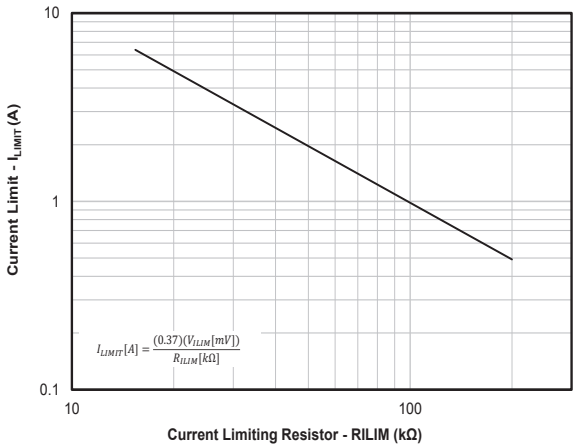
Shutdown Current Off vs. Temperature

EN = 0V, C_{IN} = C_{OUT}=10µF, Device in Shutdown



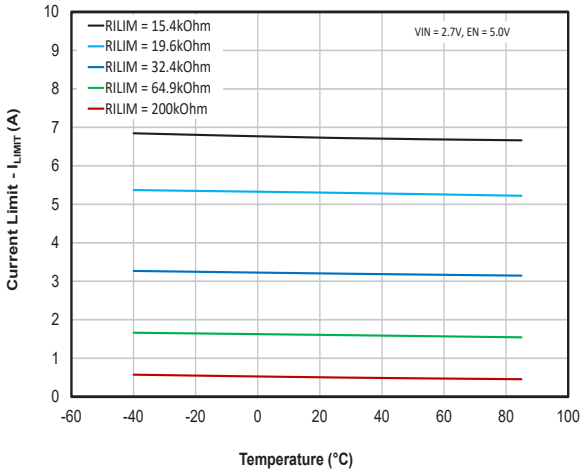
Typical Characteristics

Typcal I_{LIMIT} vs R_{LIMIT}



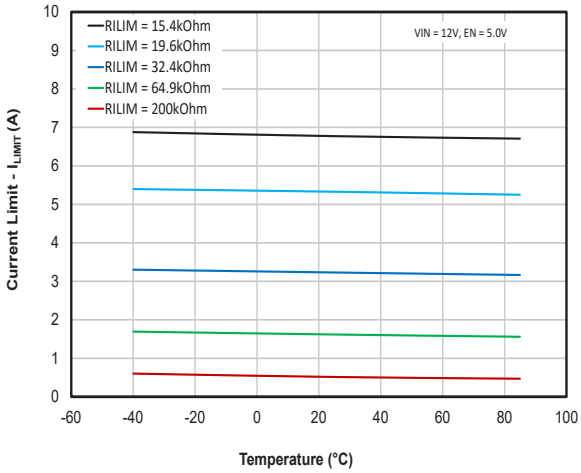
I_{LIMIT} vs. Temperature

V_{IN} = 2.7V, EN = 5V, C_{IN} = C_{OUT}=10µF



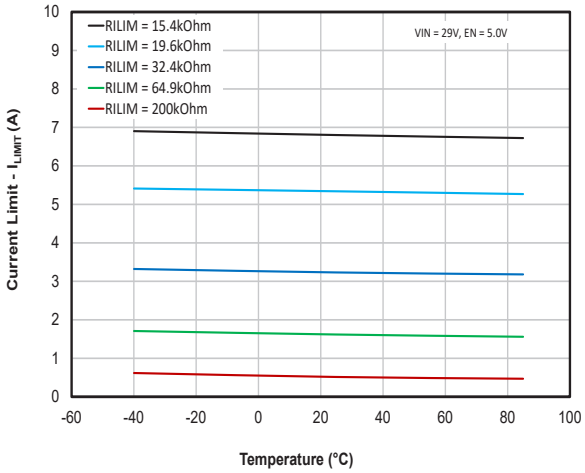
I_{LIMIT} vs. Temperature

V_{IN} = 12V, EN = 5V, C_{IN} = C_{OUT}=10µF



I_{LIMIT} vs. Temperature

V_{IN} = 29V, EN = 5V, C_{IN} = C_{OUT}=10µF



Application Information

Overview

HS2950P is a high-side load switch with a wide input voltage range of 2.7V to 29V supporting up to 5A DC load current. The device features low Rdson (25mΩ, typical) and a variety of adjustable protection features.

HS2950P offers functions with both default and adjustable options for Over Voltage Protection (OVP), Under Voltage Lockout (UVLO), Soft Start (SS), and Turn-On Delay (ONDLY). Thermal Shutdown (TSD) protection function is integrated, and the current limit (ILIM) pin resistor (RILIM) connection condition is constantly monitored. A fault flag output (FLTB) signal will be asserted low to report fault modes of load switch.

Typical Applications Circuit

Figure (4) below shows a typical circuit for a 12V application. The Over Voltage Protection Threshold is set to 12.9V. The Under Voltage Protection Threshold is set to 10.8V. The Turn On Delay is set to 4ms, and the Soft Start time is set to 0.32ms. The Over Current Protection is set to trigger at 5.5A. An explantaion on how to set each of the parameters is given in the following pages.

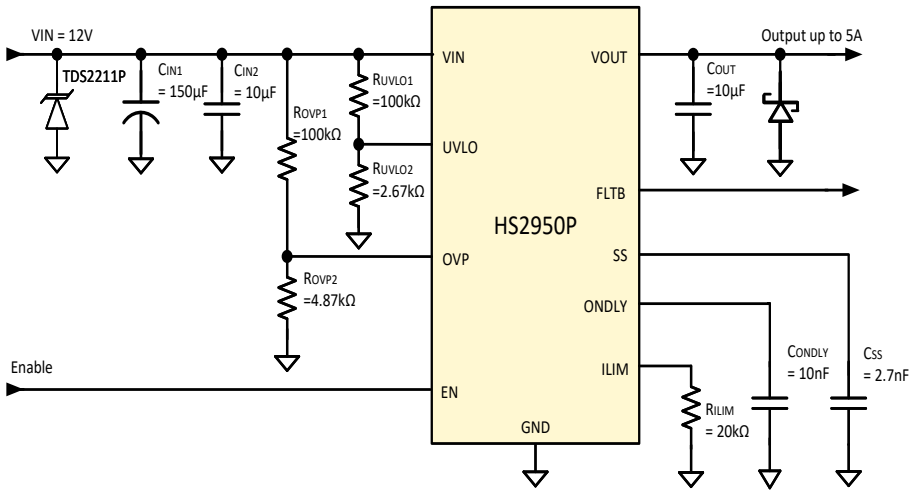


Figure (4) HS2950P Typical Applications Circuit

Application Information

Input Voltage SurgeSwitch™ Protection

A SurgeSwitch™ protection device is recommended on VIN. For applications above 22V a TDS3011P in parallel with a 10µF electrolytic capacitor and 1µ ceramic capacitor is recommended. For applications for up to 22V, a TDS2211P is resommended.

Enable and Turn On Delay

HS2950P features a high voltage enable (EN) pin. The part is enabled by pulling EN higher than 2V. When disabled, the auto-discharge function is turned on to discharge the VOUT pin to GND by 1.5KΩ internal resistance. The FLTB signal does not assert low until the device is enabled.

Once enabled, a default turn-on delay time is taken for the internal supply VDD to wake-up and the Finite State Machine (FSM) to scan all protection functions, including OVP, UVLO, TSD, and RILIM conditions.

A turn-on delay time default (t_{ON_DFT}) is 585µs typical. And the turn-on delay time can be adopted to extend the delay time by connecting an external capacitor, C_{ONDLY}, between ONDLY pin and GND. See Figure (5) for an illustration of the charging circuit.

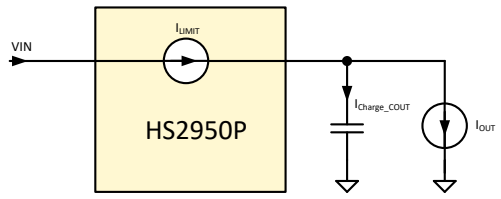


Figure (5) HS2950P Charging Circuit

Equation 1 determines which capacitor value to use when setting the desired turn-on delay time.

$$C_{ONDLY}[nF] = \frac{I_{ONDLY}[\mu A]t_{ON}[ms]}{V_{ONDLY}[V]} \quad (1)$$

When a fault condition occurs, the FSM will be reset to the initial state and t_{ON} will be executed. Once the fault condition is removed and the turn-on delay time is completed, the internal state machine starts the next phase, soft start, allowing for a controlled rise in output voltage.

Soft Start (SS)

HS2950P typically takes 37µs for the output voltage to rise from 0V to 29V if there is no capacitor connected between SS pin and GND. Adding a ceramic capacitor, C_{SS}, will lengthen the soft start time, t_{SS}, as estimated by Equation 2, where I_{SS} is the soft start capacitor charging current, typically 100µA.

$$t_{SS} = \frac{C_{SS}[nF]VIN[V]}{I_{SS}[\mu A]} \quad (2)$$

The maximum soft start capacitance is 3.3nF, to protect the device from thermal damage due to high power dissipation during soft start.

Once V_{OUT} reaches the same level as V_{IN}, the soft start phase ends. After 0.5ms (t_{FDA}) the fault flag signal deasserts and FLTB switches from low to high, indicating that the device is ready for normal operation.

Over Voltage Protection (OVP) and Under Voltage Lockout (UVLO)

HS2950P turns off the switch and prevents start-up if the input voltage rises above the OVP threshold or falls below the UVLO threshold.

When the OVP pin and UVLO pin are connected to GND (pin voltage ≤ 30mV typical), the default thresholds for OVP (3.8V typical) and UVLO (2.6V typical) are set internally.

Application Information, cont.

The programmable threshold option is set for both the OVP and UVLO pins by using external resistors. Equations 3 and 4 are used to set the desired thresholds, where, VIN_{OVP} is the OVP threshold for rising input voltage, V_{OVP} is the over voltage protection threshold at the OVP pin, typically 600mV, VIN_{UVLO} is the UVLO threshold for rising input voltage, and V_{UVLO} is under voltage protection threshold at the UVLO pin, typically 283mV.

$$VIN_{OVP}[V] = V_{OVP}\frac{R_{OVP1} + R_{OVP2}}{R_{OVP2}} \quad (3)$$

$$VIN_{UVLO}[V] = V_{UVLO}\frac{R_{UVLO1} + R_{UVLO2}}{R_{UVLO2}} \quad (4)$$

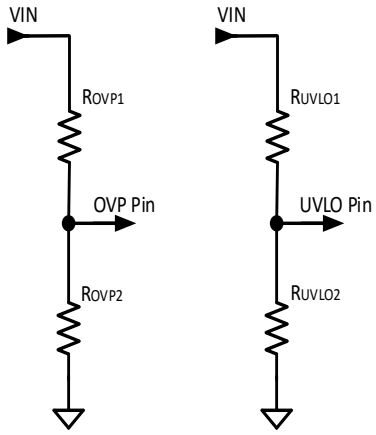


Figure (6) OVP and UVLO Programming Circuit

Over Current Protection (OCP)

HS2950P has over current protection (OCP) during soft start and normal operation. In the event of an over current condition, HS2950P limits the load current to the limit set by an external resistor, RILIM, tied from ILIM pin to GND. A resistor with 0.1% tolerance is recommended to ensure accuracy of the current limit set by the resistor. The OCP threshold ranges from 0.5A to 6.5A set by R_{ILIM}, determined by Equation 5 below.

$$I_{ILIM}[A] = \frac{(0.37)V_{ILIM}[mV]}{R_{ILIM}[k\Omega]} \quad (5)$$

Where,
I_{LIMIT} is the typical current limit value desired to be set
V_{ILIM} is the ILIM pin voltage, typically 298mV.

During OCP event, the FLTB signals a fault condition. There are two scenarios for the FLTB to signal a fault under OCP.

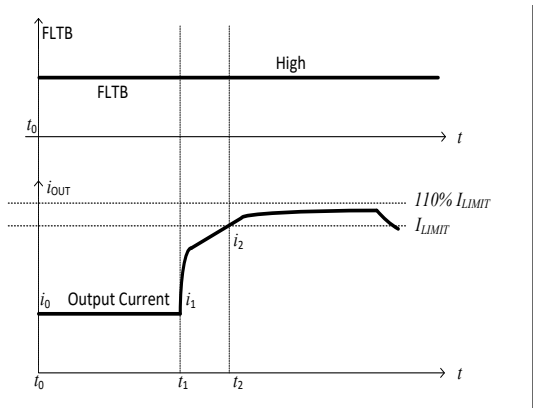


Figure (7) OCP Event with Less Over-Loaded Current

Figure (7) illustrates one of the scenarios in which the OCP event happens. At the time $t=t_2$, the output current i_{OUT} exceeds the OCP limit threshold i_2 programmed by the R_{ILIM}, but i_{OUT} is less than 110% of i_2. The FLTB signal remains high within the next 500µs and after if the output current stays higher than the OCP threshold i_2 and lower than 110% of i_2.

Another OCP scenario is shown in Figure (8) below. At time $t=t_2$, the output current i_{OUT} exceeds the OCP limit threshold i_2 programmed by the R_{ILIM}. The output current i_{OUT} continues ramping up exceeding 110% of i_2 at i_3. The FLTB signal trips 0.5ms later when the output current exceeds i_3 at $t=t_3$.

HS2950P has an over current response time (7µs typical) after the OCP event. The picture below illustrates how the ending load current varies according to different over current slew rates, S_{IOUT}, during the OCP event.

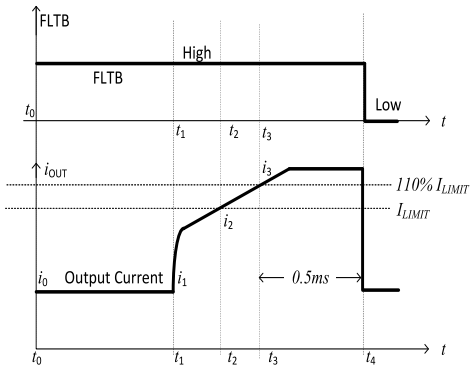


Figure (8) OCP Event with Heavy Load Current

Application Information, cont.

As shown in Figure (9) , at t_0 the output voltage and the output current are v_0 and i_0 , respectively. The output current starts to ramps up at t_1. At t_2, the output current exceeds the OCP threshold i_2. Due to the OCP response time, the output current continues to ramp up at the same slew rate, S_{IOUT}, as before, until the end of the 7µs.

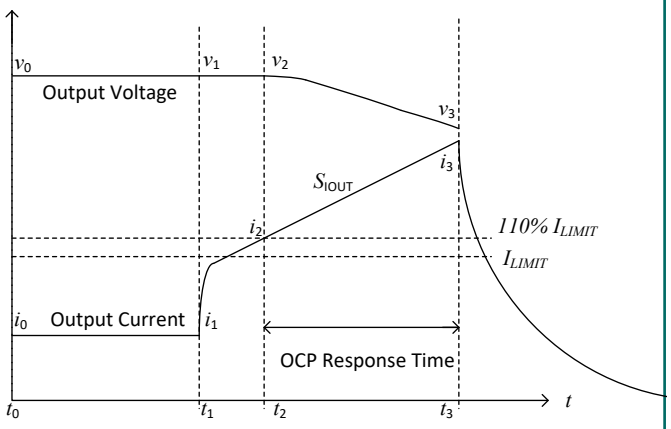


Figure (9) OCP with Different Over-Current Slew Rate

$$i_3 = i_2 + (7\mu s)(S_{IOUT}) \qquad (6)$$

The current i_3 can be estimated using Equation 6. The current i_2 is the 110% of the OCP threshold preset by the programmable resistor on the ILIM pin.

Short Circuit Protection

HS2950P has a short circuit protection function during soft start and normal operation, with a threshold setting 10% higher than the OCP level based on the RILIM resistor. If a short circuit event (Vout shorted to GND via a small impedance) occurs during soft start, the device is forced into Hiccup mode directly. If a short circuit event happens during normal operation, the device limits the current in the main switch within 7µs and shuts down. It will then enter Hiccup mode and restart after 200ms.

Thermal Shutdown Protection (TSP)

HS2950P features thermal shutdown protection to prevent part from over-heating. The device turns-off and asserts fault flag signal immediately when a junction temperature above 150°C is detected. Once TSP is triggered, the device enters Hiccup mode without any blanking time and stays there until junction temperatures cools down by 30°C.

The TSP threshold will be automatically adjusted to be 130°C, if device is operating under the current limit and the 30°C hysteresis remains the same.

Automatic Restart after Fault

HS2950P will be set to Hiccup state, where the switch is forced to shut-off, for the following conditions:

1. HS2950P over-heats and thermal shutdown threshold is reached.
2. Current limit protection is triggered and over-current condition persists beyond 0.5ms.
3. V_{OUT} drops to 1V below V_{IN} and such condition persists beyond 0.5ms (ignored by soft start phase).

The device stays in Hiccup for 200ms before it automatically tries to re-start. Re-start requires all fault condition to be removed and t_{ON} to be completed.

FLTB Signal

FLTB pin is an open drain output, and must be biased to an external voltage via a pull-up resistor. The fault flag signal is not asserted if device is disabled and the FLTB pin stays high. Once the device is enabled, the fault flag signal only releases after the part enters normal operation and FLTB pin is pulled high. During normal operation, six conditions trigger the fault flag signal to be asserted, and FLTB pin is pulled low accordingly:

1. OVP
2. UVLO
3. VILIM short or open(R_{ILIM} out of range)
4. OCP
5. Hiccup
6. OTP

Application Information

Input Capacitor Selection

In order to reduce the effects of voltage drop, noise, and bounce at the V_{IN} pin, a filter/decoupling capacitor between V_{IN} to GND is recommended. A 10µF and X7R ceramic capacitor is sufficient for most application conditions at 85°C ambient temperature. A 150µF or larger aluminum capacitor is recommended for a short-circuit test in order to minimize input voltage drop and to prevent device being damaged by inductance led voltage over-shoot on the input side

Output Capacitor Selection

A 10µF and X7R ceramic capacitor is sufficient for most application conditions at 85°C ambient. When a large output capacitor is used, a soft start capacitor and current limit resistor should be selected based on inrush current levels. This is to avoid a soft start OCP triggered Hiccup.

PCB Layout Consideration

An important objective of the layout is to minimize the PCB parasitic inductance. PCB parasitic inductance can affect several circuits' performance at turn-off, loading transients, and output short circuit application conditions. Figure (10) shows three current loops during the opening or closing of the load switch. Both positive peak voltage on the input terminal and negative peak voltage on the output terminal are related to the parasitic inductance of PCB and length of external connection lead to DC power supply or electronic loading. It is important to keep positive peak voltage and negative voltage less than the absolute maximum rating of the HS2950P. An input capacitor (C_{IN}) and an output capacitor (C_{OUT}) both need to be placed as close to the HS2950P as possible. Similarly the capacitors C_{ONDLY} and C_{SS} as well as the resistors R_{ILIM}, R_{UVLO1}, R_{UVLO2}, R_{OVP1} and R_{OVP2} should be placed as close to the HS2950P possible. The ground points should be connected to the PCB ground with traces as short as possible. A schematic illustrating the parasitic inductances in the layout is shown in Figure (10). The corresponding layout is shown in Figure (11).

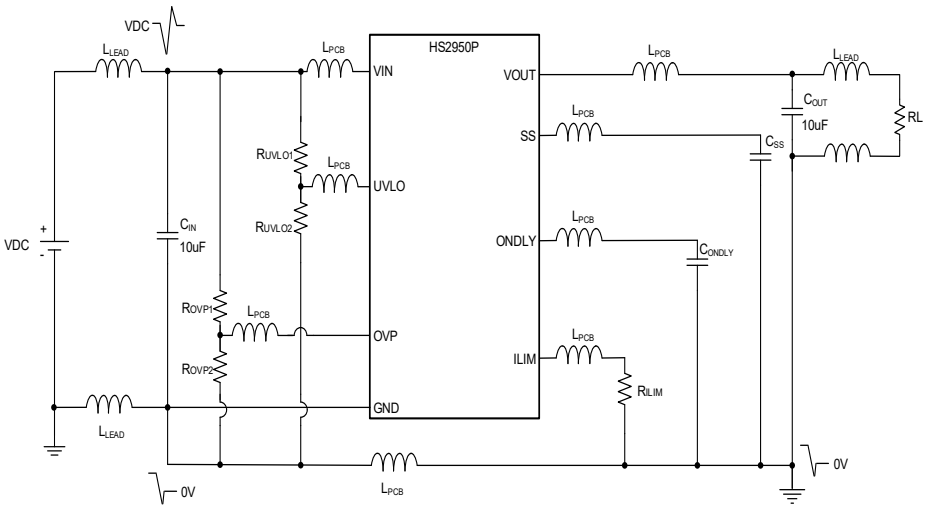


Figure (10) Layout Schematic

Application Information

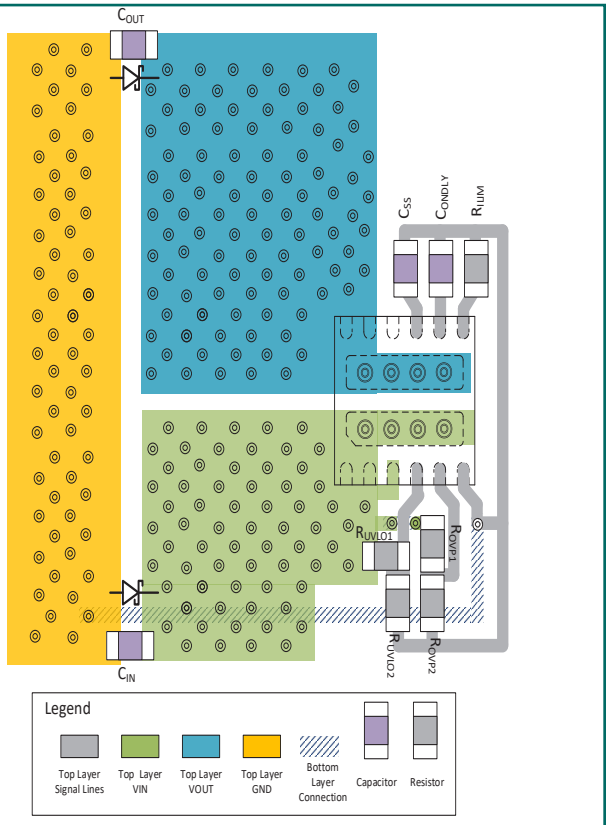


Figure (11) Layout Illustration

A negative voltage may occur on the output terminal during a short-circuit event. Negative voltage level is a product of short-circuit impedance, parasitic inductance, capacitance on the output terminal. A Schottky diode can be added to output terminal in order to minimize negative voltage. The Schottky diode should be placed close to the output capacitor with a short trace to reduce inductance.

A fast transient event, e.g. surge or ESD, may occur on the input terminal. A Transient Diverting Suppressor (TDS) should be used on the VIN line to protect the device. The TDS should be placed close to the input capacitors with short traces.

Power paths should be kept as short as possible and appropriately sized to withstand a minimum of double the maximum load current. The thermal pads for VIN and VOUT should be connected to as much copper area as possible on the top and bottom PCB layers. Thermal vias should be used for heat dissipation and to distribute current evenly. The GND at Pin 6 should be tied to the PCB ground plane by the shortest path possible.

Thermal Analysis

The maximum junction temperature of the load switch must be less than thermal shutdown threshold (150°C typical) during normal operation condition. Equation 7 describes how to calculate junction temperature (T_{J_MAX}) at 5A output loading current , 85°C ambient temperature and V_{IN} less than 5.5V.

A 0.5ms OCP blanking time and a 200ms reset time are integrated in HS2950P. Even if HS2950P operates under maximum input voltage (29V) condition with output

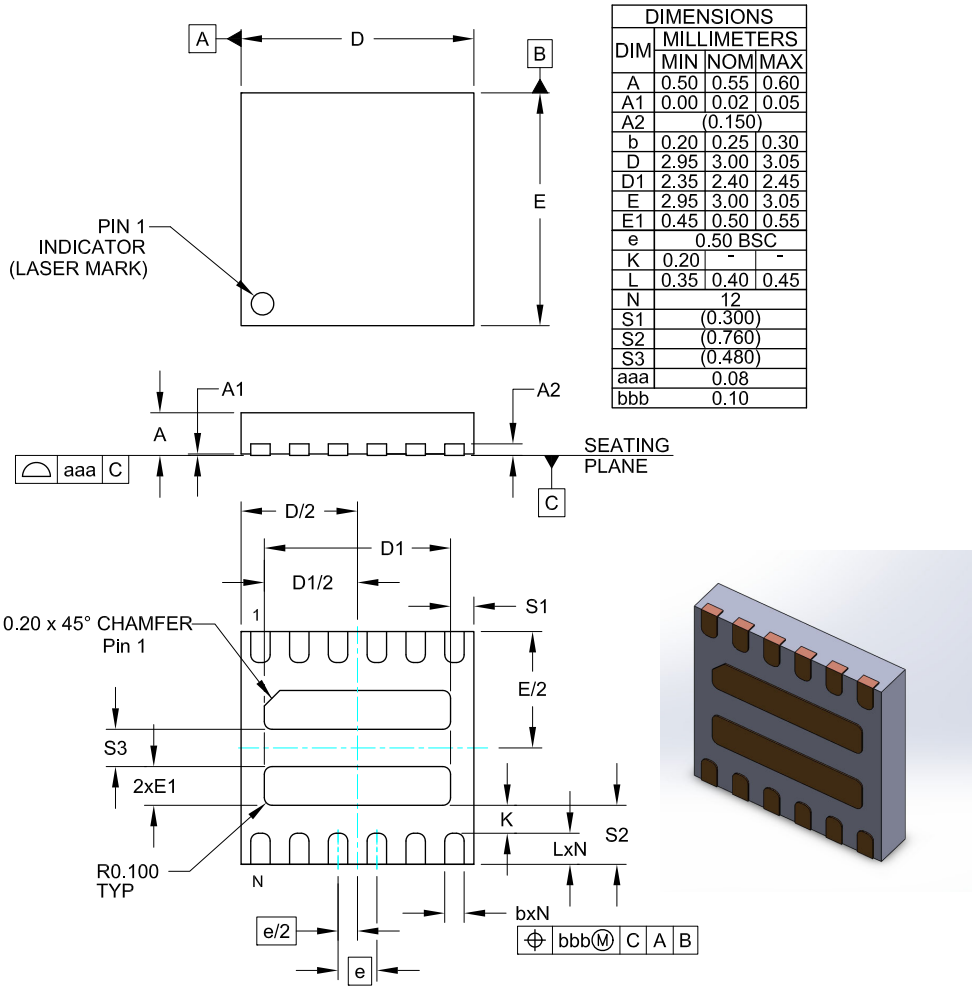
$$T_{J_{MAX}} = (I_{OUT})^2(R_{ON})(R_{\theta JA}) + T_A \quad (7)$$
$$= (5A)^2(50m\Omega)(42\,°C/W) + 85°C$$
$$= 137.5°C$$

$$P_{SC} = (VIN)(I_{LIMIT})\frac{t_{FBLK}}{t_{FBLK} + t_{RESET}} \quad (8)$$
$$= (29V)(6.5A)\frac{0.5ms}{0.5ms + 200ms}$$
$$= 0.47W$$

shorted to 0V, the max average power loss is less than 0.5W. Thermal shut-down protection will not be toggled up to 85°C ambient temperature. V_{IN}, V_{OUT} and GND pins of HS2950P dissipate the majority of the heat generated during high power loss application conditions. A proper layout reduces higher junction temperature and prevents device damage. Thermal performance is improved by connecting both V_{IN} and V_{OUT} thermal exposed pads to copper planes on both input and output terminal.

During a short circuit under normal operation, the HS2950P may become damaged if 0.5 Joule or higher power loss is dissipated on the device. To protect the HS2950P from damage in this condition, the soft-start capacitor should be less than 3.3nF to lower the average energy loss on the HS2950P to below 0.15 Joule.

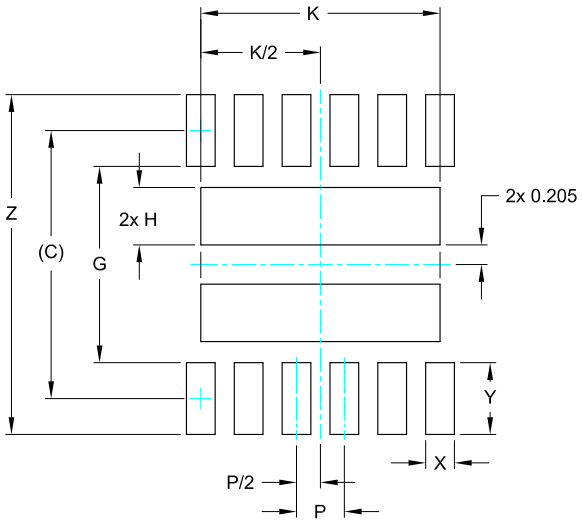
Outline Drawing - DFN 3.0mm x 3.0mm, 12 Lead



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A2		(0.150)	
b	0.20	0.25	0.30
D	2.95	3.00	3.05
D1	2.35	2.40	2.45
E	2.95	3.00	3.05
E1	0.45	0.50	0.55
e		0.50 BSC	
K	0.20	-	-
L	0.35	0.40	0.45
N		12	
S1		(0.300)	
S2		(0.760)	
S3		(0.480)	
aaa		0.08	
bbb		0.10	

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern - DFN 3.0mm x 3.0mm, 12 Lead

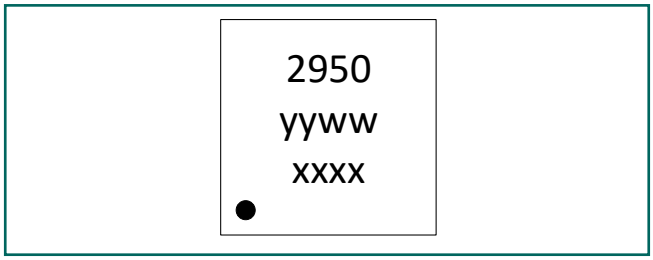


DIMENSIONS	
DIM	MILLIMETERS
C	(2.80)
G	2.05
H	0.60
K	2.50
P	0.50
X	0.30
Y	0.75
Z	3.55

NOTES:

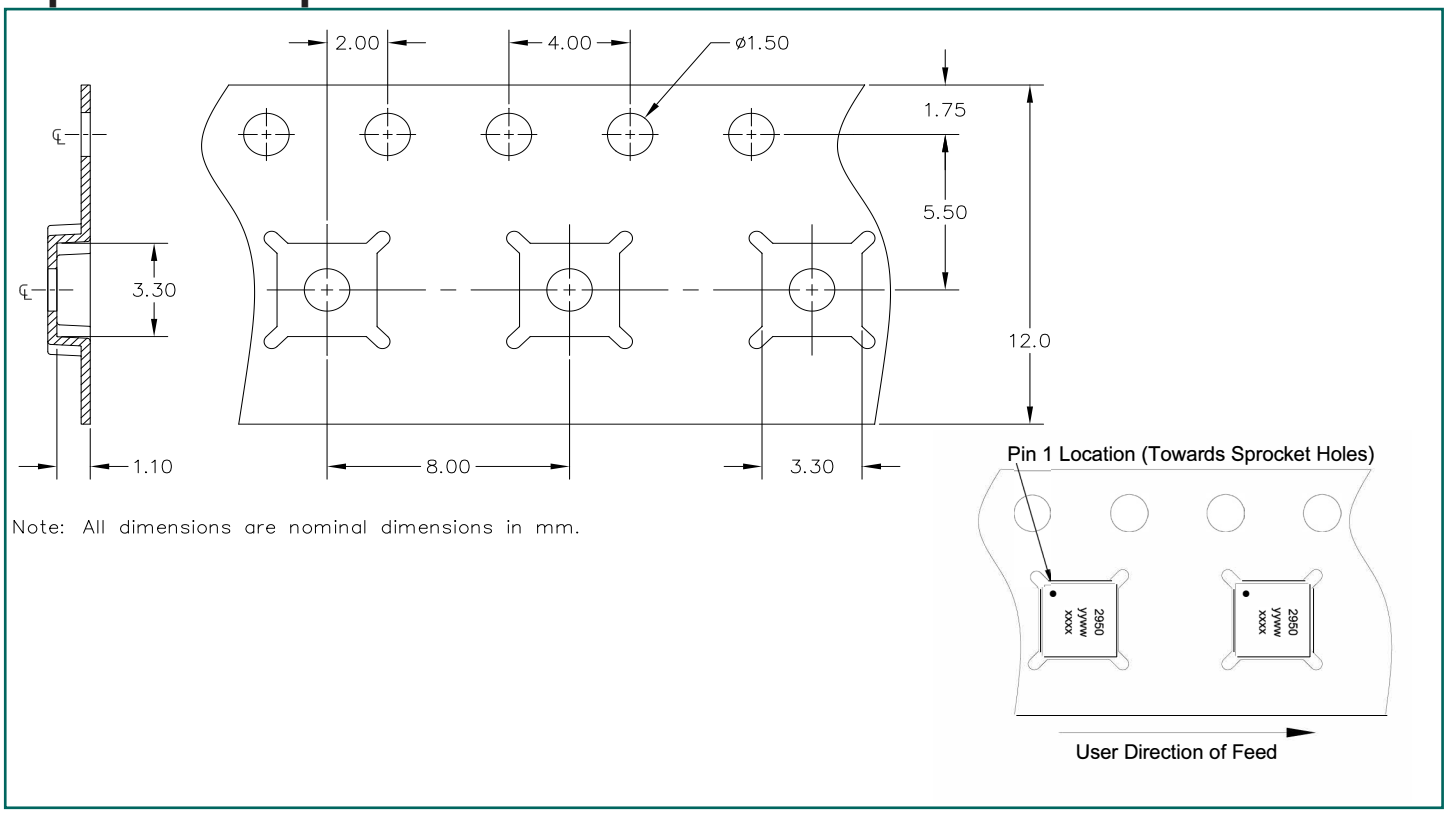
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code



Marking for the 3.0 mm x 3.0 mm
DFN 12 Lead Package :
yyww = Datecode (Example: 1652)
xxxx = Semtech Lot No. (Example: E901)

Tape and Reel Specification



Ordering Information

Part Number	Qty per Reel	Reel Size
HS2950P.M	5,000	13″
HS2950P-EVB		Evaluation Board
HotSwitch is a registered trademark of Semtech Corporation.		

Important Notice

Information relating to this product and the application or design described herein is believed to be reliable, however such information is provided as a guide only and Semtech assumes no liability for any errors in this document, or for the application or design described herein. Semtech reserves the right to make changes to the product or this document at any time without notice. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. Semtech warrants performance of its products to the specifications applicable at the time of sale, and all sales are made in accordance with Semtech's standard terms and conditions of sale.

SEMTECH PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS, OR IN NUCLEAR APPLICATIONS IN WHICH THE FAILURE COULD BE REASONABLY EXPECTED TO RESULT IN PERSONAL INJURY, LOSS OF LIFE OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. INCLUSION OF SEMTECH PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE UNDERTAKEN SOLELY AT THE CUSTOMER'S OWN RISK. Should a customer purchase or use Semtech products for any such unauthorized application, the customer shall indemnify and hold Semtech and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs damages and attorney fees which could arise.

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com