N channel 60V MOSFET

1. Description

The HS50N06DA is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as LCD inverter, computer power management and DC to DC converter circuits which need low in-line power loss.

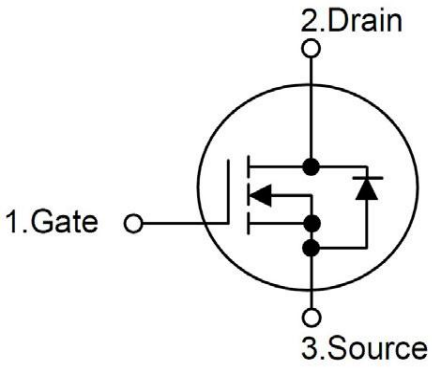
2. Feature

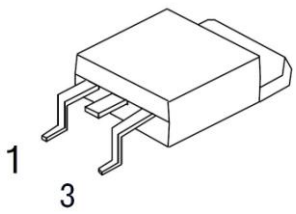
- $R_{DS(ON)} \leqq 22m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

V_{DS}	60	V
$R_{DS(on)}$	22	mΩ
I_D	50	A

3. Pin configuration

Order Number	Package
HS50N06DA	TO-252





TO-252

4. Absolute maximum ratings (Tc=25℃ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{DSS}	±20	V
Continuous Drain Current	Tc=25℃	I_D	50	A
	Tc=70℃		35.1	A
Pulsed Drain Current		I_{DM}	140	A
Power Dissipation	Tc=25℃	P_D	60	W
	Tc=70℃		38.5	
Operating Junction and Storage Temperature Range		T_J, Tstg	-55 to 175	℃

5. Thermal characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance, case to sink typ.	R_{thCS}	0.5	°C/W
Thermal resistance junction to case.	R_{thJC}	2.1	°C/W
Thermal resistance junction to ambient.	R_{thJA}	110	°C/W

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6. Electrical characteristics (T_A =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60	–	–	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=VGS, I_D=250μA	2	–	4	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V	–	–	±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V	–	–	1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=50A	–	17	22	mΩ
V_{SD}	Diode Forward Voltage	I_S=50A, V_{GS}=0V	–	1	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DD}=48V, V_{GS}=10V, I_D=50A	–	37	–	Nc
Qg	Total Gate Charge	V_{DD}=48V, V_{GS}=4.5V, I_D=50A	–	11	–	
Qgs	Gate-Source Charge		–	15	–	
Qgd	Gate-Drain Charge		–	8	–	
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz	–	2	–	Ω
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz	–	2270	–	pF
Coss	Output Capacitance		–	197	–	
Crss	Reverse Transfer Capacitance		–	62	–	
td(on)	Turn-On Delay Time	V_{GS} =10V, R_L=30Ω V_{DS}=30V, R_G=3.6Ω	–	29	–	ns
tr	Turn-On Rise Time		–	5	–	
td(off)	Turn-Off Delay Time		–	53	–	
tf	Turn-Off Fall Time		–	6	–	

Notes :a. pulse test:pulse width ≦300 us,duty cycle 2% ,Guaranteed by design,not subject to production testing.

b. HOMSEMI mos reserves the right to improve product design,functions and reliability without notice.

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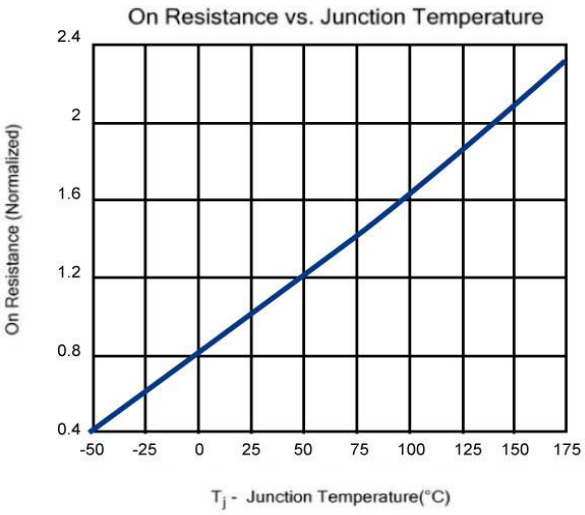

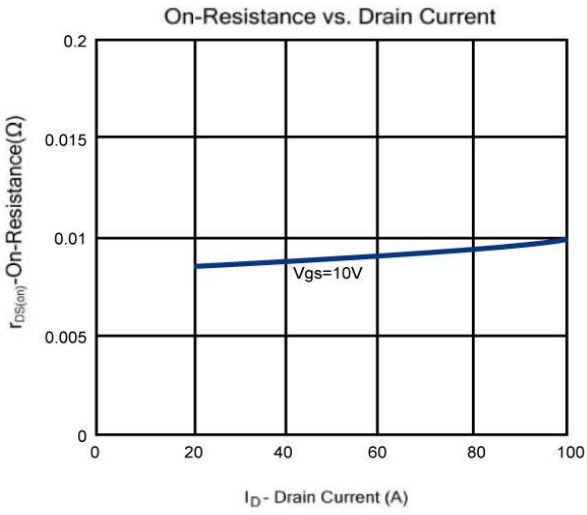

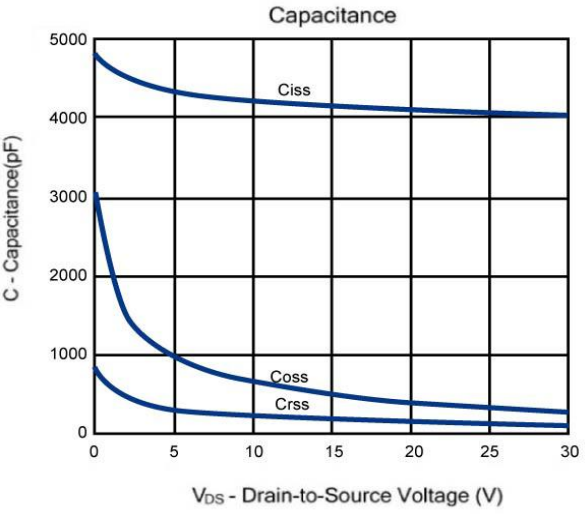

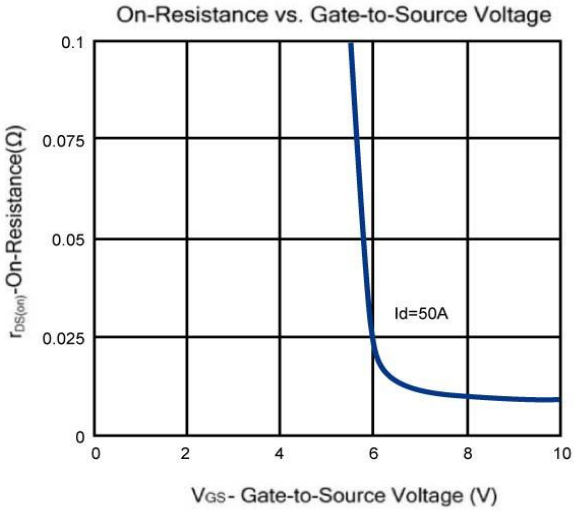

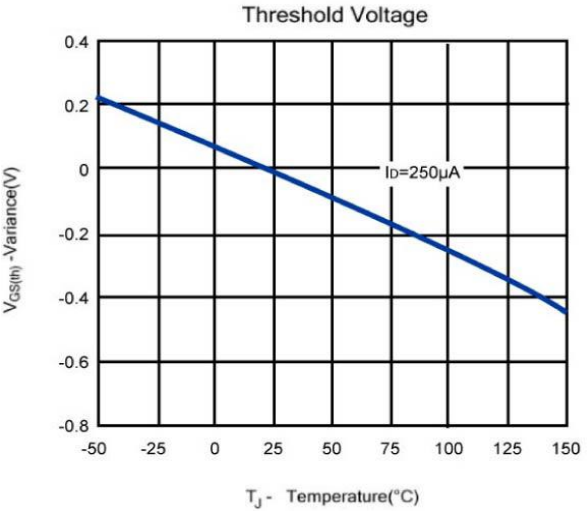

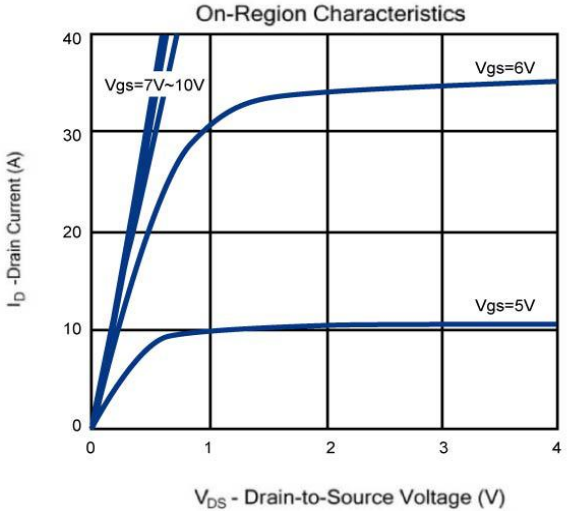

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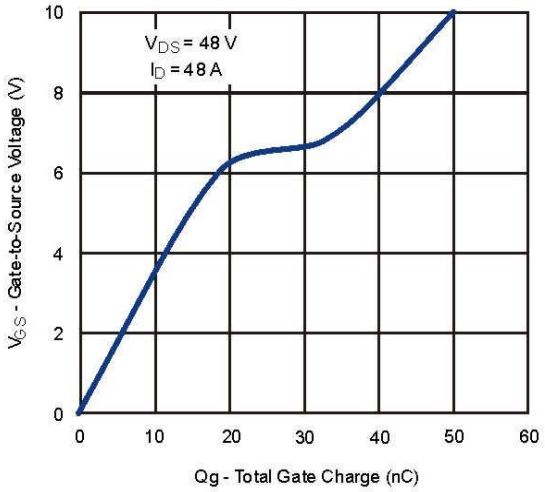
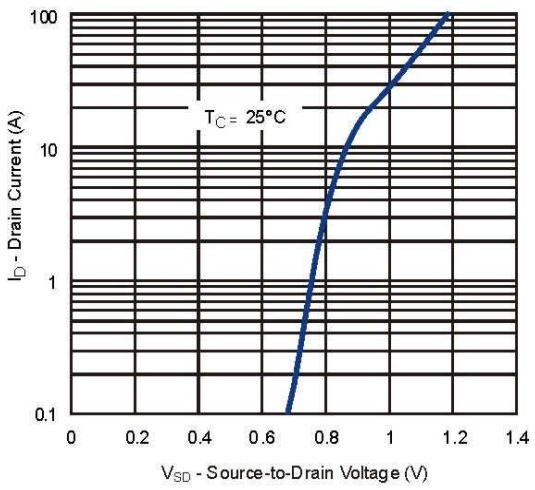
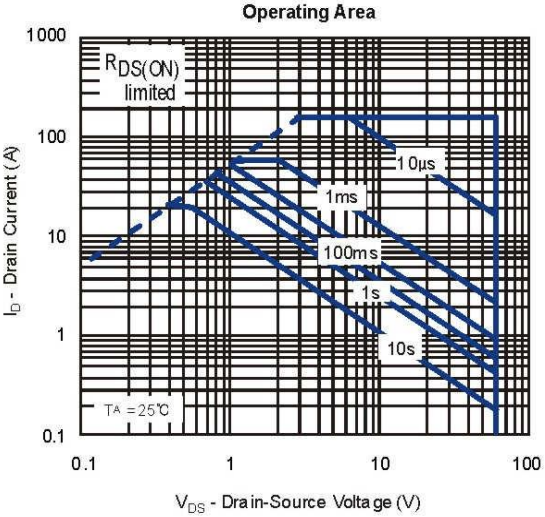
Gate Charge



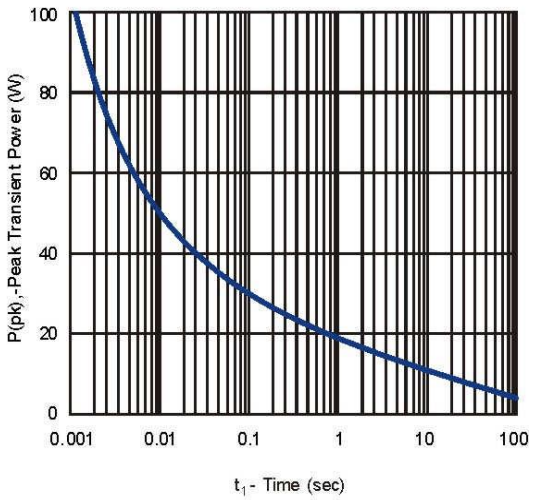
On-Resistance vs. Drain Current



Maximum Forward Biased Safe Operating Area



Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient