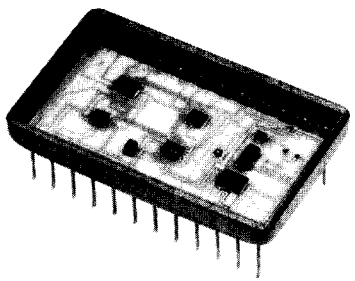
HS 5150

High Speed 8-Bit ADC with μP Interface

FEATURES

- **2.5μsec Conversion Time**
- **Three State Outputs**
- **Full MIL Operation**
  −55°C to +125°C
- **7 User-Selectable Input Ranges**
- **Adjustment Free −**
  No Gain or Offset Adjustments Necessary

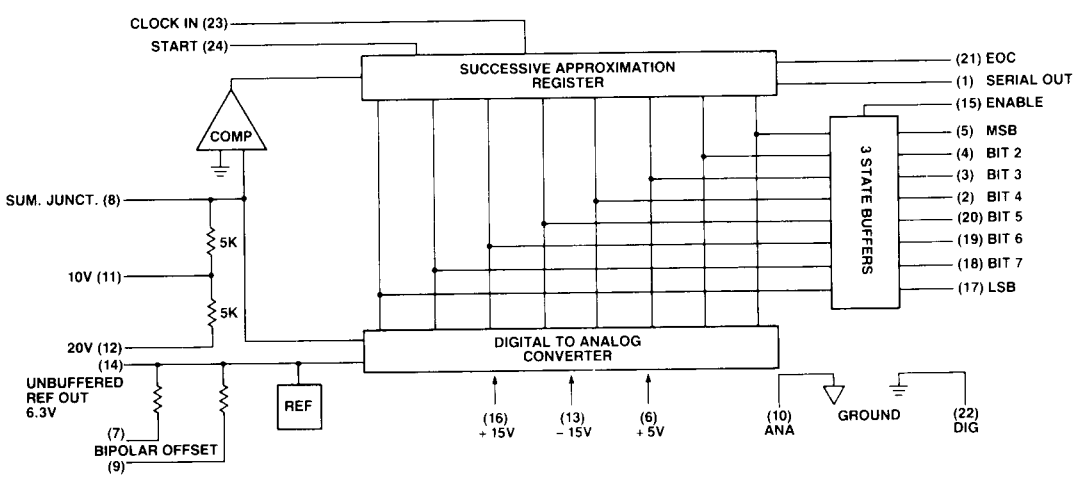


DESCRIPTION

The HS 5150 is a complete, 8-bit, successive approximation analog to digital converter with three-state output buffers for direct interface to microprocessor buses. The ADC converts in 2.5 μ sec (max), and features ± ½ LSB linearity with no missing codes guaranteed over an operating temperature of −55°C to +125°C. The HS 5150 incorporates highly stable thin-film resistor networks enabling adjustment free operation. No external gain or offset adjusting potentiometers are required for ±1 LSB absolute accuracy. The inputs can be pin programmed for 0 to +5V, 0 to +10V, ±2.5V, ±5V, ±10V, 0 to −5V, and 0 to −10V.

Three state output buffers enable interface to a variety of 8-bit microprocessors. In memory mapped applications, the ADC resembles a RAM location with 2.5 μ sec access time. The HS 5150 is available with MIL-STD-883 Rev. C, Levels B or S screening for military/aerospace applications.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C with ±15V and +5V, unless otherwise specified)

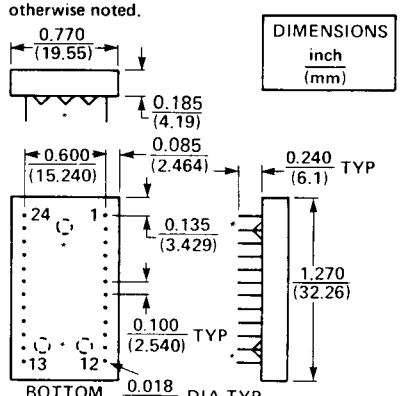
SERIES	HS 5150
TYPE	Successive Approximation
RESOLUTION	8-Bits
ANALOG INPUTS	
Input Voltage Range	7 Input Ranges
Input Impedance	2.5/5/10 KΩ
DIGITAL INPUTS	
Logic "0" (Except Enable)	0.8V max
Logic "1" (Except Enable)	2.0V min
Loading (Note 1)	1 TTL Load
Logic "0" Enable (Outputs "ON")	1.5V max
Logic "1" Enable (Outputs "OFF")	3.5V min
Loading	0.1 μA max
Clock Pulse Width	46 nsec min
Start Pulse Width	50 nsec min
DIGITAL OUTPUTS	
Parallel Outputs	
Output Current "0" and "1"	1.6 mA min
Logic "1"	2.4V min
Logic "0"	0.4V max
Serial and EOC Output Fanout[1]	5 TTL Loads
Delay from Enable Pulse to Data Valid	85 nsec typ 120 nsec max
REFERENCE, INTERNAL	
Voltage	6.3V ±5%
Drift	25 ppm/°C
Output Current	200 μA max
CONVERSION TIME[2]	2.5 μ sec max
ACCURACY	
Absolute Accuracy[3]	±1/2 LSB typ ±1 LSB max
Absolute Accuracy (−55°C to +125°C)	±2 LSB max
Zero Error	±1/4 LSB typ ±1/2 LSB max
−55°C to +125°C	±1/2 LSB typ ±1 LSB max
Linearity (−55°C to +125°C)	±1/4 LSB typ ±1/2 LSB max
No Missing Codes (−55°C to +125°C)	Guaranteed
POWER SUPPLY	
Requirements	
+15	+14.5V to +15.5V @ 20 mA max
−15	−14.5V to +15.5V @ −13 mA max
+5	+4.75V to +5.25V @ 101 mA max
Rejection Ratio	
+15	±0.03% FSR/% Supply
−15	±0.01% FSR/% Supply
Power Consumption	680 mW typ 1000 mW max
TEMPERATURE	
Operating	
C- Model	0°C to 70°C
B- Model	−55°C to +125°C
Storage	−65°C to +150°C

NOTES:

1. A TTL Load is defined as 40 μA at Logic "1" and 1.6 mA at Logic "0".
2. Conversion time of 2.5 μ sec corresponds to an external clock frequency of 3.6 MHz
3. Absolute Accuracy includes all errors gain, zero and linearity.

PACKAGE OUTLINE

Case Dimensions max unless otherwise noted.



*0.030 (0.76) +0.010 (0.25) STANDOFFS, SUPPLIED AT MANUFACTURERS OPTION.

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	SERIAL OUT	13	−15V
2	BIT 4	14	V_{REF} OUT (6.3V)
3	BIT 3	15	DATA ENABLE
4	BIT 2	16	+15V
5	BIT 1 (MSB)	17	BIT 8 (LSB)
6	+5V	18	BIT 7
7	BIPOLAR OFFSET	19	BIT 6
8	SUMMING JUNCTION	20	BIT 5
9	BIPOLAR OFFSET	21	EOC
10	ANALOG GND	22	DIGITAL GND
11	10V INPUT	23	CLOCK
12	20V INPUT	24	START

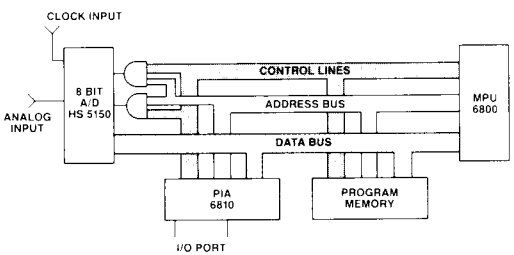
ABSOLUTE MAXIMUM RATINGS

+15V Suppy . . . . . −0.5V to +18V
−15V Supply . . . . . +0.5V to −18V
5V Supply . . . . . −0.5V to +7V
Analog Input . . . . . ±20V
Digital Inputs . . . . . −0.5V to +5.5V

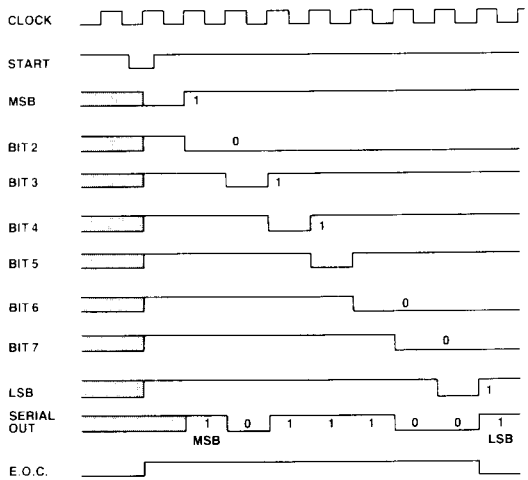
APPLICATIONS INFORMATION

The three state outputs of the HS 5150 make interfacing to data busses of minicomputers very easy. A typical application would consist of using the HS 5150 in the basic 6800 microprocessor system as shown in the block diagram below.

In this application, the HS 5150 is treated as a memory location and is addressed by using the extended addressing mode. Just two instructions are needed to acquire the desired information. First, the HS 5150 receives a start command by the use of a STORE instruction, and then a LOAD or arithmetic instruction is used to obtain the digital information by addressing the HS 5150 as a memory location. Since the HS 5150 converts in 2.5 μ sec, there is no delay waiting for the information to be valid. Several HS 5150s may be incorporated in one system by changing the address of the enable signal. The HS 5150 may be used in a similar manner with other microprocessors.



TIMING DIAGRAM



NOTES:

1. Shaded area represents indeterminate logic level.
2. Code shown represents an analog input of +7.226 volts for the 0 to +10 volts range.
3. The converter will reset on the first rising edge of the clock after the start command has gone low. Conversion will begin on the first rising edge of the clock after the start has returned high.
4. The start has to be low for a minimum of 50 nSec prior to the edge of the clock.
5. The EOC will go low approximately 45 nSec prior to Bit 8 (LSB) being valid.
6. For continuous conversion connect the EOC to the start command.

TRANSFER CHARACTERISTICS

DIGITAL OUTPUT		ANALOG INPUT RANGE						
MSB	LSB	0 to +5	0 to +10	±2.5	±5	±10	0 to −5	0 to −10
0000	0000	0	0	−2.500	−5.000	−10.000	−4.981	−9.961
0000	0001	+0.019	+0.039	−2.481	−4.961	−9.922	−4.961	−9.922
0111	1111	+2.481	+4.961	−0.019	−0.039	−0.078	−2.500	−5.000
1000	0000	+2.500	+5.000	0	0	0	−2.481	−4.961
1111	1110	+4.961	+9.922	+2.461	−4.922	−9.844	−0.019	−0.039
1111	1111	+4.981	+9.961	+2.481	+4.961	+9.922	0	0
Input Impedance		2.5K	5K	2.5K	5K	10K	2.5K	5K
Connect Input to Pin		11	11	11	11	12	11	11
Connect Pin 8 to Pin		12	Open	12 & 9	9	9	12,7 & 9	9,7
Connect Pin 10 to Pin		7 & 9	7 & 9	7	7	7	NC	NC

*Voltages given are theoretical values for the transitions indicated. Ideally, the digital output will change as the input voltage passes through the voltage level indicated.

APPLICATIONS INFORMATION (continued)

OPERATION

Data Enable — The data enable line controls the state of the parallel outputs. For a high impedance output (outputs in the off state) the Data Enable line must be at a logic "1" level. For the data to be available on the outputs, the Data Enable line must be at a logic "0" level. Data will be available 120 nsec (max) after the Data Enable goes low.

Grounds — To obtain optimum performance analog and digital grounds are not connected internally and must be tied together as close to the unit as possible. If these grounds must run separately, a non-polarized 0.01 μ F capacitor should be connected between Pins 10 and 22. The power supplies should be decoupled with a tantalum or electrolytic type capacitor located as close to the HS 5150 as possible. For optimum performance, a 1 μF paralleled by a 0.01 μ F ceramic capacitor should be connected between analog ground and the $\pm$ 15 volt supplies and between digital ground and the + 5 volt supply.

Analog Input — Since the HS 5150 is a high speed converter, the signal source must have a low output impedance at high frequencies to allow for fast changes in the current sinking and sourcing to the analog input. A suitable amplifier would be the Harris HA2525 operational amplifier or a high speed sample and hold amplifier such as Hybrid Systems' HS 346.

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 5150C	COMM., 8-BIT, ADC
HS 5150B	MIL., 8-BIT, ADC